Optimizing the Load Transient Response of the Buck Converter

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***Abstract*—Optimized gain of the voltage-error amplifier and current-mode control provide instantaneous transient response and small dc shift of the output voltage for step changes in the load current. This paper analyzes the system, determines the best compensation, provides design guidelines for buck converters powering Pentium® II processors, and presents results of simulations and experiments.**

I. INTRODUCTION

Dc/dc converters for powering high-performance microprocessors must have small transient deviation to a step change in the load current. The step load-current change is the result of active power management. The rate of change of load current is in the order of 30 A/μs. If the output voltage deviates more than a few percent from the nominal value due to the step load-current change proper operation is not guaranteed.

This paper deals with the issue of optimizing the load transient response of the synchronous buck converter. (That converter is the preferred choice in microprocessor power-supply applications.) First, the power-supply specifications of the Intel Pentium® II processor are reviewed. Then the theoretical limits of the load transient response of the buck converter are determined. This is followed by a brief overview of the known load transient reduction techniques (increasing the output capacitance, load-current or capacitor-current feedforward, V^2 architecture, zero-impedance converter). After the overview, the optimal load transient response of the processor power supply is determined. We then synthesize the required output impedance of the buck converter with a constant-off-time current-mode controller, determine the compensation of the error amplifier, and provide a design procedure. Computer simulations and experimental results complement the theoretical derivations.

II. OBJECTIVE SPECIFICATIONS

Due to the presence of active power management, the supply current of the new Pentium® II family of Intel microprocessors changes rapidly and over a wide range during normal operation of the computer. The changes in the supply current are the results of stopping the clock to various internal sections of the processor. Three states are to be considered with reduced power consumption, Stop-Grant, Sleep, and Deep Sleep.

Table I [1] presents the voltage and current specifications for the processor during the three states.

TABLE I
PENTIUM® II PROCESSOR VOLTAGE AND CURRENT SPECIFICATIONS

Symbol	Parameter	Processor core freq. (MHz)	Min.	Typ.	Max.	Unit
Vcc_{CORE}	Vcc for processor core			2.8		V
	Vcc_{CORE} static tolerance		–0.060		0.100	V
	Vcc_{CORE} transient tolerance	233 266 300	–0.140 –0.140 –0.130		0.140 0.140 0.130	V V V
Icc_{CORE}	Current for Vcc_{CORE}	233 266 300		6.9 7.8 8.7	11.8 12.7 14.2	A A A
$Icc_{SGNTCORE}$	Icc for Stop-Grant Vcc_{CORE}	233 266 300		0.8 0.9 TBD	1.1 1.2 TBD	A A A
$Icc_{SLPCORE}$	Icc for Sleep Vcc_{CORE}			0.070	0.080	A
$Icc_{DSLPCORE}$	Icc for Deep Sleep Vcc_{CORE}				0.020	A
$dIcc_{CORE}/dt$	Icc slew rate				30	A/μs

According to [1], the output voltage measured at the converter output pins on the system board must be within the transient range shown in Table I, including the transition from $Icc_{SGNTCORE}$ (Stop-Grant state) to Icc_{CORE} (Maximum) or from Icc_{CORE} (Maximum) to $Icc_{SGNTCORE}$ (Stop-Grant state), except for input voltage turn-on and turn-off. This tolerance must include the variation due to dc voltage regulation plus the effects of an output load transient (slew rate) of 30 A/μsec at the converter output pins. The load transient response may not exceed the static voltage specification for longer than 2 microseconds. The toggle rate for the output load transition may range from 100 Hz to 100 kHz. Under the above conditions and for all toggle rates, the transient response must be measured over a 20 MHz frequency band, and at ambient temperatures between 25°C and 50°C.

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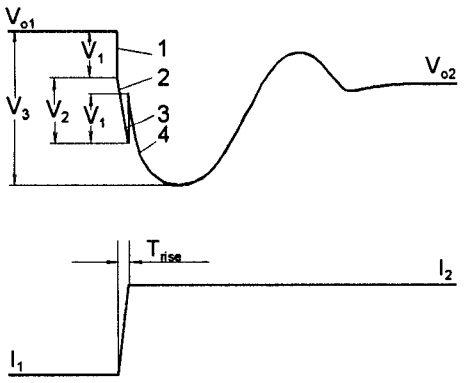

Fig. 1. Output voltage (top) and load current (bottom).

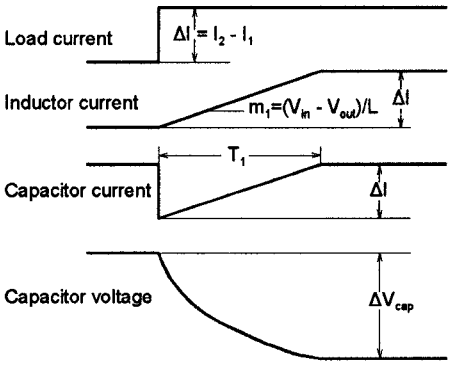

Fig. 2. Waveforms for the calculation of the minimum achievable peak deviation of the capacitor voltage.

III. THEORETICAL LOAD TRANSIENT RESPONSE PERFORMANCE LIMITS

Fig. 1 shows the typical output voltage transient (top) and the load current that generates it (bottom). The transient comprises four distinct sections. In section 1 the output voltage steps downward from its steady-state value V_{o1} by a voltage V_1. This step is caused by the equivalent series inductance, ESL (or L_e), of the output capacitor of the switching regulator. The magnitude V_1 of the step is equal to the product of L_e and the rate of change, or *di/dt*, of the load current. The *di/dt* is equal to $(I_2 - I_1)/T_{rise}$. In section 2 the output voltage continues to move downward, but as a ramp function rather than a step function. The magnitude V_2 of the ramp voltage is equal to the product of the load current and the equivalent series resistance, ESR (or R_e) of the output capacitor. In section 3 the output voltage steps in the opposite direction (upward). Again, this step is caused by the combination of the change in the *di/dt* of the load current and the ESL of the output capacitor. The magnitude of the step is V_1. In section 4, the output voltage continues to move but at a much slower rate than in the first three sections. The peak deviation of the output voltage from the initial value is V_3; eventually the output voltage settles to a new value V_{o2}. In section 4 the time function of the output voltage is determined by the dynamic behavior of the converter and by the applied control method.

Considering the presently practical switching frequencies (100 to 500 kHz) and the 30 A/μsec rate of change of the load current, even with an optimal controller it would not be possible to reduce the peak deviation of the output voltage below the value:

$$V_1 + V_2 = \frac{I_2 - I_1}{T_{rise}} L_e + (I_2 - I_1) R_e \qquad (1)$$

The minimum achievable peak deviation of the capacitor voltage of the buck converter (neglecting for the moment the ESL and ESR of the capacitor and assuming optimal control) can be calculated from the waveforms shown in Fig. 2. The top trace in that figure shows the load current, the second trace from the top shows the current in the filter inductor of the converter, the third trace from the top shows the current in the output capacitor of the converter, and the bottom trace shows the deviation of the output voltage. In the figure and in the expression for the peak deviation, the ripple current in the inductor and the ripple voltage across the capacitor are neglected, for simplicity. The result is

$$\Delta V_{cap,down} = \frac{\Delta I^2}{2(V_{in} - V_{out})} \frac{L}{C} \qquad (2)$$

At suddenly decreasing load, the voltage deviation would be upward. For that case, the peak deviation in the capacitor voltage is

$$\Delta V_{cap,up} = \frac{\Delta I^2}{2V_{out}} \frac{L}{C} \qquad (3)$$

In (2) and (3) L is the inductance of the energy-storage inductor of the buck converter and C is the capacitance of the output capacitor.

Although usually the effect of the ESL can be neglected due to the high-frequency bypass capacitors around the processor, the effect of the ESR must be taken into account. The output voltage of the converter is equal to the sum of the resistive and capacitive voltage drops. The voltage deviation vs. time function is

$$\Delta v_o(t) = t^2 \frac{m}{2C} + t\left(m R_e - \frac{\Delta I}{C}\right) - R_e \Delta I \qquad (4)$$

where $m = (V_{in} - V_{out})/L$ or $m = -V_{out}/L$ is the slope of the inductor current. It is a straightforward matter to calculate the minimum or maximum peak deviation of the output voltage from (4).

IV. OVERVIEW OF LOAD TRANSIENT REDUCTION TECHNIQUES

The most obvious "brute-force" solution for reducing the transient deviation is to increase the capacitance at the output of the converter. As (2) and (3) show, the capacitive deviation is inversely proportional to that capacitance. Also, more capacitance usually has less ESR, leading to a smaller resistive deviation. Unfortunately, more capacitance with less ESR costs

more and requires more volume and board area. In addition, even with a large capacitor, the voltage-regulating loop must be fast enough to command full (or zero) duty ratio in a fraction of the theoretically achievable minimum current ramp-up (or ramp-down) time (T_1 in Fig. 2). If the loop response is sluggish, the peak deviation tends to approach the open-loop value of the deviation, which is

$$\Delta V_{cap,open-loop} = \Delta I \sqrt{\frac{L}{C}} \qquad (5)$$

In the past much effort was expended on improving the transient response by using the information on the load current. References [2] to [6] discuss various versions and developments of the load-current feedforward technique.

The idea of combining current-mode control with feedforward of the load current was first introduced in [2]. Reference [3] presented experimental results in a buck converter application.

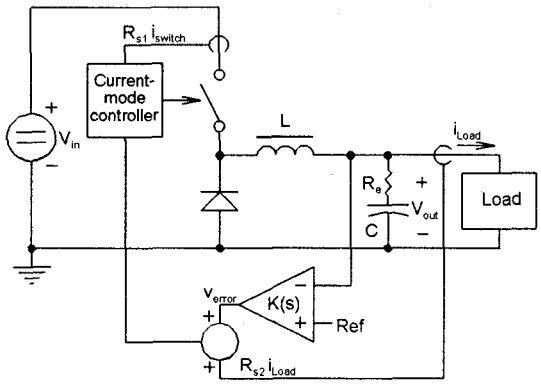

Fig. 3. Load-current feedforward.

Fig. 3 shows the basic concept of load-current feedforward. By summing the voltage-error signal and a signal proportional to the load current, and feeding the sum to the current-mode controller, the switch (or inductor) current will automatically and without delay follow the load-current variations even if the gain of the voltage-regulating loop reaches zero dB at a low frequency. The concept works with any kind of current-control technique, but best performance can be obtained when the current-command signal and the inductor current are closely related, e.g., hysteretic control [7] or constant-off-time control.

Reference [4] discusses the case when the feedforward signal is the current of the output capacitor instead of the load current (Fig. 4). The advantage is that a small current transformer can be used for current sensing, which makes the circuit implementation simpler and reduces the loss in the sense resistor. The dc current information is lost, however, therefore additional circuitry is required for overcurrent protection.

The recently proposed V^2 architecture [5] (Fig. 5) eliminates the external current sensor, instead it uses the ESR of the output capacitor for obtaining information on the current. The control method is constant-off-time current-mode control. As was the case in [4], additional circuitry is required for overcurrent protection. Also, relying on the widely varying ESR of electrolytic capacitors gives cause for concern. The effect of the capacitive component of the output voltage is not discussed in [5], and it is not known how the system performs if the capacitive component is commensurate with the resistive component.

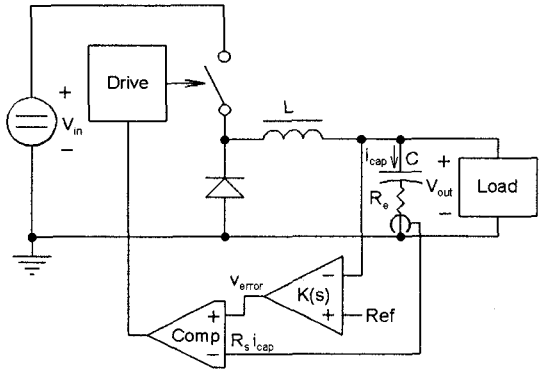

Fig. 4. Feedforward of the capacitor current.

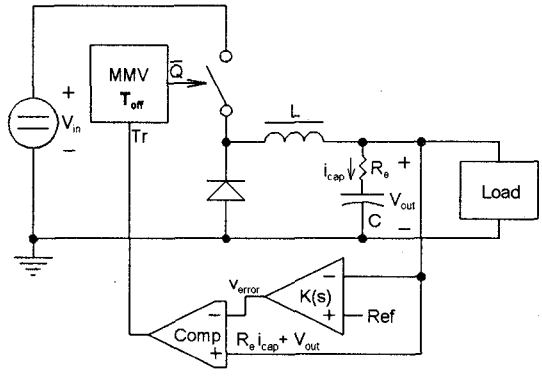

Fig. 5. V^2 architecture.

Reference [6] describes the 'zero-impedance' converter. Nominally zero output impedance is achieved by closing a positive current feedback loop inside the negative voltage-feedback loop, and by choosing the transfer function of the current feedback loop appropriately. The zero-impedance converter is essentially a converter with load-current feedforward.

V. OPTIMAL LOAD TRANSIENT RESPONSE

Neglecting for a moment the effect of the ESL, a step change of ΔI in the load current causes an initial change in the output voltage of a dc/dc converter that is equal to the product of the ESR and ΔI. It is not possible to reduce the transient deviation below that value. For a given capacitor technology, the cost of the capacitors tends to be inversely proportional to the ESR:

The smaller the ESR is, the more expensive the capacitor will be. Therefore, it makes economical sense to select a capacitor which has a worst-case ESR that is just below the limit determined by the transient tolerance specifications, e.g., the ones shown in Table I.

Accordingly, the optimal load transient response is as follows: After the initial inductive overshoot or undershoot, the output voltage moves to, and stays at, the extreme value (minimum in normal state, maximum in stop-grant state) of the static tolerance (taking, of course, into account the ripple voltage, and the initial tolerance and drift of the control circuit). That position allows the use of capacitors with the highest ESR and, consequently, lowest cost. Figs. 6a and 6b illustrate the point. Fig. 6a shows the specified supply voltage tolerance bands for the 300-MHz Pentium® II processor, together with the optimal load transient response, where the light-load static output voltage is at the maximum value and the heavy-load static output voltage is at the minimum value. It is assumed that the setpoint tolerance of the converter is ±0.75% and the ripple voltage is 1% peak-to-peak. From the figure it can be determined that the total available low-frequency deviation for a 13-A load change is 90 mV. That allows an ESR of 90m/13 = 6.9 mΩ. If both the light-load and heavy-load static output voltages would be equal, as per Fig. 6b, the available low-frequency deviation would be only 24 mV, allowing an ESR of only 24m/13 = 1.85 mΩ. That would require a capacitor with about one-fourth ESR of the previous case, or about four times the size and cost.

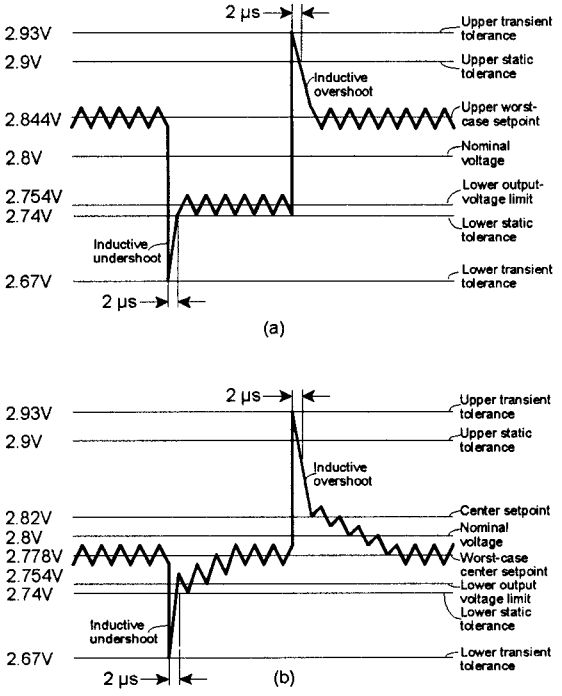

Fig. 6. Load transient responses and supply voltage tolerance bands for the 300-MHz Pentium® II processor: (a) load transient response with dc shift, (b) load transient response without dc shift. Response (a) tolerates a much larger ESR than response (b).

It is clear that none of the above discussed load transient reduction techniques, including the V^2 technique, is optimal for processor power supply applications. The reason is that they all tend to bring back the output voltage to the same set point, and thus they effectively double the peak-to-peak deviation of the output voltage. It is also clear that the optimal output impedance (the one that provides the best exploitation of the output capacitance) is resistive and equal to the ESR. In the next section we shall discuss how to design the system for producing an output impedance that is equal to the ESR

VI. DESIGN FOR OPTIMAL OUTPUT IMPEDANCE

A. Required Voltage-Error Amplifier Transfer Function

The first step in the design is to determine the output impedance of the feedback-regulated converter. That can be done, for example, by using the method of injected/absorbed currents discussed in [8]. Fig. 7 shows the equivalent circuit of the system. In the figure $A(s)$ and $B(s)$ are the characteristic coefficients that describe the dynamic behavior of the converter. $A(s)$ is the relationship between the controlled quantity, which is the inductor current for current-mode controlled converter, and the current injected toward the load. $B(s)$ is the measure of the dependence of the injected current from the output voltage. In the equivalent circuit the effect of the input voltage variations is neglected, which is a reasonable assumption for current-mode controlled buck converters. R_s is the value of the current-sense resistor.

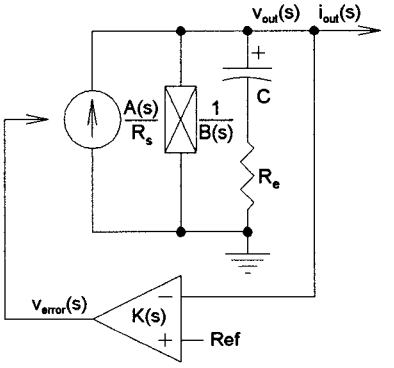

Fig. 7. Equivalent circuit of the feedback regulated converter (for determining the output impedance).

The following equation can be written for the system in Fig. 7:

$$\left[v_{out}(s)\cdot K(s)\frac{A(s)}{R_s} - i_{out}(s)\right]\left[\frac{1}{B(s)}\left\|\left(R_e+\frac{1}{sC}\right)\right.\right] = v_{out}(s) \tag{6}$$

From (6) the output impedance is

$$Z_{out}(s) = -\frac{v_{out}(s)}{i_{out}(s)} = \frac{1+sR_eC}{B(s)+sC\left[1+B(s)R_e\right]-K(s)A(s)R_s^{-1}\left(1+sR_eC\right)} \tag{7}$$

Substituting R_e for the output impedance and solving for $K(s)$ yields the following transfer function for the voltage-error amplifier:

$$K(s)=\frac{B(s)+sCB(s)R_e-R_e^{-1}}{A(s)R_s^{-1}(1+sCR_e)} \tag{8}$$

A good choice for controlling the converter is constant-off-time current-mode control (Fig. 8). That control technique features high rejection ratio for input voltage variations, quick response from the control input to the inductor current, and allows the use of only the switch peak current information. Hysteretic current-mode control [7] also provides high input-voltage rejection ratio and quick control-to-inductor current response, but requires that both the peak and valley current information be available. In addition, hysteretic control is patented, while constant-off-time control is in the public domain. Other current-mode control techniques (constant-frequency peak current control, PWM conductance control, average current control) are also less advantageous than constant-off-time control.

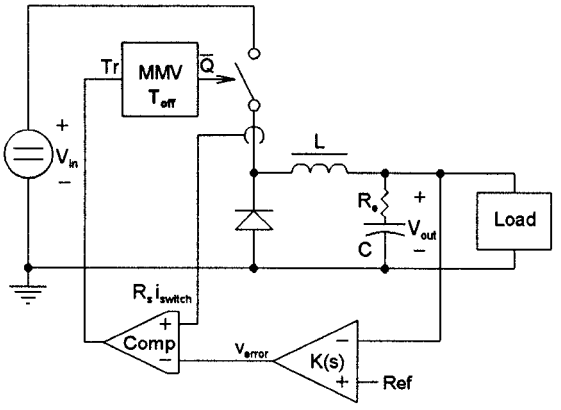

Fig. 8. Constant-off-time current-mode control.

The characteristic coefficients of the constant-off-time current-mode-controlled buck converter are as follows.

$$A(s)=1 \qquad B(s)=-\frac{T_{off}}{2L} \tag{9}$$

Substituting the characteristic coefficients in $K(s)$ yields

$$K(s)=-\frac{R_s\left(\frac{1}{R_e}+\frac{T_{off}}{2L}+sCR_e\frac{T_{off}}{2L}\right)}{1+sCR_e} \tag{10}$$

Recognizing, that the zero in (10) is typically well above the switching frequency, the last term in the numerator can safely be neglected. Also, in most practical applications, R_e is usually much smaller than $T_{off}/2L$, which means that the required transfer function is

$$K(s)=-\frac{R_s}{R_e}\frac{1}{1+sCR_e} \tag{11}$$

This transfer function can be easily realized with an operational amplifier as shown in Fig. 9. The ratio R_2/R_1 must be equal to R_s/R_e, and the product R_2C_1 must be equal to the time constant R_eC of the output capacitor. Note that if the R_eC time constant is commensurate with, or smaller than, the switching period, the pole of the transfer function can be neglected, and C_1 can be omitted from the error amplifier. Note also that the dc shift of the output voltage is proportional to the value of the sense resistor. A large tolerance in the sense resistance (e.g., using the $R_{DS(ON)}$ of the MOSFET for current sensing) would greatly reduce the available dc shift and would require an output capacitance with extremely small ESR.

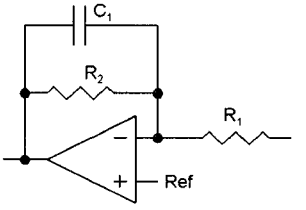

Fig. 9. Voltage-error amplifier compensation.

B. Design Procedure

The steps of a typical design for meeting the load transient requirements of the Pentium® II application are as follows.

1) Determine the maximum acceptable ESR of the output capacitor from the allowable dynamic deviation and the magnitude of the load current step.

$$R_{e(\max)}=\frac{\Delta V_{out}}{\Delta I_{out}}=\frac{90\text{m}}{13}=6.9\,\text{m}\Omega \tag{12}$$

2) Calculate the minimum inductance of the energy-storage inductor from the ESR, off time, dc output voltage, and peak-to-peak output ripple voltage.

$$L_{\min}=\frac{V_{out}T_{off}R_e}{V_{ripple,p-p}}=\frac{2.8\cdot 2.5\mu\cdot 6.9\text{m}}{20\text{m}}=2.4\,\mu\text{H} \tag{13}$$

3) Determine the minimum capacitance of the output capacitor from the requirement that the output be held up while the inductor current ramps up (or down) to the new value. The minimum capacitance would produce an initial *dv/dt* which is equal (but opposite in sign) to the *dv/dt* generated by the *di/dt* in the inductor and the ESR of the capacitor.

$$C_{\min}=\frac{\Delta I}{R_e(di/dt)}=\frac{13}{6.9\text{m}\cdot[2.2/(1.2\cdot 2.4\mu)]}=2.47\text{mF} \tag{14}$$

Here *di/dt* is the rate of rise or fall of the inductor current, whichever is smaller. It is assumed that the minimum voltage across the inductor is 2.2 V and the inductor tolerance is 20%.

4) Select a capacitor that has more capacitance and less ESR than the values calculated from (14) and (12).

5) Select the input and feedback resistors for the voltage-error amplifier (or the terminating resistor in the case when the error amplifier is of the transconductance type) such that the dc gain is equal to the ratio of the current sense resistor and the ESR of the output capacitor.

6) Select a compensating capacitor such that it provides a pole frequency in the transfer function of the error amplifier that is equal to $1/(2\pi R_e C)$.

VII. RESULTS OF COMPUTER SIMULATIONS AND EXPERIMENTS

Computer simulations were conducted both with an averaged nonlinear model using the demo version of Micro-CAP V and with a complete switched model using the demo version of PSIM. (The demo versions of Micro-CAP V and PSIM can be downloaded from http://www.spectrum-soft.com and http://portal.ca/~powersim, respectively.) Fig. 10 shows the averaged nonlinear model, where the error amplifier is implemented as a transconductance amplifier. The averaged model does not reveal the details on the time scale of the switching cycle but is fast and quite useful for quick studies regarding sensitivities to parameter variations. For example, Figs 11a and 11b show the effects of the variations of the ESR and output capacitance on the load transient.

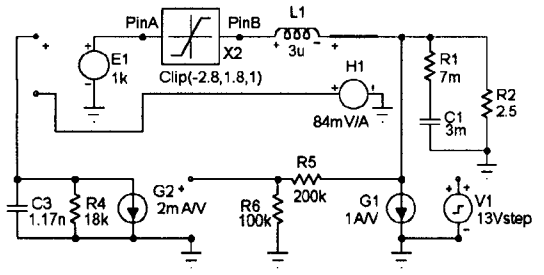

Fig. 10. Averaged nonlinear model.

The switched model is useful for determining the output ripple, ripple-feedback instabilities, and the details of various switching waveforms. For example, Fig. 12 shows the output voltage and the inductor current for the same set of parameters as in Fig. 10. As can be seen both in Figs 11 and 12, for the nominal output capacitance of 3 mF and nominal ESR of 7 mΩ the transient responses are virtually identical.

We also took experimental data on a test circuit controlled by a new constant-off-time current-mode controller IC, the ADP3152 from Analog Devices. This IC features the VID output voltage programming and status monitor signal required in the Pentium® II guidelines of [1]. Another version of the IC (ADP3153) includes a controller for a low-dropout (LDO) linear regulator, to be used in multi-processor applications.

Fig. 13 shows the schematic of the test circuit. In order to demonstrate the optimal response theory, we chose the compensation not based on the worst case parameters, but on the measured parameters. We used six pieces of 560-μF, 25-V, FA series Panasonic aluminum electrolytic capacitors in parallel. The ESR of the six parallel capacitors was 6.15 mΩ. Thus the 13 A load step produced an approximately 80 mV step in the output voltage. The total capacitance of 3.36 mF and ESR of 6.15 mΩ limited the inductance to less than 3.5 μH [calculated from (14)]. We selected 3.3 μH.

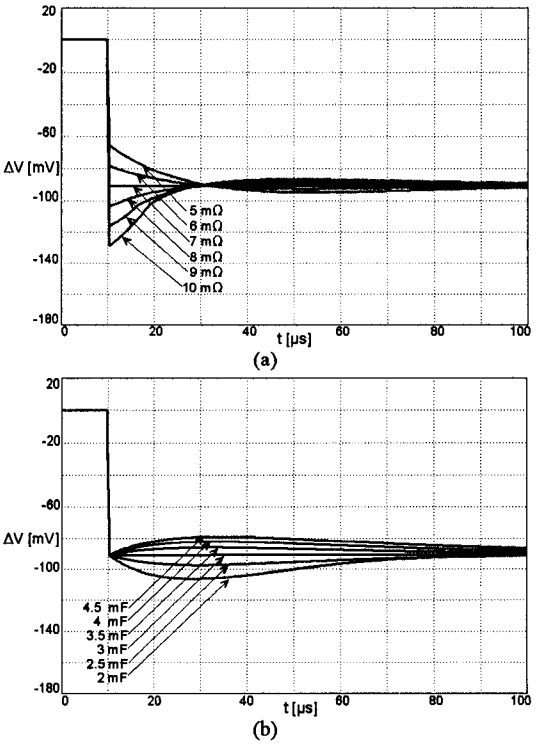

Fig. 11. Effects of the variations of the ESR (a) and output capacitance (b) on the load transient.

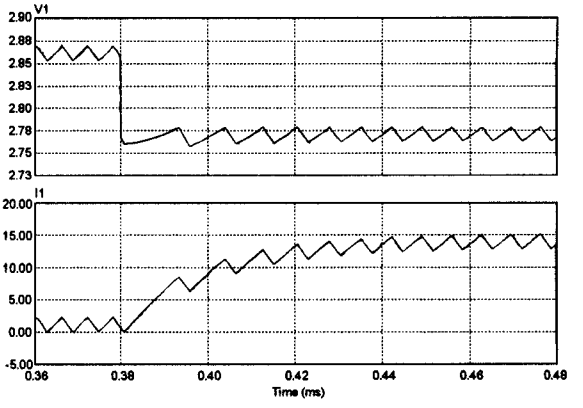

Fig. 12. Simulated output voltage (top trace) and inductor current (bottom trace).

To determine the compensation and to create an intentional output voltage offset, it is necessary to understand the components of the feedback network. The sensed output voltage is divided by three, is measured against a reference voltage by a transconductance amplifier with a transconductance of 2.2 mS, develops a voltage via the

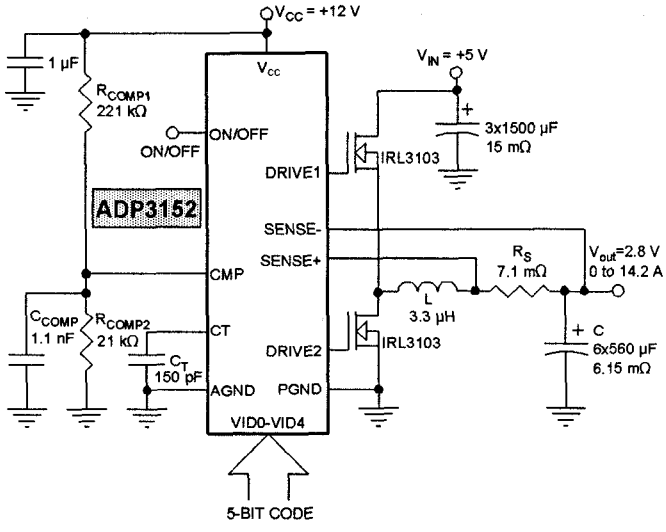

Fig. 13. Test circuit schematic.

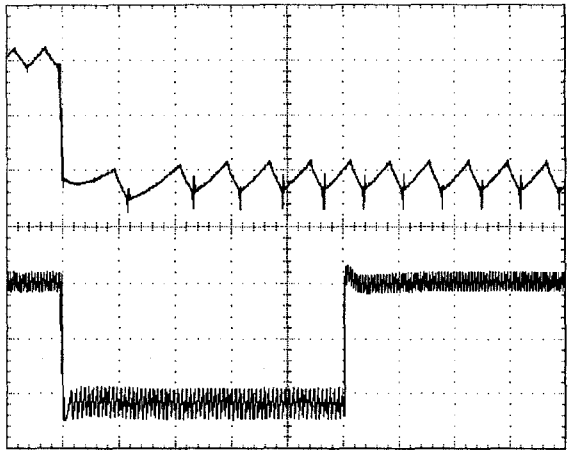

Fig. 14. Measured load transient response. Both traces show the output voltage response to a 13-A change in the load current, but with two different time scales, 10 µs/div. (top trace) and 100 µs/div. (bottom trace). Vertical scale: 40 mV/div.

compensation termination, is divided by 12, and with that voltage the peak current is programmed. Those are the gain factors. The offset is determined by noting that the output of the transconductance amplifier commands zero current when it is at approximately 0.7 V, and that voltage also corresponds to a balanced input. Thus, when the output voltage equals three times the reference voltage, the transconductance amplifier will have a net output of zero current.

The compensation components for the ADP3152 were chosen as follows. The equivalent current sensing resistor was chosen to be 7.1 mΩ. That produces a nominal 100 mV drop at 14 A load—allowing sufficient headroom for ripple current below the peak current limiting threshold of 130 mV. According to the text, we should set the dc gain (from output voltage to current-programming voltage) equal to the ratio of the current sense resistor R_s and the ESR, R_e. The loop transconductance G_m, from output voltage to inductor current, will be the transconductance amplifier gain, 2.2 mS, divided by both 3 at the front end and 12 at the tail end, for a net transconductance of 61µS. Therefore, the terminating resistance should be set equal to $R_s/(R_e G_m)$, or 7.1m/(6.15m x 61µ) = 19 kΩ. Since the IC is powered by a regulated 12 V supply, we can calculate two resistors to create a divider from 12 V which yields 1.3 V, and which has an impedance at the divider tap of 19 kΩ. That yields the values that we used in the test circuit: 221 kΩ (top), and 21.0 kΩ (bottom).

Since the amplifier termination time constant should equal that of the output capacitance and ESR, the amplifier termination capacitance should be 1.1 nF. That value was also used in the circuit.

Fig. 14 shows the transient response, with two different time scales. It is clear that we were able to achieve the desired and predicted response. The response of the output current is balanced nearly perfectly against the output capacitor impedance to prevent both the overshoot, which would widen the dynamic regulation tolerance, and the undershoot, which if the load step were to revert at the point where the undershoot is highest, would also widen it.

SUMMARY

Switched-mode power converters are limited by current technology to switch at speeds slower than the 2 µs which is allowed for dynamic regulation of a Pentium® II processor. Thus the output capacitor impedance sets the limit of achievable response capability for a power converter. By first choosing that capacitor according to the minimum impedance required by the load specification, and then tailoring the compensation to match that impedance according to the guidelines set forth in this paper, the converter can have an instantaneous response (180 degrees of phase margin) to a load step change. The regulation performance is limited only by the actual output capacitors.

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