Optimum Harmonic Reduction With a Wide Range of Modulation Indexes for Multilevel Converters

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***Abstract*—This paper proposes a novel modulation technique to be applied to multilevel voltage-source converters suitable for high-voltage power supplies and flexible ac transmission system devices. The proposed technique can generate output stepped waveforms with a wide range of modulation indexes and minimized total voltage harmonic distortion. The main power devices switch only once per cycle, as is suitable for high-power applications. In addition to meeting the minimum turn-on and turn-off time requirements for high-power semiconductor switches, the proposed technique excludes from the synthesized waveform any pulses that are either too narrow or too wide. By using a systematic method, only the polarities and the number of levels need to be determined for different modulation levels. To verify the theory and the simulation results, a cascaded converter-based hardware prototype, including an 8-b microcontroller as well as modularized power stage and gate driver circuits, is implemented. Experimental results indicate that the proposed technique is effective for the reduction of harmonics in multilevel converters, and both the theoretical and simulation results are well validated.**

***Index Terms*—High-voltage power supplies, multilevel converters, pulsewidth modulation.**

I. Nomenclature

m	Number of switching angles.
V_k	kth level dc voltage.
n	Odd harmonic order.
α_k	kth switching angle.
$t_{\text{on(min)}}$	Minimum turn-on time of the semiconductor device.
$t_{\text{off(min)}}$	Minimum turn-off time of the semiconductor device.
$\text{Max}()$	Maximum function.
f_L	Line frequency.
h_1	Amplitude of the fundamental component.
h_n	Amplitude of the nth harmonic voltage.
V_{dc}	Voltage of dc sources.
M	Multilevel modulation index.

II. Introduction

RECENTLY, multilevel voltage-source converters have become an important technology in high-power applications. Several multilevel converter topologies [1]–[4] and modulation techniques [5]–[8] have been developed for and applied to high-power systems. With devices or converter modules in series and with balanced voltage sharing among them, the lower voltage rated switches can possibly be used in high-voltage multilevel converters. Given the requirements for quality and efficiency in high-power systems, as well as the limitations of switching speed, low switching frequency and small total harmonic distortion (THD) are desirable. By applying appropriate modulation schemes, these two goals can be achieved simultaneously. The challenge of the modulation techniques, therefore, plays a very important role in multilevel converter circuits.

Previous harmonic optimization techniques in [3] and [6] initiated the concept of achieving harmonic reduction using selected harmonic elimination. These techniques require more than one switching per cycle to obtain a wide modulation index range. In this paper, the proposed modulation technique involves generalizing the optimum harmonic reduction technique that switches the main power devices once per cycle, and at the same time, achieving a wide range of modulation indexes. The output voltage presents a stepped-type wave shape, similar to what can be achieved with the traditional methods. This method is fairly simple to implement in multilevel converters. The basic concept is to swap the polarity of some levels so that a low modulation index can be obtained. The computation effort is seamless for the entire range of modulation indexes. Consider, for example, a seven-level cascaded inverter. The traditional selected harmonic elimination can only reach the modulation index of 0.5. The proposed method, however, indicates that the modulation index of 0.1 can be easily achieved.

III. Optimized Harmonic Stepped-Waveform Technique

A. Conventional Stepped Waveforms

Fig. 1 shows a generalized quarter-wave symmetric stepped-voltage waveform synthesized by a $2m + 1$ level converter, where m is the number of switching angles. By applying the Fourier series, the amplitude of any odd nth harmonic of the stepped waveform can be expressed as (1), whereas the amplitudes of all even harmonics are zero

$$h_n = \frac{4}{n\pi}\sum_{k=1}^{m}[V_k \cos(n\alpha_k)]. \tag{1}$$

According to Fig. 1, α_1 to α_m must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \cdots < \alpha_m < \frac{\pi}{2}.$$

Consider (1). To minimize harmonic distortion and to achieve adjustable amplitude for the fundamental component, up to

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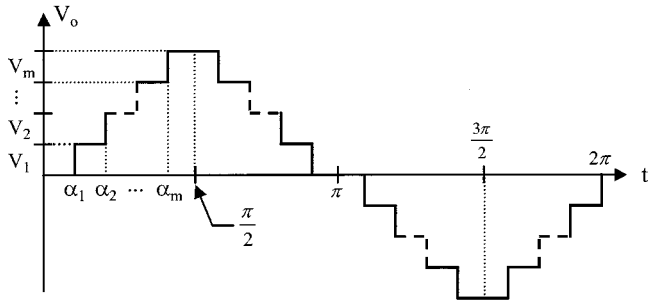

Fig. 1. Generalized $2m + 1$-level quarter-wave stepped-voltage waveform.

$m - 1$ harmonic components can be removed from the voltage waveform. In general, the most significant low-frequency harmonic components will be chosen for elimination. Then, high-frequency harmonic components can be readily removed by using additional filter circuits. According to (1), to keep a constant number of eliminated harmonics, all switching angles must be less than $\pi/2$. However, if the switching angles do not satisfy the condition, this scheme no longer exists. As a result, this modulation scheme basically provides a narrow range of modulation indexes, which is the main disadvantage. For example, in a seven-level, equally stepped waveform, to continue eliminating two surplus harmonic components, its modulation index is only available from 0.5 to 1.05. At any modulation index lower than 0.5, if this scheme is still applied, the number of harmonic components that might be eliminated will reduce from two to one. As a result, a low-order harmonic component appears in the output waveform. In turn, the total voltage harmonic distortion increases. In Section III-B, a new technique is presented to overcome the limitation of the conventional scheme.

B. New Stepped Waveforms

As discussed in Section III-A, the traditional stepped waveform provides a narrow modulation index range. This paper, therefore, proposes a new modulation technique, which is an extension of the conventional stepped-waveform technique. The proposed technique can generate output voltage waveforms with a wide range of modulation indexes. With a set of appropriate switching angles, this proposed modulation scheme also minimizes the THD of the synthesized waveforms for certain modulation indexes. In addition to meeting the minimum turn-on and turn-off time requirements for high-power semiconductor devices, the proposed technique avoids the undesirable pulses from the synthesized waveform.

To minimize the THD of the line voltage, the lowest significant $m - 1$ nontriplen harmonic components need to be eliminated from the synthesized phase voltage, where m is the number of switching angles in the phase voltage waveform. Take a three-phase seven-level stepped waveform as an example. In this case, $m = 3$. To minimize line-to-line voltage harmonic distortion and to achieve an adjustable amplitude for the fundamental component, from (1), up to two surplus harmonics are selected for removal. Thus, the fifth and seventh harmonics, the two lowest nontriplen harmonics, are chosen to be eliminated from the phase voltages.

The new stepped-waveform concept, which provides a wide range of modulation indexes and remains the number of eliminated harmonic components, is proposed in this section.

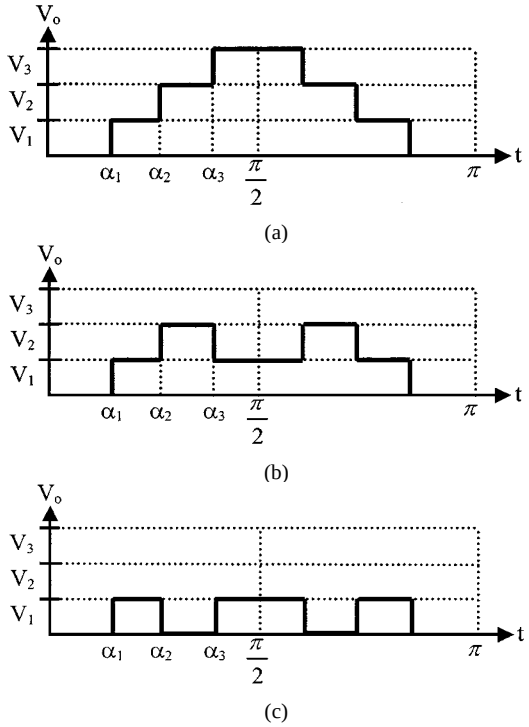

Fig. 2. Positive half cycle of a seven-level stepped waveform with different modulation indexes. (a) High modulation index. (b) Middle modulation index. (c) Low modulation index.

Fig. 2 illustrates the positive half cycle of seven-level stepped waveforms with different modulation index levels. In this case, the range of modulation indexes can be divided into three levels; i.e., high, middle, and low. An output waveform with a high modulation index level is shown in Fig. 2(a). Whenever α_3 is greater than $\pi/2$, this waveform no longer exists. Therefore, an output waveform shown in Fig. 2(b), which gives a middle range of modulation indexes, will be applied instead. The basic idea is to swap the polarity of the top level of the waveform from positive to negative, while the polarity of the other levels are not changed. When the switching angles α_1 to α_3 in Fig. 2(b) are not convergent at a low modulation index, an output waveform shown in Fig. 2(c) will replace it. In low modulation index level, the polarity of the middle level of the output waveform is swapped to negative, and the polarity of the top level is swapped to positive. In general, a stepped waveform, which comprises m switching angles, can be divided into m modulation index levels. By using this technique, wide modulation indexes, low switching frequencies and minimized harmonic distortion in output waveforms can be achieved.

IV. Optimum Harmonic Reduction With a Wide Range of Modulation Indexes in $2m + 1$-Level Waveform

A. Selective Harmonic Elimination

By using the Fourier series, the odd harmonics of the waveforms shown in Fig. 2(a)–(c) are expressed as follows:

$$h_n = \frac{4}{n\pi}[V_1\cos(n\alpha_1) + V_2\cos(n\alpha_2) + V_3\cos(n\alpha_3)] \quad (2)$$

$$h_n = \frac{4}{n\pi}[V_1\cos(n\alpha_1) + V_2\cos(n\alpha_2) - V_3\cos(n\alpha_3)] \quad (3)$$

$$h_n = \frac{4}{n\pi}[V_1\cos(n\alpha_1) - V_2\cos(n\alpha_2) + V_3\cos(n\alpha_3)]. \quad (4)$$

According to (2)–(4), α_1–α_3 must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}.$$

Because of their symmetric characteristic, no even harmonic components exist in these three waveforms. By inspecting (2)–(4) and Fig. 2, at an edge corresponding to a switching angle, the rising edge provides positive polarity for the corresponding cosine term, whereas the falling edge gives the cosine term a negative polarity.

Following this observation, the generalized amplitude of odd harmonic components in a $2m+1$ level output waveform for all modulation indexes is given as

$$h_n = \frac{4}{n\pi}[V_1 \cos(n\alpha_1) \pm V_2 \cos(n\alpha_2) \pm \cdots \pm V_m \cos(n\alpha_m)]. \quad (5)$$

Switching angles α_1–α_m must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \cdots < \alpha_m < \frac{\pi}{2}.$$

In (5), the positive sign expresses the rising edge, and the negative sign expresses the falling edge. In this paper, V_1–V_m are set to equal $V_{\rm dc}$; therefore, (5) becomes

$$h_n = \frac{4V_{\rm dc}}{n\pi}[\cos(n\alpha_1) \pm \cos(n\alpha_2) \pm \cdots \pm \cos(n\alpha_m)]. \quad (6)$$

By using systematic analysis, only the polarities and the number of levels are required to determine the switching angles for different modulation index levels in any multilevel topologies to which multilevel synchronous modulation is applied.

B. Minimum Turn-On and Turn-Off Time Considerations

To properly operate high-power semiconductor devices, minimum turn-on time, $t_{\rm on(min)}$, and minimum turn-off time, $t_{\rm off(min)}$, need to be taken into account. The gate turn-off (GTO) thyristor is used as an example. The minimum turn-on time is the minimum time that the GTO requires to establish uniform anode current conduction. To be able to turn off its rated anode current under the specified conditions, the minimum turn-on time is also necessary for the GTO. Normally, the GTO is connected to a snubber circuit for turn-off protection. During the on-state, the snubber capacitor must be discharged, so it is ready for dv/dt protection at turn-off. Therefore, another minimum on-time is required so the snubber may recover. Hence, the control logic for the GTO is generated according to these two minimum turn-on times, i.e., minimum on-time for the GTO and minimum on-time for the snubber. On the other hand, minimum turn-off time is the minimum time that the GTO requires before it may be triggered again by a positive gate current. If the device is retriggered during this time, there is a certain risk of localized turn-on, and destruction may result.

Two well-known multilevel topologies are investigated in term of how the minimum on-time and off-time affect their synthesized output waveforms. Fig. 3(a) and (b), for example, illustrate a five-level diode-clamped inverter and a five-level cascaded inverter, respectively. DC voltage sources are assumed to be well balanced in both topologies. Now,

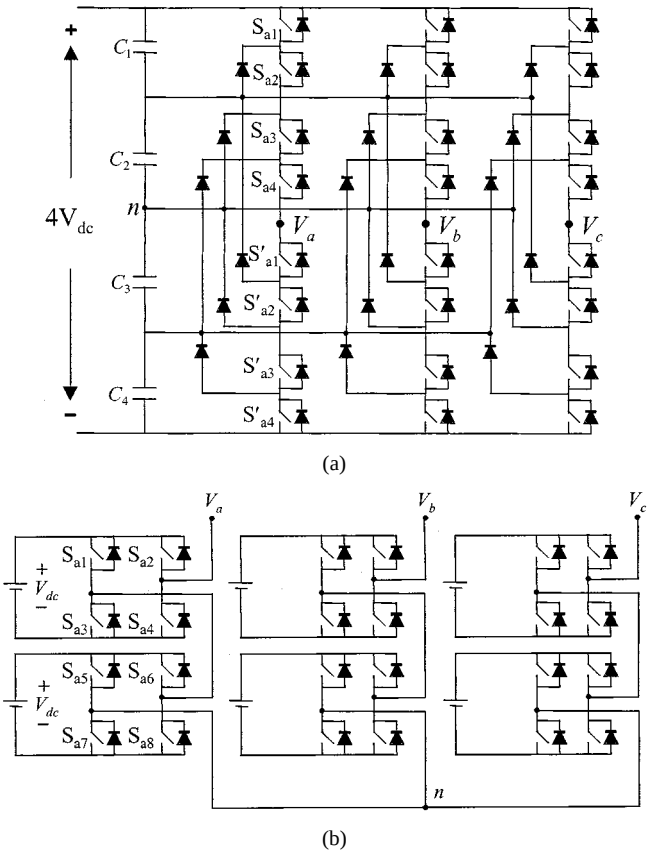

Fig. 3. (a) Five-level diode-clamped inverter. (b) Five-level cascaded inverter.

consider a five-level phase voltage, V_{an}, shown in Fig. 4(a), for a high modulation index. Fig. 4(b) shows the gate signals of the top switches, S_{a1}–S_{a4}. The other four gate signals of the bottom switch, S'_{a1}–S'_{a4}, are complementary to the signals of the top switches, S_{a1}–S_{a4}. Therefore, they are not shown here. From Fig. 4(b), gate signal, S_{a1}, follows the top-level waveform shown in Fig. 4(a), while gate signal S_{a4} follows the bottom-level waveform. Hence, pulse p must satisfy the minimum turn-on time of switch S_{a1} and satisfy the minimum turn-off time of switch S_{a4}. However, the power semiconductor devices can be controlled to avoid the undesirable pulses by coordinating of the gate signals of the other two phases. Because of its complexity, this method is not used in conjunction with the proposed technique. In the cascaded multilevel case, a possible set of four gate signals, S_{a1}–S_{a4}, of the top-level H-bridge inverter is shown in Fig. 4(c). It is obvious that the minimum turn-on and turn-off times are not required in this topology. Fig. 5 shows the five-level phase voltage, V_{an}, for a low modulation index. Clearly, the same scenario occurs here. By observation, the greatest switching angle, α_m, must take into account the minimum turn-on and turn-off time. Hence, α_m in Fig. 1 must satisfy the following condition:

$$\alpha_m < \frac{\pi}{2} - (\max(t_{\rm on(min)}, t_{\rm off(min)}) \cdot \pi \cdot f_L). \quad (7)$$

To explain the approach numerically, the 5SGF40L4502 4.5-kV/4.0-kA GTO from ABB is used as an example. According to the datasheet, the required minimum turn-on time is 100 μs. The minimum turn-off time of this GTO is also 100 μs. In this example, an assumed minimum turn-on time for snubber circuit

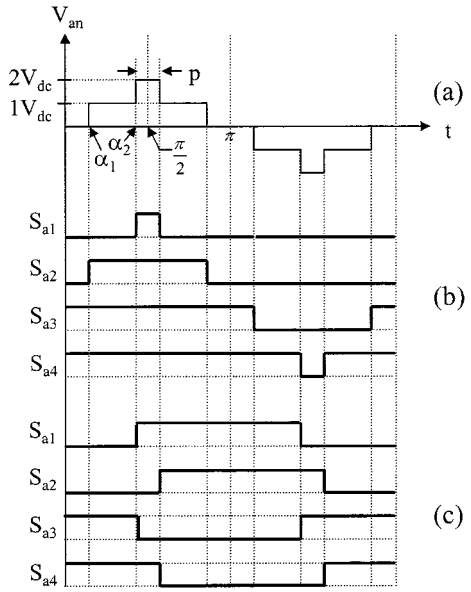

Fig. 4. (a) Five-level phase voltage waveform for high modulation index. (b) Gate signals of the top four switches of the diode-clamped inverter shown in Fig. 3(a). (c) Gate signals of the four switches of the top H-bridge inverter of the cascaded inverter shown in Fig. 3(b).

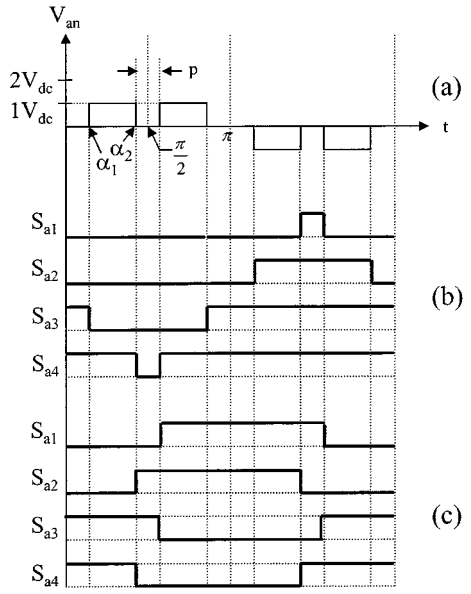

Fig. 5. (a) Five-level phase voltage waveform for low modulation index. (b)Gate signals of the top four switches of the diode-clamped inverter shown in Fig. 3(a). (c) Gate signals of the four switches of the top H-bridge inverter of the cascaded inverter shown in Fig. 3(b).

is less than 100 μs. Based on a 60-Hz system, from (7), α_m must be less than 88.92° to meet the minimum turn-on and turn-off time of the given GTO. As a result, whenever α_m is greater than 88.92°, a switching pattern for different modulation index levels will be applied.

V. Simulation Results and Experimental Results

In this paper, a seven-level cascaded inverter, which is shown in Fig. 6, is a topology chosen for study. The mod-

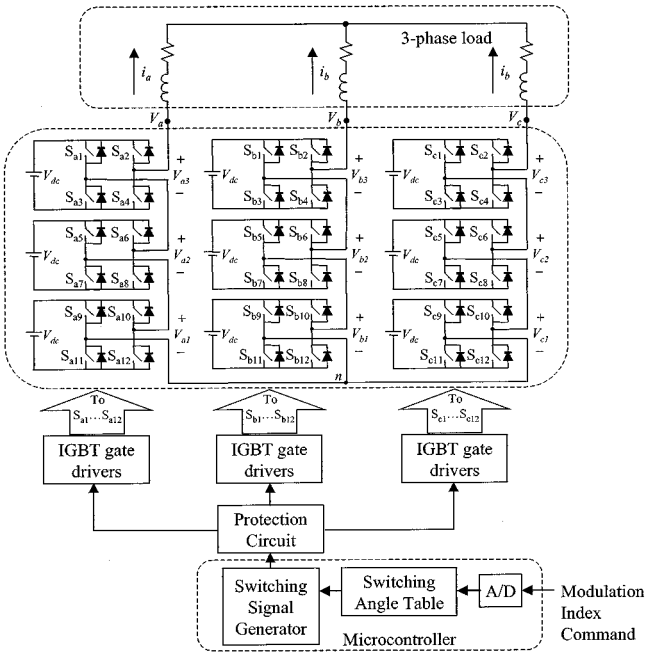

Fig. 6. Seven-level cascaded inverter system.

TABLE I
Calculated Switching Angles for Different Modulation Index Levels

Modulation Index Level	Modulation Index, M	α_1	α_2	α_3
High	1.05	12.57°	23.81°	54.33°
	1.0	11.68°	31.18°	58.58°
	0.85	22.77°	49.38°	64.57°
	0.7	38.34°	53.93°	73.96°
	0.6	39.43°	58.58°	83.10°
Middle	0.5	19.32°	66.11°	80.18°
	0.4	44.17°	74.33°	87.40°
	0.36	45.85°	79.87°	88.62°
Low	0.3	29.23°	39.24°	52.51°
	0.2	50.92°	63.36°	73.19°
	0.1	55.85°	63.43°	83.02°
	0.05	57.98°	61.86°	86.6°

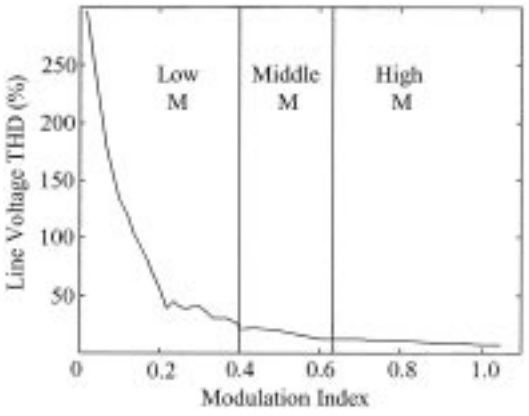

Fig. 7. Modulation index versus line-voltage THD.

ulation index for the cascaded multilevel waveform, M, is defined as follows:

$$M = \frac{h_1}{mV_{\rm dc}}. \tag{8}$$

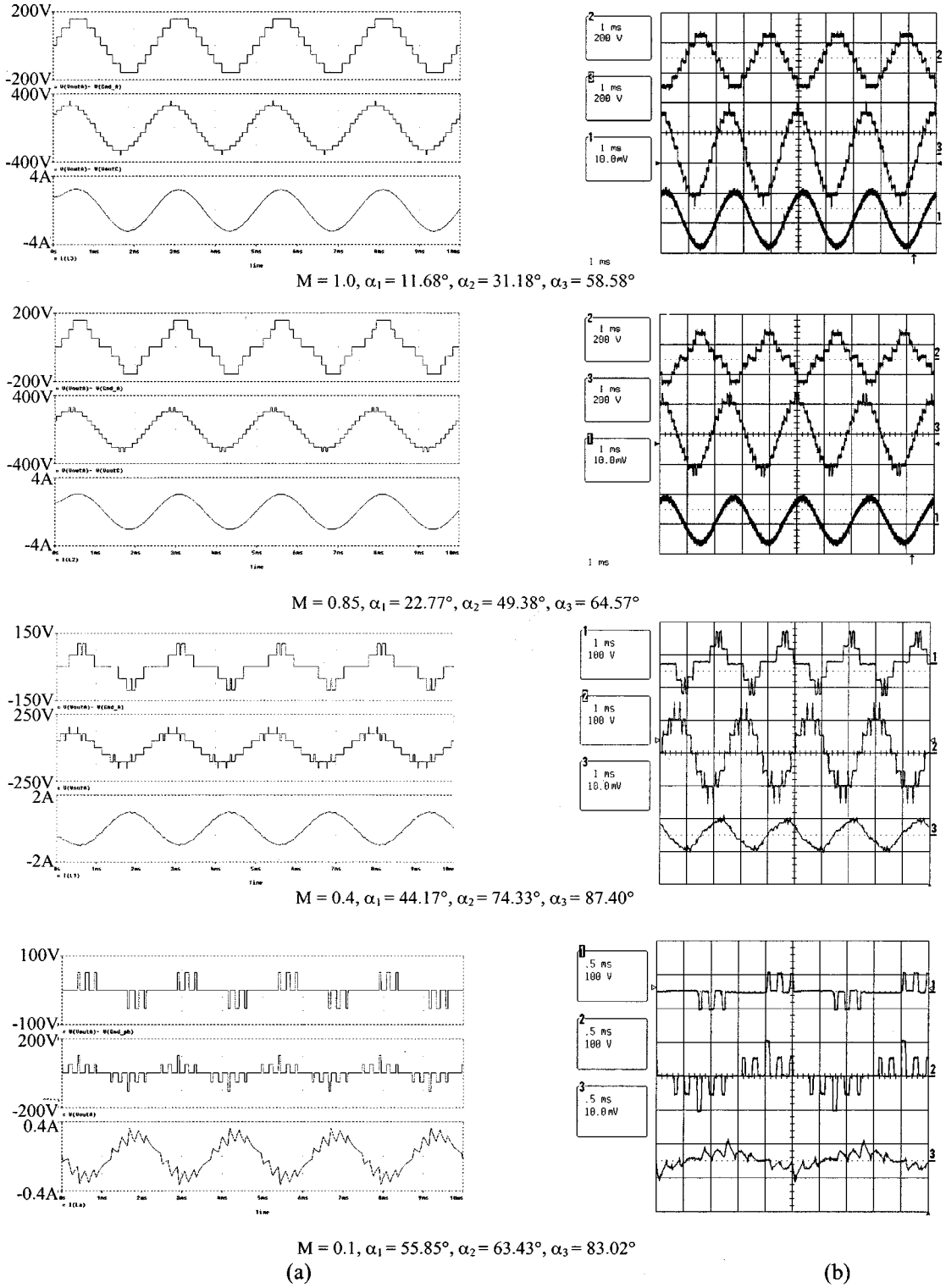

Fig. 8. Waveforms of phase voltage, line voltage, and load current. (a) Simulation results. (b) Experimental results.

A seven-level waveform for middle modulation index level is used as an example. To minimize the total line voltage harmonic distortion, the fifth and seventh harmonics need to be eliminated from the phase voltage. Thus, from (6) and (8), a set of nonlinear equations for $M = 0.4$, are given as follows:

$$[\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3)] = \frac{3(0.4)\pi}{4} \tag{9}$$

$$[\cos(5\alpha_1) + \cos(5\alpha_2) - \cos(5\alpha_3)] = 0 \tag{10}$$

$$[\cos(7\alpha_1) + \cos(7\alpha_2) - \cos(7\alpha_3)] = 0. \tag{11}$$

By using the Newton–Raphson method, the switching angles for a given modulation index can be easily obtained from (9)–(11) [6], [9]. Likewise, the switching angles for other

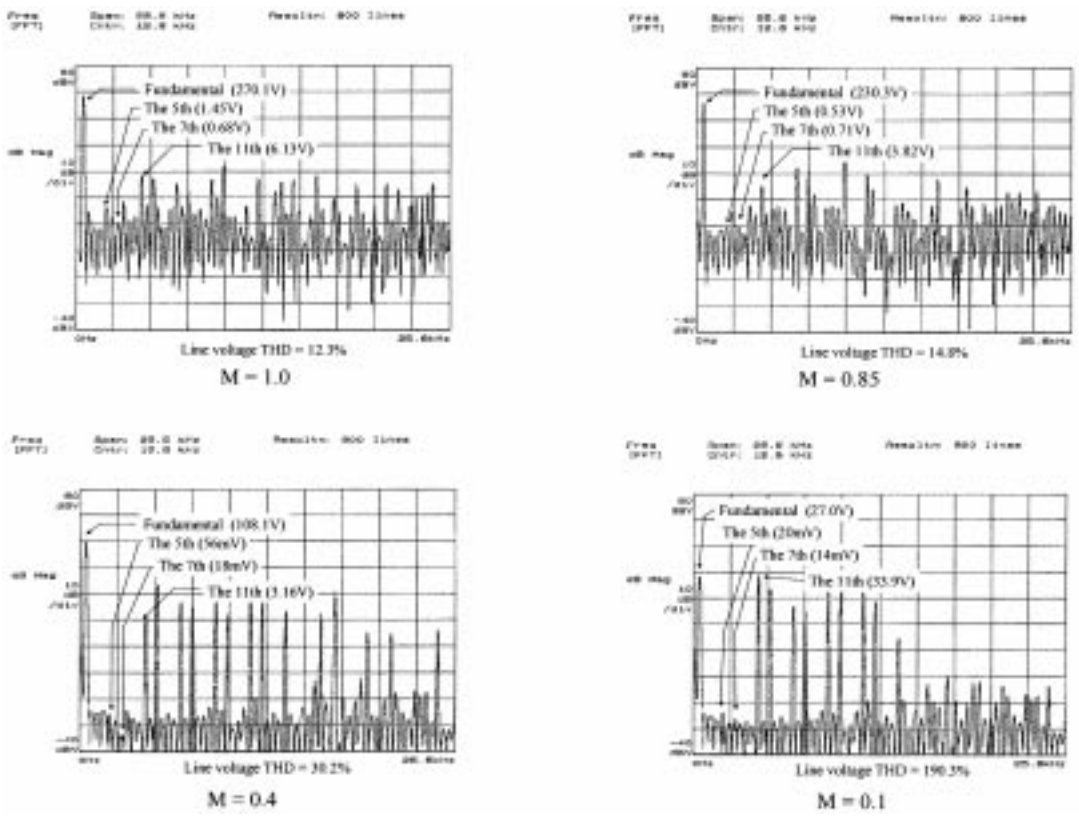

Fig. 9. Measured line-voltage spectra.

modulation indexes can be solved and are partially tabulated in Table I.

To indicate the quality of the output waveform, the total line voltage harmonic distortion is defined as follows:

$$\mathrm{THD}(\%) = \frac{\sqrt{\sum_{n=2}^{200}[h_n]^2}}{h_1} \cdot 100. \tag{12}$$

Fig. 7 shows the relationship between all modulation indexes and the calculated level of line voltage THD. It shows that the line voltage THD is inversely proportional to the modulation index. It is possible to reduce the voltage THD at a lower modulation index; however, the proposed technique needs to be extended to include more than one switching per cycle or to be applied associate with a small low-pass filter circuit.

To verify the simulation results, a seven-level voltage source converter, using cascaded inverters with separated dc sources as shown in Fig. 6, is used as a hardware prototype. In a power stage, four HGT30M60B-model insulated gate bipolar transistors (IGBTs), are used as the main switches, which are connected in full-bridge configuration. Each power stage is supplied by a variable dc source. In the control circuit, an 8-b microcontroller is employed to generate the necessary gate drive signals. A set of switching angles for entire modulation indexes is calculated offline and is stored in the program memory of the microcontroller. An analog-to-digital converter is used to convert analog modulation index command to digital domain for the controller. Fig. 8 shows simulation and experimental results of phase voltage, line voltage, and load current with modulation indexes of 1.0, 0.85, 0.4, and 0.1. The experimental line voltage spectra in decibels are also presented in Fig. 9. As expected, the results show that the fifth and the seventh harmonics of the line voltage are very small in magnitude. Because of the 120° phase shifts among phase voltages, all triplen harmonics in line voltages are also very small. The experimental results closely match the calculated and simulated results well.

Due to limited computational capability and control resolution, the experimental output quality is not as good as expected, especially at low modulation indexes. It should be noted that the number of levels is actually reduced when modulation is less than 0.5. This result agrees with the initial analysis in which the convergence failed at $M = 0.5$. At $M = 0.4$, the seven-level waveform becomes five levels, and at $M = 0.1$, it becomes three levels.

VI. Conclusion

This paper has presented a new modulation technique to be applied to multilevel voltage source converters and suitable for high-voltage high-power applications. The proposed technique can generate output stepped waveforms with wide modulation indexes and minimal THD. For all modulation index levels, the switching devices of the main power stage switch only once per cycle, which is suitable for the use with high power semiconductor devices. The simulation and experimental results validate the theoretical analysis. A three-phase seven-level cascaded inverter prototype is used as an example. The principle developed in this paper can be easily applied to other multilevel converter topologies and with any number of levels. For THD concerns, the proposed technique can be further extended to have more

than one switching per line cycle to lower THD at low modulation indexes.

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