Optimum High-k Oxide for the Best Performance of Ultra-scaled Double-Gate MOSFETs

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(Dated: January 27, 2022)

A widely used technique to mitigate the gate leakage in the ultra-scaled metal oxide semiconductor field effect transistors (MOSFETs) is the use of high-k dielectrics, which provide the same equivalent oxide thickness (EOT) as SiO_2, but thicker physical layers. However, using a thicker physical dielectric for the same EOT has a negative effect on the device performance due to the degradation of 2D electrostatics. In this letter, the effects of high-k oxides on double-gate (DG) MOSFET with the gate length under 20 nm are studied. We find that there is an optimum physical oxide thickness (T_{OX}) for each gate stack, including SiO_2 interface layer and one high-k material. For the same EOT, Al_2O_3 (k=9) over 3 Å SiO_2 provides the best performance, while for HfO_2 (k=20) and La_2O_3 (k=30), SiO_2 thicknesses should be 5 Å and 7 Å, respectively. The effects of using high-k oxides and gate stacks on the performance of ultra-scaled MOSFETs are analyzed. While thin oxide thickness increases the gate leakage, the thick oxide layer reduces the gate control on the channel. Therefore, the physical thicknesses of gate stack should be optimized to achieve the best performance.

INTRODUCTION - The scaling of transistors requires the thinning of SiO_2 gate oxide [1], which can induce significant gate tunneling below 1 nm oxide thicknesses. To mitigate the gate tunneling current in a thin oxide layer of ultra-scaled MOSFETs, high-k dielectrics are used [2, 3]. However, due to the thicker high-k gate oxides, performance drops have been observed in the ultra-scaled MOSFETs with k > 30 [4–9]. Thicker T_{OX} from larger k values worsen the short channel effects, even if the EOT is kept the same [4]. This happens due to the effect of the lateral field in the oxide, which is more pronounced in higher k materials [4, 5], and fringing capacitance due to spread of potential between the gate and the source and drain [6]. It is known that not only EOT, but also the physical oxide thickness plays important roles in SCEs. However, it is not clear what the solution is as the gate lengths of MOSFETs approach below 20 nm [1, 3, 10].

In this work, we attempt to answer these questions: 1) What is the impact of using a different high-k materials with the same EOT on an ultra-scaled DG MOSFET? 2) What is the optimum thickness of high-k gate stack for a fixed EOT? 3) How do we analytically estimate the gate leakage in the off state for a specific gate stack? We show that for ultra-scaled DG MOSFETs, there is an optimum oxide thickness that balances gate leakage of a thin oxide layer and SCEs of thick oxides. We provide an analytical model for the effect of high-k on the gate control and gate leakage current.

METHODOLOGY - A self-consistent Schrödinger-Poisson solver, based on the real-space effective-mass approximation and the wave function formalism, including direct gate and Fowler-Nordheim tunneling currents is used to simulate DG MOSFETs [11–14]. This work only considers electrons for calculations, while holes are not taken into account for the n channel devices. Neglecting holes means that band-to-band tunneling is ignored in these simulations. This effect is negligible in devices, whose source-to-drain voltage (V_{DS}) is smaller than the band gap of the channel material [15, 16]. DG device specifications are in correspondence to the ITRS table data for the 2015 node (Fig. 1). The transport direction is aligned with the <110> crystal axis and the confinement direction is (001). The source and drain regions are doped with a donor concentration ND = 10^{20}[/cm^3]. For all simulations EOT is fixed at 0.86 nm. The gate dielectric constant varies from 3.9 to 30 (Table I). Physical oxide thickness (T_{OX}) changes with the k value to keep EOT fixed, according to the following equation for the cases without any interface layer:

$$T_{OX} = EOT \times \frac{k_{OX}}{k_{SiO_2}} \tag{1}$$

However, for the gate stacks with SiO_2 interface layer and fixed EOT, $T_{OX} = T_{SiO_2} + T_{high-k}$ and T_{high-k} is calculated as:

$$T_{high-k} = (EOT - T_{SiO_2}) \times \frac{k_{high-k}}{k_{SiO_2}} \tag{2}$$

Two gate-dielectric configurations with five different oxide materials are examined in this paper. (I) All oxide materials are directly deposited on the Si channel, without any interface oxide, with the same EOT, but different k and T_{OX}. TiN metal gate contacts are characterized by work function of 4.25 eV, and their electron effective mass

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($m^* = m_0$). (II) SiO_2-high-k gate stack with TiN contacts. Effective masses are assumed isotropic (Table I). Relative dielectric constants and band gap for each material are described in Table I. Sub-threshold swing (SS), drain induced barrier lowering (DIBL) and gate tunneling current are calculated at the OFF-state, where drain off current is kept at about 100 nA/um.

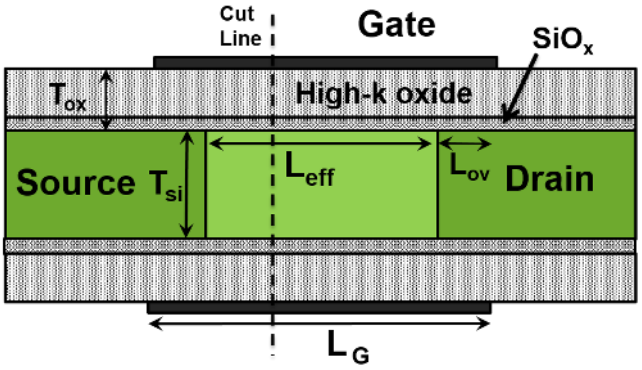

FIG. 1. Schematic view of the double-gate MOSFETs considered in this paper. The geometry parameters are the same node 2015 from ITRS tables [1]. The gate length is set to 16.7 nm. There is gate-source/drain overlap equal to 10% of the gate length (i.e. 1.6 nm). The thickness of Si channel is 5.3 nm. Currents are normalized by the channel width per side, which means simulated current divides by 2. Supply voltage (V_{DD}) is set to 0.83 V.

TABLE I. Dielectric constant k, band gap, conduction band (CB) offset to Si, and tunneling effective mass (m^*) for the oxide materials used in this work are shown. tunneling effective masses are from multiple experiments and theoretically calculated references [17, 18]. P values are calculated from equation 4 for each specific oxide material. Starred (*) numbers are used for these materials in our simulations. Physical thickness of each oxide material is shown for both configurations I and II.

Material	SiO_2	Si_3N_4	Al_2O_3	HfO_2	La_2O_3
K	3.9	7*-8	9*-10	20*-25	27-30*
Band gap [eV]	9	5.3	8.8	5.8	6
CB offset [eV]	3.5	2.4	2.8	1.5	2.3
m^*/m_0	0.4*-0.5	0.4	0.35	0.11*-0.17	0.27
P[nm^{-1}]	6.06	5.02	5.07	2.08	4.04
T_{OX}(No Interface)	0.9	1.6	2.0	4.9	6.6
T_{OX}(T_{SiO_2} = 3Å)	-	1.3	1.6	3.5	4.6
T_{OX}(T_{SiO_2} = 5Å)	-	-	1.4	2.5	3.3
T_{OX}(T_{SiO_2} = 7Å)	-	-	1.1	1.5	1.9

RESULTS AND DISCUSSION The ballistic $I_D - V_{GS}$ characteristics of DG MOSFET presented in Fig. 1 are simulated for $V_{DS} = V_{DD} = 0.83$ V. Fig. 2-A shows the results for the configuration I, without interface layer and with no gate leakage assumption. As expected, the thicker oxide would degrade the device performance by increasing the sub-threshold swing (SS) and lowering ON-current for the fixed OFF-current [6]. However, when gate tunneling is included, in the SiO_2 case, the OFF-current rises above 100 nA/um. OFF-current below 100 nA/um is considered as the OFF state in ITRS guideline [1]. For Si_3N_4, in the configuration I, ON-current is around 3430 uA/um, which is a bit less than ON-current for the device with Al_2O_3 oxide. Although, $T_{OX_{Si_3N_4}}$ is thinner than $T_{OX_{Al_2O_3}}$, it provides less ON-current for the fixed OFF-current. This is a result of high gate leakage at OFF state in Si_3N_4, which drops SS as well. $I_{Gate_{Si_3N_4}}$ is 90 times more than $I_{Gate_{Al_2O_3}}$ and contributes as 22 % of I_{OFF}. As the gate leakage cannot be controlled by gate voltage, it degrades sub-threshold swing, and consequently the ON-current.

Figs. 2-B to 2-D show the effect of using interface layer and its thickness on $I_D - V_{GS}$. Fig. 2-B depicts the transfer characteristics of a device with Al_2O_3 as the gate stack. As it is shown in Table I, T_{OX} ($T_{OX} = T_{SiO_2} + T_{Al_2O_3}$) with different interface layer thickness up to 5 Å, is still thick enough to keep the gate leakage very low. Thin high-k gate stack (4 Å Al_2O_3 on top of 7 Å SiO_2) cannot keep the leakage current low enough to turn off the device. The electrostatics and the gate leakage in the required voltage range does not vary drastically, which keep the $I_D - V_{GS}$ characteristics similar in the interested range. In Fig. 2-C high-k material is HfO_2. Reduction in the T_{OX} from 4.9 nm (no interface layer) to 1.5 nm (7 Å interface layer) impacts on SCEs. All cases can turn off the device ($I_{OFF} < 100$ nA/um) except the case with 7 Å interface layer. The case with 5 Å interface layer provides the best SS and better ON current at fixed I_{OFF} of 100 nA/um. In the case of La_2O_3 as high-k material in Fig. 2-D, T_{OX} reduces from 6.6 nm (no interface layer) to 1.9 nm (7 Å interface layer) impacts SCEs drastically. Each case turns off the device properly ($I_{OFF} < 100$ nA/um), however the case with 7 Å interface layer provides the best I_{ON} at fixed I_{OFF}, as it has the thinnest oxide.

In Figs. 3-A to 3-D, performance metrics, including I_{ON}, gate leakage current in the OFF-state, subthreshold swing (SS) and DIBL for fixed I_{OFF} of 100 nA/um are depicted. I_{ON} increases by reduction of the high-k thickness for the same EOT in the gate stack (i.e. increase in SiO_2 interface layer thickness). Optimum physical oxide thickness helps the device to turn off, as well as provides stronger electrostatics. The optimum oxide thickness for each gate stack can be achieved with a layer of SiO_2 and high-k material. Al_2O_3 gate stack shows optimum ON current at $T_{SiO_2} = 3$ Å. However, for both HfO_2 and La_2O_3 oxide materials, thicker SiO_2 interface layer improves the device I_{ON} (Fig. 3-A). In Fig. 3-B, the gate leakage current at the OFF-state is shown, which is part of the drain current. The drain current has two components; the source to drain current and the gate to drain current (gate leakage). Gate leakage results from the tunneling of electrons through the potential barrier between the gate and the channel. I_{Gate} is exponentially related to the oxide thickness ($T_{OX} = T_{SiO_2} + T_{high-k}$) and oxide effective mass [3, 16]. Al_2O_3 and HfO_2 have similar I_{Gate}. This similarity in I_{Gate} is a result of the light effective mass of HfO_2 (0.11 m_0) compared to Al_2O_3 (0.35

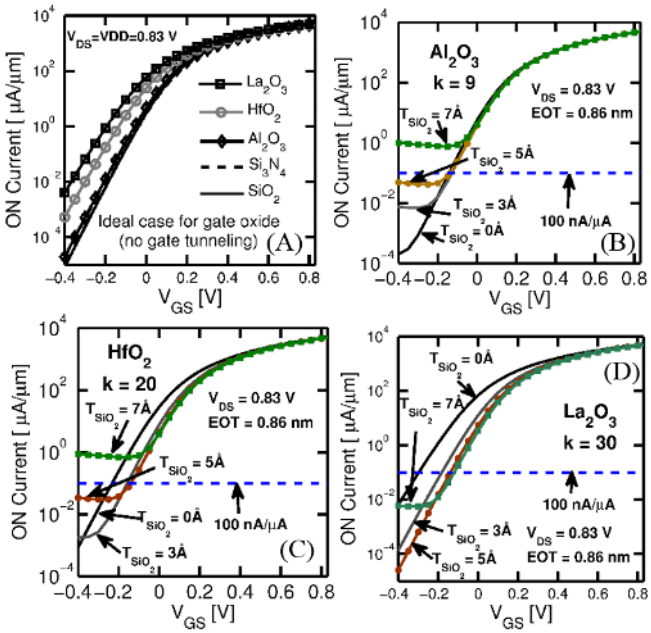

FIG. 2. Typical $I_D - V_{GS}$ transfer characteristics at V_{DS} = 0.83 V of DG MOSFETs with fixed EOT of 0.86 nm, and various dielectric materials (different k). (A) With the assumption that ideal oxides which do not have any leakage. (B) with Al_2O_3 and SiO_2. (C) with HfO_2 and SiO_2. (D) with La_2O_3 and SiO_2.

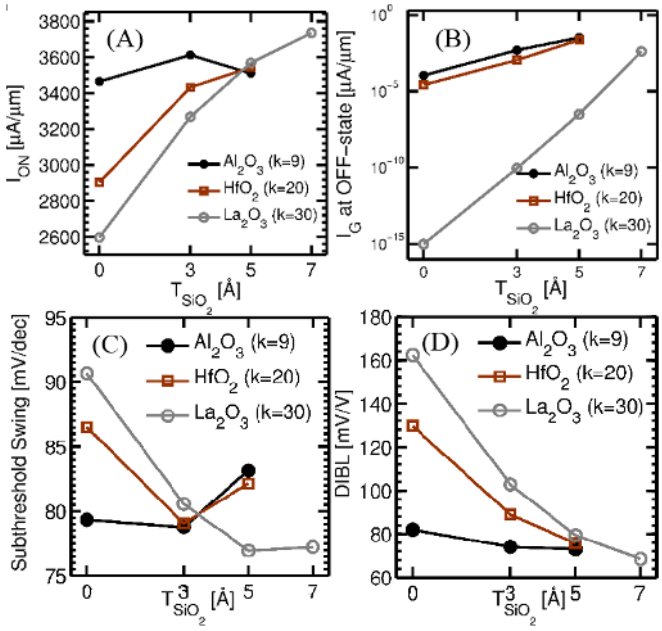

FIG. 3. Performance metrics of DG MOSFETs with fixed EOT of 0.86 nm, and various dielectric materials (different k) at fixed I_{OFF} (100 nA/um). If $I_D - V_{GS}$ could not go below 100 nA/um at off state were dropped out of these figures. (A) ON current I_{ON}, (B) Gate leakage (I_{Gate}), (C) Sub-threshold swing (SS) and (D) Drain induced barrier lowering (DIBL).

m_0), while their dielectric constants are very different. Replacing oxide materials and varying the interface layer thickness impacts SS values (Fig. 3-C). SS depends on the current at sub-threshold region, which is controlled by the electrostatics and the gate leakage [16]. Thinning T_{OX} enhances the gate control, which improves SS until I_{Gate} becomes comparable to I_{OFF}. I_{Gate} does not change exponentially with the gate bias, which leads to higher SS value. As it is depicted in Fig. 3-D DIBL improves by a reduction in the oxide thickness [6], but for very thin oxides, higher gate leakage slows down the DIBL value reduction [9]. Thin T_{OX} improves the gate control over the channel (or top of the barrier), which results in weaker drain control over the channel.

Gate leakage occurs as the carrier tunnels through the oxide layer between the gate contact and the channel. The potential barrier for a gate stack is depicted in Fig. 4-A. Using the tunneling transmission equation, we can estimate the tunneling gate leakage. In Fig. 4-B, the tunneling transmission is calculated using equation 3, which shows a strong correlation with gate leakage in Fig. 2-B. Tunneling transmission (Trans) for the gate stack is calculated as:

$$Trans \approx e^{-2(T_1.P_1+T_2.P_2+...)} \quad (3)$$

$$P = \sqrt{\frac{2m^*U}{\hbar^2}} \quad (4)$$

where T_i and P_i are thickness and decaying wave-vector of carrier in i^{th} oxide within the gate stack, accordingly. The decaying wave-vector, P_i, in each oxide layer is calculated from the effective mass, m^*, and the potential barrier height, U (the CB offset in Table I), which are listed in Table I for different high-k materials. Current is calculated as $I \approx \frac{q^2}{h}.M.Trans.dU$, where M is number of modes, q is electron charge and h is Planc constant and dU is tunneling energy window, which is equal to the potential difference between channel and gate. Except $Trans$, which is calculated from equation 3 the rest of the relation for current is fixed for all of the DG devices in this work [19].

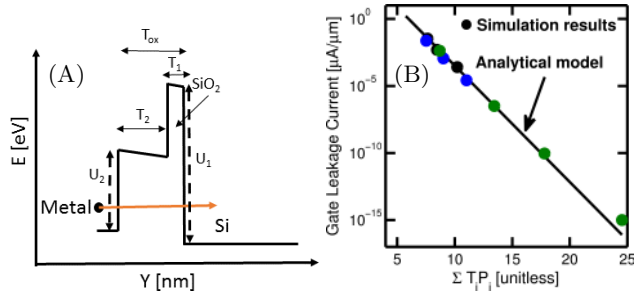

FIG. 4. (A) tunneling through the potential barrier for a 2-material gate stack. (B) Gate tunneling current calculated by the presented extensive computational model, QTBM, and the line is calculated by the analytical model from equation 3 and $I \approx \frac{q^2}{h}.M.Trans.dU$. Different colored circles are the results from rigorous simulations for different gate stacks.

In Figs. 5-A to 5-D, potential difference of OFF and ON states are shown overlapped with the electron flow in the OFF state for SiO_2 (Fig. 5-A) and different HfO_2

thicknesses over the interface layers. The potential difference between ON and OFF states shows only the effect of gate voltage variation on the potential and removes the potential difference between source and drain. Potential spread over the source and the drain are larger for thicker oxides (Figs. 5-A and 5-B). These potential spreads show the effect of increasing fringing capacitance by using thicker oxides, which degrades the device performance. By T_{OX} reduction, the potential spread reduces (Figs. 5-B to 5-E). However, in the very thin oxide case (Fig. 5-E) gate tunneling increases, which drastically reduces the device performance.

Fig. 6-A shows the capacitance network, including the fringing capacitance between the gate and the source/drain, which will be added to the gate capacitance. From the potential profile and fringing field in the Figs 5-A to 5-D, it can be observed that the potential profile broadening is proportional to the physical oxide thickness. This degrades oxide capacitance (C_{OX}). We found that the total oxide capacitance can be crudely estimated as:

$$\frac{C_{OX}}{A} \approx \frac{\epsilon_{OX}}{T_{OX}}(1 - \frac{\alpha T_{OX}}{L_G}) \tag{5}$$

where A and L_G are the gate area and the gate length, and ϵ_{OX} and α are the equivalent gate stack dielectric constant and the empirical factor to estimate C_{OX} degradation. In double gate, it is found that α to be around 0.5. Fig. 6-B shows the effect of the fringing capacitance on the total gate oxide capacitance from our simple model $\frac{\epsilon_{OX}}{T_{OX}}(1 - \frac{\alpha T_{OX}}{L_G})$ on the SS values. When SiO_2 interface layer is thin, the physical thickness and fringing capacitance are large and the fringing capacitance deteriorates the performance for thick gate stacks. This simple model can be used to *estimate* the effect of physical oxide thickness and gate length on the performance of DG MOSFETs. Here, we used our analytical model to estimate SS using the following equation [20]:

$$SS \approx ln(10)\frac{kT}{q}(1 + \frac{C_{Si}}{C_{OX}}) \tag{6}$$

where C_{Si} is the channel capacitance and C_{OX} is the modified oxide capacitance from equation 5 that takes into account fringing field effect. In Fig. 6-B, C_{Si} is extracted from the calculated SS for the DG MOSFET with only La_2O_3 as oxide. Then, SS for gate stack with different SiO_2 interface layer is estimated using equations 5 and 6. As T_{SiO_2} increases and T_{OX} decreases, the gate tunneling begins to deteriorate the performance and saturates SS, which shows there are other factors such as gate leakage, and source to drain tunneling [3] in determination of SS and equation 6 will not work well at that point.

CONCLUSION - Scaling MOSFETs below 20 nm using thicker high-k oxides drastically degrades the device performance for a fixed EOT. Therefore, introducing higher-k oxide should be examined carefully for penalty in electrostatics. Using very thin oxides also causes gate

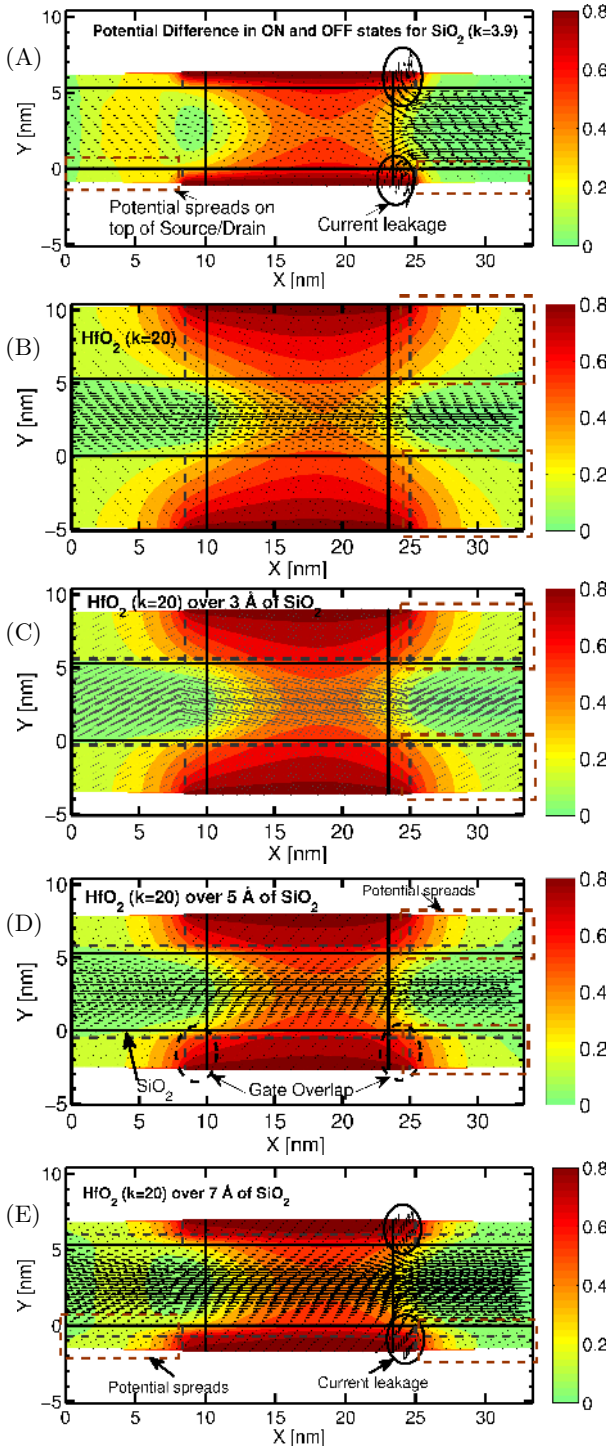

FIG. 5. The potential difference between OFF and ON states overlapped with the electron flow in the OFF-state for DG MOSFET with (A) SiO_2 oxide. (B) HfO_2 without interface layer. (C) HfO_2 over 3 Å interface layer. Potential spread over the source and the drain sections are weaker than only HfO_2 case, but stronger than SiO_2. (D) HfO_2 over 5 Å interface layer. Potential spread over the source and the drain sections are weaker than HfO_2 over 3 Å interface layer, but stronger than SiO_2. Still, gate tunneling is negligible. (E) HfO_2 over 7 Å interface layer. Gate leakage current is very strong which prevents the device from turning off.

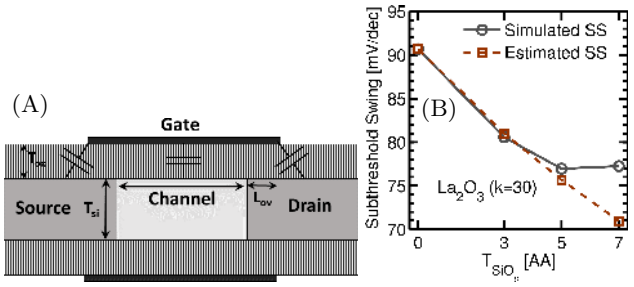

FIG. 6. (A) Capacitance network between the gate and channel, source and drain is depicted. While fringing capacitance between the gate and the source/drain increases the total oxide capacitance degrades. The potential between gate and the channel and the source/drain rather than being confined only between the gate and the channel. This degrades the device performance for thicker gate stack. (B) Electrostatics degradation factor, $1 - \frac{\alpha T_{OX}}{L_G}$, reduces by thinning the gate stack. This impact on SS for different La_2O3 gate stack is depicted as an example. Analytically calculated SS is shown over simulated ones.

leakage. An optimum combination of k value and oxide effective mass and thickness, or engineered gate stack, should be used to provide strong electrostatics and acceptable gate leakage. We provided a simple analytical model to estimate the gate leakage for each gate stack, as well as a model for the electrostatic degradation due to the fringing capacitance. Additionally, we showed there is an optimum gate stack thickness for any high-k material. Gate overlaps, source/drain doping and scattering can impact on the quantitative results. Therefore, for any specific device, it will be more accurate to do further investigation to find the optimum geometry and design for the best performance.

ACKNOWLEDGMENTS

The authors would like to thank M. Rush, Y. M. Tan, C.P. Chang, C. Cheung, J. Fonseca and S. Mehrotra. The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the US National Science Foundation under Grant Nos. EEC-0228390, EEC-1227110, EEC-0228390, EEC-0634750, OCI-0438246, OCI-0832623 and OCI-0721680 is gratefully acknowledged. This work is also part of the "Accelerating Nano-scale Transistor Innovation with NEMO5 on Blue Waters" PRAC allocation support by the National Science Foundation (award number OCI-0832623).

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