Optimum ZVS Full-Bridge DC/DC Converter with PWM Phase-Shift Control: Analysis, Design Considerations, and Experimental Results

Richard Redl
ELFI S.A.
Derrey-la-Cabuche
CH-1756 Onnens FR, Switzerland

Laszlo Balogh
Ascom Energy Systems
Murtenstrasse 133
CH-3000 Berne 5, Switzerland

David W. Edwards
Pacific Electro Dynamics
Redmond, Washington, U.S.A.
(formerly with Ascom Energy Systems)

Abstract — **By adding a simple external commutating aid circuit to the full-bridge dc/dc converter with phase-shift control and by reducing the magnetizing inductance, optimum performance (i.e. ZVS operation and high conversion efficiency) can be achieved from full load down to almost zero load. An analysis is presented to determine the required and available commutation energies. The analysis is complemented with design considerations and experimental results taken from a 3-kW converter operating at 200-kHz clock frequency.**

I. INTRODUCTION

The full-bridge converter with PWM phase-shift control [1] is potentially capable of achieving very high efficiency at high operating frequencies because it combines the advantages of hard-switching technology (small conduction losses in the semiconductor devices) and soft-switching technology (small switching losses). The circuit offers several additional benefits, too, e.g.:

- constant-frequency operation with linear control,
- essentially transparent behavior and ease of design,
- low EMI,
- integration of the stray components (junction capacitances, leakage inductance, body diodes) in the power circuit, and
- usually no need for additional passive waveshaping components (inductors and capacitors). If those components are needed, they have very small size.

The circuit also has a few drawbacks, including

- complex phase-shift controller,
- excessive ringing and overshoot across the rectifier diodes, and
- the loss of soft switching at light load.

Recently, the problem of the complex controller has been alleviated by the introduction of integrated controllers by at least two vendors. To reduce the ringing and overshoot across the rectifier diodes, a dissipative clamp [2], a low-loss active clamp [3], or a simple commutating aid circuit [4], [5] were suggested. The dissipative clamp circuit of [2] causes extra loss and reduces the efficiency. (The loss in the design reported in [2] is about 20 W and the corresponding drop in efficiency is about 2%.) The active clamp of [3] does not lead to reduced efficiency but requires an additional power transistor (and a diode if there is no intrinsic diode built into the transistor), a large capacitor, an extra control circuit for the clamp transistor, and a floating drive circuit. Also, the clamp circuits do not contribute to the extension of soft switching toward light load. The commutating aid circuit [4], [5] substantially reduces the ringing and overshoot, without introducing losses or an additional controlled power device. It comprises only a small inductor and two diodes. In addition to the beneficial effect on the voltage stress of the rectifiers, the commutating aid circuit also contributes to (1) the extension of soft switching toward light load and (2) an optimal winding configuration of the power transformer. (There is no need to build in a large leakage inductance in the transformer.) However, even with the commutating aid circuit it is impossible to achieve soft switching at very light load (e.g. in the 3% to 30% range).

The loss of soft switching at light load is considered a serious drawback and efforts have been made to avoid it (see, e.g. [6]–[7]). Reference [6] recommends two additional inductors and capacitors. Although theoretically the technique is suitable for maintaining soft switching even at zero load, the experimental results indicate that the leakage inductance causes severe overshoot and ringing across the rectifiers, leading to inferior efficiency. Reference [7] recommends using two sets of commutating aid circuit plus a capacitor in parallel with the primary of the transformer to establish a circulating current. No efficiency data are reported in [7].

In this paper we shall show that soft switching can be maintained from virtually zero to full load, by using the commutating aid circuit proposed in [4] *and* by properly selecting the other circuit inductances (the magnetizing inductance and the output filter inductance). The proposed technique does not require extra components other than the small inductor and the two diodes of the commutating aid circuit. The converter operates with soft switching over the full load current range, by optimally taking advantage of the stored inductive energies in the circuit. The converter achieves very high light-load efficiency (typically 94% at 10% load, in an experimental circuit with 53.6 V output), without significant penalty on the full-load efficiency. (The penalty on the full-load efficiency is typically 0.2%). If desirable, the efficiency of the converter can be tailored to match the load profile, so that maximum average efficiency is obtained. In addition to the improvement in light-load efficiency, the voltage overshoot across the output rectifier diodes also becomes well controlled due to the commutating aid circuit.

In Section II of this paper a detailed analysis of the switch transitions of the converter is presented, using equivalent circuits for each phase of the operation. Section III discusses the required and available commutation energies of the clocked (or *passive-to-active*, *P-A*) leg of the converter. (Note that the available commutation energy for the modulated, or *active-to-passive* (*A-P*), leg is not limited, and the *A-P* leg never loses soft switching if the dead time between the turn-off of a switch and the turn-on of the other switch is long enough.) Section IV presents a loss analysis, experimental data taken from a 3-kW converter operating at 200-kHz clock frequency, and design considerations.

II. ANALYSIS OF SWITCH TRANSITIONS

A. Topology

Figure 1 shows the topology of the optimum ZVS full-bridge converter. There are two differences between the topology of Figure 1 and the topology discussed in [4]. Those differences are: 1. The magnetizing inductance L_m is now a carefully designed relatively small value. (In [4], the effect of the magnetizing inductance on the transition of the *P-A* leg was not considered.) 2. The commutating aid circuit comprising D_1, D_2, and L_c is now at

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the *A-P* leg. (As was shown in [8], the currents in the clamp diodes are reduced if the commutating aid circuit is at the *A-P* leg. In [4], the difference between the two locations was not considered; the test results presented in [4] were taken with the commutating aid circuit located at the *P-A* leg.)

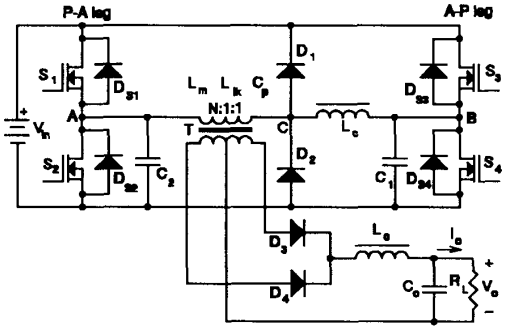


Figure 1. Optimum ZVS full-bridge PWM phase-shift dc/dc converter.

B. Waveforms and Operating States

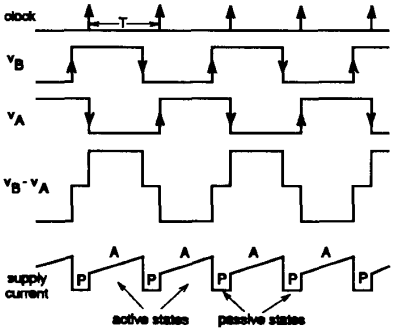


Figure 2. Waveforms and operating states.

Figure 2 shows the basic waveforms and operating states. The converter has two pairs of principal operating states, determined by the two pairs of allowed combinations of the switch states. In the first pair of states the two diagonally placed switches (S_1 and S_4 or S_2 and S_3) are conducting. Energy is absorbed from the input voltage source during these states, therefore the states are called *active*. When two switches on the same side of the power bus are conducting (i.e. either S_1 and S_3 or S_2 and S_4), there is no energy absorption. Those states are called *passive*. As can be seen, the *clocked* leg of the converter (in our case the leg with the center point marked A) switches only from the passive state to the active state. For that reason, the clocked leg is also called the *passive-to-active* (or *P-A*) leg. The *modulated* leg (with the center point marked B) always switches from the active state to the passive state and is also called *active-to-passive* (or *A-P*) leg. As has been shown in several studies, there is a significant difference between the switch transitions of the two legs.

C. Switching from Active State to Passive State (A-P Transition)

Figure 3 shows the equivalent circuit of the converter when it switches from the active state (in this case the one defined by the conduction of S_2 and S_3), to the passive state (defined by the conduction of S_2 and S_4). In the equivalent circuit the transformer is represented by the magnetizing inductance L_m , the leakage inductance L_{lk} , and an equivalent parasitic capacitance C_p (transformed to the primary side). C_1 is the sum of the equivalent capacitances of the switches S_3 and S_4 and the external stray and snubber capacitances loading the leg center point B. (Note: The equivalent capacitance of a MOSFET switch is the linear capacitance which stores the same amount of energy as does the nonlinear output capacitance when the voltage across it is V_{in}.) The diode drawn with dashed line represents the fact that current cannot be reversed in the output inductor. The voltages across the capacitances and the currents in the inductances are the initial conditions of the transition. I_m is the peak value of the magnetizing current, I_p' is the peak value of the current in the output inductor transformed to the input side, V_o' is the output voltage transformed to the input side. The equivalent circuit is valid down to zero load.

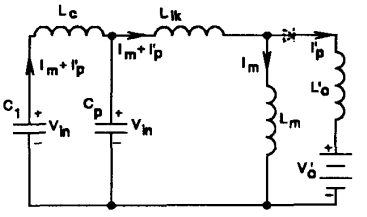


Figure 3. Equivalent circuit during the *A-P* transition

Assuming that the magnetizing and the reflected output inductances are much larger than the leakage and commutating inductances, the equivalent circuit can be simplified to that in Figure 4.

If the current in the output inductor is relatively high, the equivalent circuit of Figure 4 yields a linear leg voltage vs. time function. At zero load current the equivalent circuit in Figure 5a and the leg voltage function of Figure 5b are valid.

The *A-P* transition is completed when either the anti-parallel diode of the other switch in the leg (the body diode of the MOSFET switch or an external diode) comes into conduction, or the other switch is turned on, whichever happens earlier.

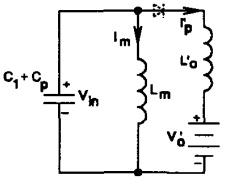


Figure 4. Simplified equivalent circuit during the *A-P* transition

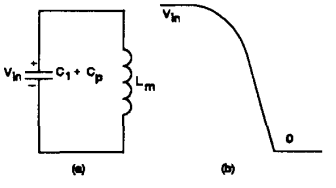


Figure 5. Simplified equivalent circuit during the *A-P* transition (a) and leg voltage vs. time (b) at zero load current.

A delay time must be inserted between the turn-off of the first switch and the turn-on of the second switch. In order to avoid lossy

charge or discharge of the capacitance loading the junction of the two switches, the delay time must be above a certain limit [4]. The theoretical upper limit for the delay time is the minimum duration of the passive state. Note that with a large magnetizing inductance it might not be possible to select a delay time which would ensure soft switching at light load. If, however, the magnetizing inductance is reduced for another reason (namely to help the soft switching of the *P-A* leg), selecting a large-enough delay time might become possible.

D. Switching from Passive State to Active State (P-A Transition)

Depending on the operating mode (continuous or discontinuous current in the filter inductor) and circuit parameters, the following four cases are possible during the *P-A* transition:

1 The converter is in discontinuous mode. The transformer is not shorted through the rectifier diodes.
2. The converter is in continuous mode and the magnetizing current in the transformer is larger than the reflected inductor valley current. The transition is over before the current in the primary drops below the difference of the magnetizing current and the reflected inductor valley current. The transformer remains shorted during the transition by the simultaneously conducting rectifier diodes D_3 and D_4.
3. The converter is in continuous mode and the magnetizing current in the transformer is larger than the reflected inductor valley current. The current in the primary drops below the difference of the magnetizing current and the reflected inductor valley current during the transition. At that moment the transformer comes out of the shorted state.
4. The converter is in continuous mode and the magnetizing current in the transformer is smaller than the reflected inductor valley current. The transformer remains shorted during the duration of the transition.

1) *Discontinuous inductor-current mode (DICM):* Figure 6 shows the equivalent circuit during the passive-to-active transition in DICM.

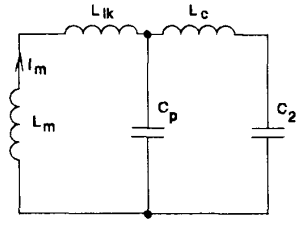


Figure 6. Equivalent circuit during the *P-A* transition, DICM.

Figure 7a shows a simplified equivalent circuit (again using the assumption that the leakage and commutating inductances are much smaller than the magnetizing inductance). Figure 7b shows the leg voltage waveform. As can be inferred from the waveform, an optimal delay time exists which minimizes the capacitor discharge losses when the leg voltage cannot swing all the way to the other bus. That delay time is independent from the magnetizing current or the input voltage.

2) *Continuous inductor-current mode (CICM):* Figure 8 shows the equivalent circuit at the beginning of the passive-to-active transition in CICM. The transformer is shorted. The equivalent circuit remains valid during the duration of the transition if the magnetizing current is smaller than the reflected inductor valley current or if the leg voltage swings to the other bus before the primary current drops below the difference of the magnetizing current and the reflected inductor valley current. (When that happens the transformer comes out of the shorted state and the equivalent circuit of Figure 8 will not be valid anymore.)

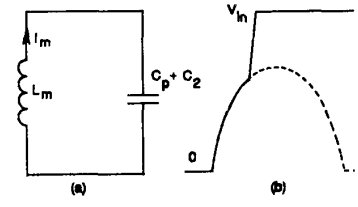


Figure 7. Simplified equivalent circuit during the *P-A* transition in DICM (a), and leg voltage vs. time (b).

In the circuit of Figure 8 the presence of the parasitic capacitance of the transformer and similar magnitudes of the leakage inductance L_{lk} and commutating inductance L_c make difficult the introduction of a simplified equivalent circuit. If we replace the circuit of Figure 8 with that of Figure 9a, the result is somewhat pessimistic because in the actual converter the voltage across C_p does not need to swing all the way to the other bus during the transition. If the commutating inductance is significantly larger than the leakage inductance the voltage change across C_p can be neglected and the component values in parentheses give a reasonably good approximation.

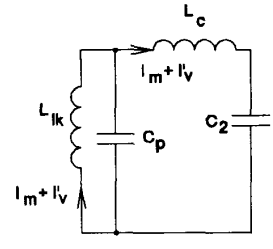


Figure 8. Equivalent circuit at the beginning of the *P-A* transition in CICM.

The leg voltage waveform in Figure 9b shows the case when the available stored energy is not sufficient for providing a full swing and the other switch is turned on slightly later than the optimum.

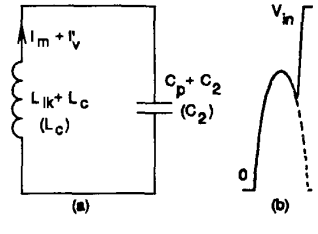


Figure 9. Simplified equivalent circuit during the *P-A* transition in CICM when the transformer is shorted (a), and leg voltage vs. time (b).

If the magnetizing current is larger than the reflected valley current and if during the transition the current in the commutating induc-

tance drops below the difference between the magnetizing current and the reflected valley current, the transformer comes out from the shorted state. Then the equivalent circuit of Figure 10 becomes valid. Here we assumed that the voltage across the parasitic capacitance does not change during the first part of the transition (i.e. the leakage inductance is much smaller than the commutating inductance).

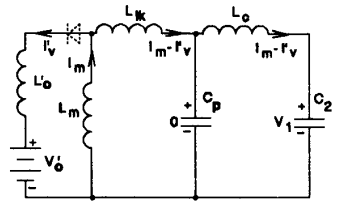


Figure 10. Equivalent circuit during the *P-A* transition in CICM when the transformer comes out from the shorted condition.

The initial capacitor voltage V_1 can be calculated from the law of conservation of energy. The result is

$$V_1 = 2\sqrt{\frac{L_c}{C_2} I_m I_v'} \tag{1}$$

III. COMMUTATION ENERGIES OF THE *P-A* LEG

The voltage of the capacitance loading the *P-A* leg changes by the amount of V_{in} at each *P-A* transition. The voltage change represents a change of energy. That energy is the *required commutation energy*. Due to the currents flowing in them, the circuit inductances store energy. Some of that energy can be used for changing the voltage of the loading capacitance of the *P-A* leg. That energy is the *available commutation energy*. The *P-A* leg operates with soft switching if the following two conditions are met simultaneously: 1. The available commutation energy is larger than the required commutation energy. 2. The switch turn-on delay is within the limits determined by the circuit parameters. (The turn-on delay was discussed in detail in [4].)

A. Required Commutation Energy

The required commutation energy depends on the nature of the transition. If the parasitic capacitance of the transformer changes voltage during the transition (as, e.g. in DICM or in CICM when the magnetizing current is larger than the reflected valley current *and* the voltage V_1 is smaller than V_{in}), the required commutation energy is

$$E_{c(req)} = \frac{1}{2}(C_p + C_2)V_{in}^2 \tag{2}$$

If the parasitic capacitance of the transformer does not change voltage during the transition (as, e.g. in CICM when the magnetizing current is smaller than the reflected valley current, or the magnetizing current is larger than the reflected valley current *and* the voltage V_1 is larger than V_{in}), the required commutation energy is

$$E_{c(req)} = \frac{1}{2}C_2 V_{in}^2 \tag{3}$$

B. Available Commutation Energy

The available commutation energy can be obtained from the equivalent circuits of Figures 6, 8, and 10. From the equivalent circuit of Figure 6, in DICM the available commutation energy is

$$E_{c(avail)} = \frac{1}{2}(L_m + L_{lk} + L_c)I_m^2 \tag{4}$$

From the equivalent circuits of Figures 8 and 10, in CICM, when the magnetizing current is larger than the reflected valley current, the commutation energy is

$$E_{c(avail)} = \frac{1}{2}L_m(I_m - I_v')^2 + \frac{1}{2}(L_{lk} + L_c)(I_m + I_v')^2 \tag{5}$$

From the equivalent circuit of Figure 8, in CICM, when the magnetizing current is smaller than the reflected valley current, the available commutation energy is

$$E_{c(avail)} = \frac{1}{2}(L_{lk} + L_c)(I_m + I_v')^2 \tag{6}$$

In (4) (DICM), the magnetizing current I_m is

$$I_m = \frac{1}{2L_m}\sqrt{\frac{2I_o L_o N V_o V_{in} T}{\left(\frac{V_{in}}{N} - V_o\right)}} \tag{7}$$

In (5) and (6) (CICM), the magnetizing current is

$$I_m = \frac{V_o N T}{2L_m} \tag{8}$$

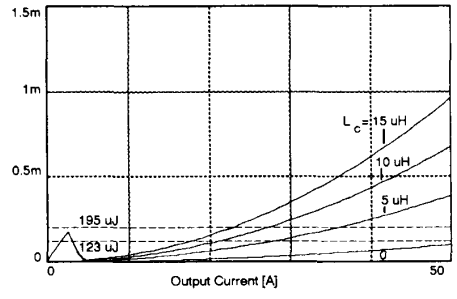
and the reflected valley current is

$$I_v' = \frac{I_o}{N} - \frac{V_o T}{2L_o N}\left(1 - \frac{V_o}{V_{in}}N\right) \tag{9}$$

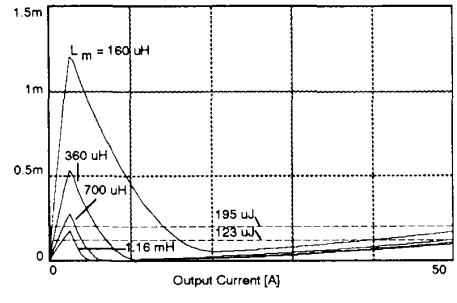
(Note: For simplicity, in the expressions for the magnetizing current and the reflected valley current we neglected the effect of the voltage drop of across the commutating inductance. That voltage drop can be significant at small magnetizing and filter inductances, requiring a noticeable increase in the control duty ratio. The voltage drop has, however, only small influence on the available commutation energy.)

It is interesting to plot the commutation energy in function of the load current. Figures 11a, 11b, and 11c show the available commutation energy of a 3-kW converter with various combinations of magnetizing and commutation inductances vs. load current. Figure 11a gives the commutation energy for the case when the magnetizing inductance is large (1.16 mH) and the commutating inductance is varied from zero to 15 μH. Figure 11b gives the commutation energy for the case when the magnetizing inductance is varied from 160 μH to 1.16 mH, and the commutating inductance is zero. Figure 11c gives the commutation energy for the case when the magnetizing inductance is varied from 160 μH to 1.16 mH, and the

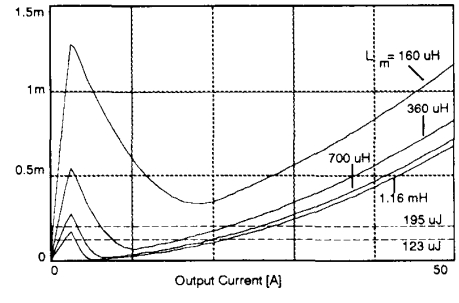
commutating inductance is 10 μH. (For all three figures, the input voltage is 380 V, the output voltage is 53.6 V, the clock frequency is 200 kHz, the transformer turns ratio is 14/3/3, the output filter inductance is 17 μH, and the transformer leakage inductance is 1.5 μH. In all three figures, we also indicated by dashed horizontal lines the required maximum and minimum commutation energies for the transformer parasitic capacitance of C_p = 1 nF and leg capacitance of C_2 = 1.7 nF. The maximum energy is 195 μJ and the minimum energy is 123 μJ .)



(a)



(b)



(c)

Figure 11. Available and required commutation energies vs. output current; (a) L_m = 1.16 mH, (b) L_c = 0, (c) L_c = 10 μH.

As can be seen from Figure 11c, the combination of a 160-μH magnetizing inductance and a 10-μH commutating inductance yields an available commutation energy which is above even the maximum value of energy required for soft switching virtually over the full load-current range (from less than 1 A to 50 A, i.e. 2% to 100%). Note that if a 10-μH commutating inductor is used and the magnetizing inductance is large (1.16 mH), soft switching is lost *below* about 22 A, i.e. 44% of full load (Figure 11a, minimum energy line). If a 160-μH magnetizing inductance is used and no commutating inductor is added, soft switching is lost *above* about 14 A, i.e. 28% of full load (Figure 12b, maximum energy line). In that case, soft switching is reestablished above about 40 A (minimum energy line).

IV. LOSS ANALYSIS, EXPERIMENTAL DATA, AND DESIGN CONSIDERATIONS

A. Loss Analysis

A benefit of the reduced magnetizing inductance is the extension of soft switching toward *smaller* load currents and a corresponding increase in the light-load efficiency. A disadvantage is, however, that the reduced magnetizing inductance increases the conduction losses and reduces the efficiency at *larger* load currents. For a fair evaluation of the effect of the magnetizing inductance, the total loss of the converter must be determined in function of the load current at various magnetizing inductances. As we shall see, the increase in the conduction loss at large load currents is negligible compared to the decrease in switching loss at small load currents.

Equation (10) gives the total loss.

$$P_{tot} = P_{Q(cond)} + P_{Q(off)} + P_{Q(on)} + P_{D(cond)} + P_{D(sw)} + P_{Tr(core)} + P_{Tr(w)} + P_{L(core)} + P_{L(w)} + P_{R(aux)} \quad (10)$$

The total loss has the following major components: transistor conduction loss, transistor turn-off loss, transistor turn-on loss, rectifier diode conduction and switching losses, transformer core and winding losses, filter inductor core and winding losses, and auxiliary resistive losses. The transistor conduction loss is

$$P_{Q(cond)} = 2R_{DS(on)}I^2_{pr(rms)} \quad (11)$$

where $R_{DS(on)}$ is the on resistance of the MOSFET, and $I_{pr(rms)}$ is the rms current flowing in the primary winding of the transformer. In CICM and at large filter inductance the primary rms current can be approximated as

$$I_{pr(rms)} = \sqrt{I_m^2(1 - \frac{2}{3}D) + I_o^2\frac{D}{N^2}} \quad (12)$$

where D is the duty ratio of the active state. The total transistor turn-off loss is

$$P_{Q(off)} = \frac{N}{12T}\left(I_m + \frac{I_p}{N}\right)^2 t_{off}^2 C_1 + \frac{N}{12T}\left(I_m + \frac{I_v}{N}\right)^2 t_{off}^2 C_2 \quad (13)$$

where t_{off} is the current fall time of the MOSFET switches. Calculating the transistor turn-on loss is more complicated than calculating the turn-off loss because several operating states are possible and the presence or absence of those operating states depends on the available commutation energies and switch delay times. Also, the losses are different for the *A-P* and *P-A* legs. The starting point is to determine the voltages V_{C1} and V_{C2} across the capacitances C_1 and C_2 at the instants the switches are turned on. The turn-on loss is

$$P_{Q(on)} = \frac{1}{2T}\left[C_1(V_{C1} - V_{in})^2 + C_2(V_{C2} - V_{in})^2\right] \quad (14)$$

The conduction loss of the rectifier diodes is

$$P_{D(cond)} = V_F I_o + R_D I_o^2 \quad (15)$$

where V_F is the diode offset voltage and R_D is the diode resistance. The switching loss of the rectifier diodes is

$$P_{D(sw)} = R_{eq} I_o^2 \quad (16)$$

where R_{eq} simply represents the empirical dependence of the switching loss on the output current. The transformer core loss is

$$P_{Tr(core)} = \left(\frac{V_{in} DT}{2N_{pr} A_{e(Tr)}}\right)^2 V_{Tr} P_{W/V} \quad (17)$$

where N_{pr} is the number of primary turns, $A_{e(Tr)}$ is the cross section area, V_{Tr} is the core volume, and $P_{W/V}$ is the specific core loss (loss per unit volume). The transformer winding loss is

$$P_{Tr(w)} = R_{ac(pr)}\left[I_m^2(1 - \frac{2}{3}D) + I_o^2 \frac{D}{N^2}\right] + \left[R_{dc(sec)} + R_{ac(sec)}\right]\frac{I_o^2}{2} \quad (18)$$

where $R_{ac(pr)}$, $R_{dc(sec)}$, and $R_{ac(sec)}$ are the ac and dc resistances of the primary and secondary windings. The inductor core loss is

$$P_{L(core)} = \left[\left(\frac{V_{in}}{N} - V_o\right)\frac{DT}{2N_L A_{e(L)}}\right]^2 V_L P_{W/V} \quad (19)$$

where N_L is the number of turns, $A_{e(L)}$ is the cross section area, V_L is the core volume, and $P_{W/V}$ is the specific core loss (loss per unit volume). The inductor winding loss is

$$P_{L(w)} = R_L I_o^2 \quad (20)$$

where R_L is the dc resistance of the inductor winding. The auxiliary resistive losses (PCB, connector, circuit breaker, etc) are given by

$$P_{R(aux)} = R_{aux} I_o^2 \quad (21)$$

A spreadsheet was developed for calculating the losses and the efficiency of the converter. The results are presented in the next section together with the measured data.

B. Experimental Data

We carried out efficiency measurements on a 3-kW converter operating at 200-kHz clock frequency. The parameters of the converter are given in Section III.B. Figure 12 shows the measured and calculated efficiencies with three magnetizing inductances, 1.16 mH, 360 μH, and 160 μH.

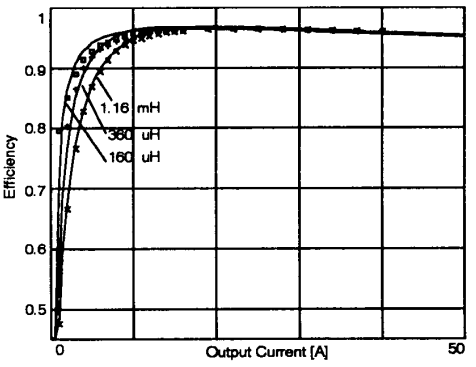


Figure 12. Measured and calculated efficiencies vs. output current.

As can be seen, there is good agreement between the measured and calculated efficiencies. It is also clearly visible that the reduction of the magnetizing inductance significantly improves the light-load efficiency. With the large magnetizing inductance, the efficiency drops to about 82% at 4 A load; with 160 μH, the efficiency is still about 92% at 4 A, and is about 80% at 1 A, which is only 2% of the full load. It is notable that the reduced magnetizing inductance has very little effect on the efficiency above 12A — for all three cases the efficiencies stay above 95% from 12 A to 50 A, with peaks between 96.5% and 96.8%. The peaks are around 50% of full load.

The improvement is even better observable on the loss vs. output current function, in Figure 13. That figure shows the measured and calculated losses in the converter with 1.16 mH and with 160 μH magnetizing inductances, in the zero to 20-A range.

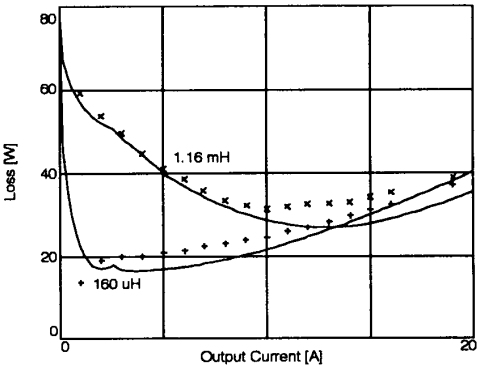


Figure 13. Loss vs. output current.

As can be seen, between 1 A and 5 A output currents the loss of the converter with the 160 μH magnetizing inductance is much less than that with 1.16 mH (by about 20 to 40 W).

Figures 14a, 14b, 14c, and 14d show the effects of the magnetizing and commutating inductances on the transition of the *P-A* leg. Figure 14a shows the waveform at 15 A output current in the case where the commutating inductance is 10 μH, and the magnetizing inductance is 1.16 mH. Figure 14b shows the waveform at 25 A output current in the case where the commutating inductance is zero, and the magnetizing inductance is 160 μH. In both cases, soft switching is lost. Figures 14c and 14d show the waveforms at 4 A and 25 A output current in the case where the commutating inductance is 10 μH, and the magnetizing inductance is 160 μH. As can be seen, the converter operates with soft switching at both output current values.

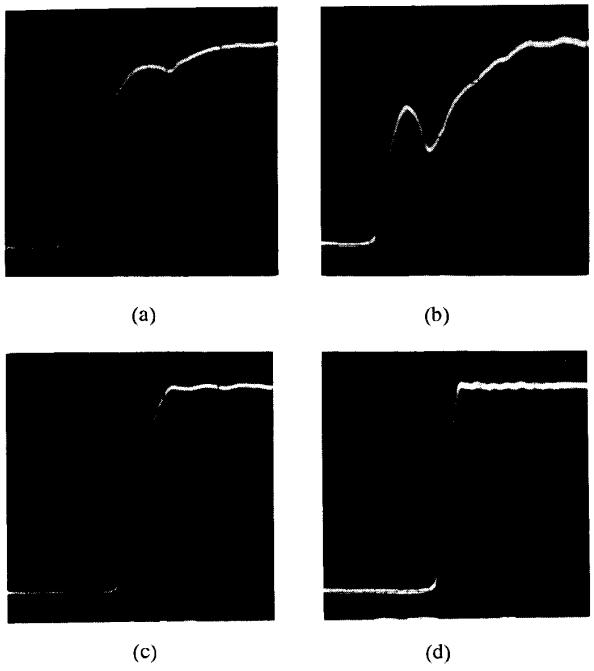


Figure 14. Transitions of the *P-A* leg: (a) 10 μH commutating inductance, 1.16 mH magmetizing inductance, 15 A output current; (b) zero commutating inductance, 160 μH magnetizing inductance, 25 A output current; (c) 10 μH commutating inductance, 160 μH magnetizing inductance, 4 A output current; (d) 10 μH commutating inductance, 160 μH magnetizing inductance, 25 A output current. Scales: 100 ns/div., 100 V/div.

C. Design Considerations

As was demonstrated above, by reducing the magnetizing inductance, the loss of soft switching can be avoided. If the magnetizing inductance is selected such that the minimum of the available commutating energy in CICM is above the maximum required commutating energy, soft switching will be lost only at a very small output current (typically less than 5% of full load). The minimum available energy in CICM is where the magnetizing current and the reflected valley current are equal. From the equality of those currents, as well as from (2), (5) or (6), (7) and (8), the maximum allowed magnetizing inductance can be calculated as

$$L_m = \frac{NV_oT}{V_{in}}\sqrt{\frac{L_{lk}+L_c}{C_p+C_2}} \qquad (22)$$

From (22), in the experimental circuit the magnetizing inductance must stay below 215 μH to ensure soft switching.

Soft switching is inevitably lost at very light load. The limit output current below which soft switching is lost can be calculated from (2), (4) and (7). For the experimental circuit with 160 μH magnetizing inductance, the calculation yields 430 mA, in good agreement with the observed value of about 0.5 A (1% of full load). A possible solution to extend the range of soft switching further downward is to use a swinging output inductor and a small preload. In the experimental circuit, if the inductance of the output inductor increases to 170 μH (a tenfold increase) below 0.5 A output current, a 43-mA preload will ensure soft switching down to zero. That preload is less than 0.1% of the full load.

Note that in many practical applications the efficiency drop caused by the loss of soft switching at light load is not as important as the increased EMI and noise. In those cases it might be easier to control the EMI or noise by slowing down the turn-on of the MOSFET switches than by reducing the magnetizing inductance. Using a 15-ohm series gate resistor in the experimental circuit with die-size 107 MOSFETs we achieved a *dV/dt* of approximately 600 V/μs at hard switching. That value was lower than the maximum *dV/dt* under soft-switching conditions.

SUMMARY

By adding a simple external commutating aid circuit to the full-bridge dc/dc converter with phase-shift control and by reducing the magnetizing inductance, we achieved soft switching from full load down to 1% load. The efficiency was 92% at 8% load, and stayed above 95% from 15% load to full load. Analyses and design considerations were presented to determine the required and available commutation energies, the converter losses, and the optimal magnetizing inductance. Experimental data taken from a 3-kW converter with 200-kHz clock frequency verified the theoretical results.

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