Organic Electronics on Banknotes

Ute Zschieschang, Tatsuya Yamamoto, Kazuo Takimiya, Hirokazu Kuwabara, Masaaki Ikeda, Tsuyoshi Sekitani, Takao Someya, and Hagen Klauk*

Modern banknotes include up to 50 different anti-counterfeiting features, such as watermarks, holograms, raised printing, embedded foil strips, fluorescent inks, and many others. To supplement these passive security features, active electronic anti-counterfeiting and tracking features in the form of silicon integrated circuits have been considered,[1] but have thus far not been realized, mainly because of the significant thickness of standard silicon wafers (>500 μm). The thickness of silicon chips can be reduced to about 20 μm,[2,3] but this may still be too thick for incorporation into banknotes. Other techniques allow thin silicon membranes to be transferred from a wafer onto plastic substrates and be processed into flexible circuits.[4,5] Although it may be possible to transfer silicon membranes onto banknotes as well, the harsh process conditions during circuit fabrication following the transfer of the membranes may irreversibly damage the banknotes.

In contrast, organic thin-film transistors (TFTs) are readily fabricated on a variety of surfaces, including foils,[6–10] fibers,[11,12] and paper.[13–15] The ability to fabricate organic circuits on banknotes may create the possibility of outfitting banknotes with active electronic security features, provided the device fabrication process does not damage the banknotes and provided the operating voltage and power consumption of the circuits is sufficiently low to allow power being supplied by radio-frequency coupling with low magnetic fields.[16]

The key to realizing low-voltage organic TFTs on delicate substrates, such as banknotes, is the use of a high-capacitance gate dielectric prepared under mild thermal and chemical conditions. A promising option are hybrid dielectrics composed of a thin aluminum oxide layer and an alkylphosphonic acid self-assembled monolayer (SAM).[17–19] The aluminum oxide layer is produced by briefly exposing the surface of the aluminum gate electrodes (bottom-gate structure) to an oxygen plasma, which increases the native AlO_x thickness to about 3 to 4 nm, depending on the plasma power. The organic monolayer is then allowed to self-assemble on the AlO_x surface by immersing the substrate in a solution of a commercially available alkylphosphonic acid in a gentle solvent (2-propanol). Anchoring of the alkylphosphonic acid molecules on the AlO_x surface occurs by heterocondensation of the phosphonic acid groups with surface hydroxyl groups[20] and involves the formation of mono-, bi-, or tridentate adsorption complexes (with the phosphonic acid group binding to the surface via one, two, or three P-O-Al linkages).[21–23] Mono- or bidentate surface binding would also allow the unreacted phosphonic-acid moieties to crosslink with adjacent molecules. One concern with AlO_x/SAM dielectrics is whether the AlO_x surface might be corroded by the alkylphosphonic acid. Corrosion has indeed been observed when using phosphonic acids with very short alkyl chain lengths, such as ethylphosphonic acid,[19] but has not been observed with long-chain phosphonic acids, such as octadecylphosphonic acid, which is employed in this work.

AlO_x/SAM gate dielectrics have previously been used to fabricate low-voltage organic complementary circuits on glass[24] and on plastic substrates[25] and are utilized in this work to realize functional organic TFTs and circuits on banknotes. The transistors and circuits have a thickness of less than 250 nm and can be operated with voltages of about 3 V.

A photograph of a 5-Euro note with arrays of organic TFTs and circuits fabricated directly on the surface of the banknote is shown in **Figure 1**a. The fabrication process (described in the Supporting Information) is similar to the process previously reported for the fabrication of low-voltage organic TFTs and circuits on glass.[17] Except for the formation of the SAM, this is an all-dry manufacturing process that avoids the use of liquids and chemicals. The organic semiconductors, dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT)[26,27] for the p-channel TFTs and hexadecafluorocopperphthalocyanine ($F_{16}CuPc$)[28] for the n-channel TFTs, were both deposited in vacuum. The TFTs employ the inverted staggered (bottom-gate, top-contact) device structure. The metal and semiconductor layers were all patterned using polymer shadow masks.[24–27] Mechanical and environmental protection of the TFTs and circuits is in principle possible by covering the devices with a thin organic/metallic passivation layer deposited at room temperature from the vapor phase.[29]

Figure 1 illustrates the significant surface topography of the banknotes. However, because the topography is dominated by long-range waviness, rather than short-range roughness,

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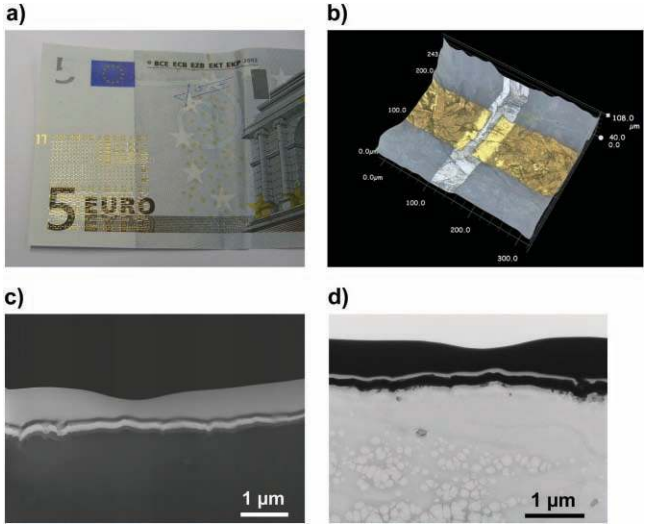

Figure 1. a) Photograph of a 5-Euro note with arrays of organic transistors and circuits. b) Photograph of an individual transistor on a banknote (image acquired with a Keyence VHX-1000 microscope). c) Cross-sectional scanning electron microscopy (SEM) image of the surface of a banknote with an Al/AlO_x/SAM/Au capacitor. d) Transmission electron microscopy (TEM) image of the surface of a banknote with an Al/AlO_x/SAM/Au capacitor (image acquired with an HF-3300 Cold-FE TEM, Hitachi High-Technologies Corp.).

it is possible to obtain organic TFTs with acceptable electrical performance despite this topography. **Figure 2** shows the current-voltage characteristics of a DNTT p-channel TFT and of a F_{16}CuPc n-channel TFT on a 5-Euro note. Owing to the small thickness (5.7 nm) and the large capacitance (700 nF cm^{-2}) of the AlO_x/SAM gate dielectric, the TFTs can be operated with low voltages of about 3 V. Despite the small dielectric thickness, the gate leakage current at the maximum gate bias is below 10^{-9} A, confirming that the plasma-grown AlO_x and the solution-processed alkylphosphonic acid SAM form a continuous, conformal coating with useful insulating properties on the aluminum gate electrodes. The field-effect mobility extracted from the transfer characteristics of the DNTT p-channel TFT is 0.2 cm^2 V^{-1}s^{-1}, which is within a factor of three of the mobility of DNTT TFTs on plastic substrates[27] and within an order of magnitude of the mobility on oxidized silicon substrates.[26] The subthreshold swing is 110 mV per decade, which is close to that of DNTT TFTs on plastic substrates (100 mV decade^{-1}).[27] The mobility of the F_{16}CuPc n-channel TFTs (0.005 cm^2 V^{-1}s^{-1}) is within a factor of 5 of that of F_{16}CuPc TFTs on glass.[17,18,28]

The shortest channel length we are able to realize with polymer shadow masks is 10 μm. A comparison of DNTT TFTs with channel lengths of 10, 15, and 30 μm on a 5-Euro note is shown in Figure S4. The mobility of these TFTs is essentially independent of the channel length (0.2 cm^2 V^{-1}s^{-1}). The shorter TFTs have a larger off-state drain current (10^{-10} rather than 10^{-11} A) and hence a smaller on/off ratio (10^4 rather than 10^5) than the long-channel devices. For comparison, DNTT TFTs on plastic substrates have off-state drain currents of about 10^{-12} A and on/off ratios of about 10^6.[22]

To evaluate the yield and uniformity of organic TFTs on banknotes we measured 100 DNTT transistors with identical channel length (30 μm) and channel width (100 μm) on a 5-Euro note. If we define a TFT as functional if the mobility is at least 0.05 cm^2 V^{-1}s^{-1} and the on/off ratio is at least 3×10^3, then the yield is 92%. The current-voltage characteristics and the distribution of the electrical parameters of these 92 functional TFTs are shown in **Figure 3a** and 3b. Compared with organic TFTs on glass substrates, where the yield is essentially 100% and the parameter variations are only a few percent,[17] the yield we have obtained on banknotes is substantially lower and the parameter distribution is substantially wider. The threshold voltage, for example, has a standard deviation of 80 mV and varies between –1.0 and –1.4 V (see Figure 3b). Such wide parameter variations would be problematic if the TFTs were employed in active-matrix light-emitting diode displays or in analog or mixed-signal integrated circuits, where image fidelity and circuit linearity are strongly dependent on tight parameter uniformity.[24] Properly designed digital circuits, on the other hand, can often tolerate a certain level of parameter variations.[30]

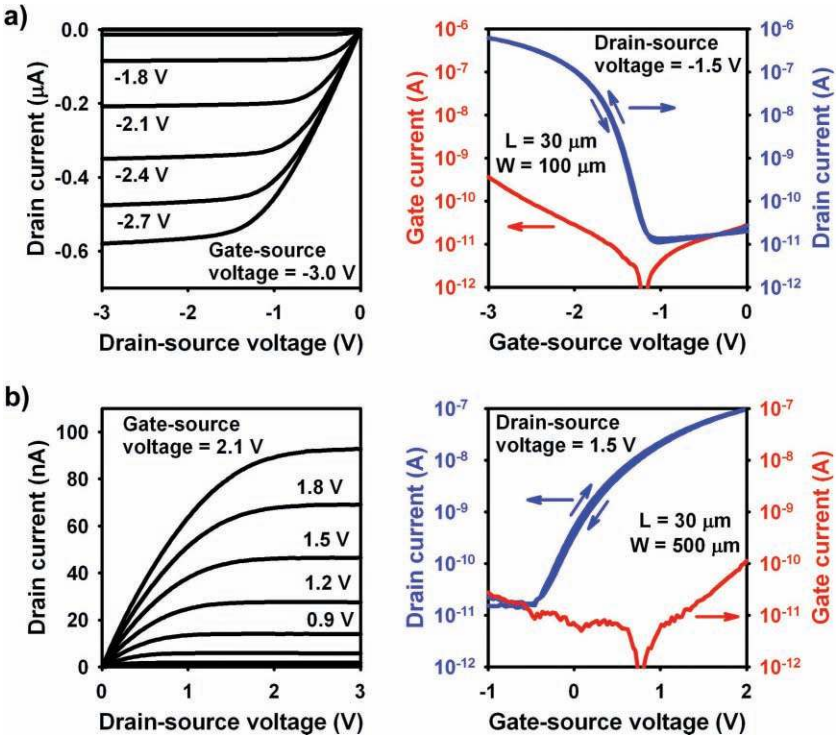

Figure 2. a) Current-voltage characteristics of a DNTT p-channel transistor on a 5-Euro note. The field-effect mobility is 0.2 cm^2 V^{-1}s^{-1}. b) Current-voltage characteristics of a F_{16}CuPc n-channel transistor on a 5-Euro note. The field-effect mobility is 0.005 cm^2 V^{-1}s^{-1}.

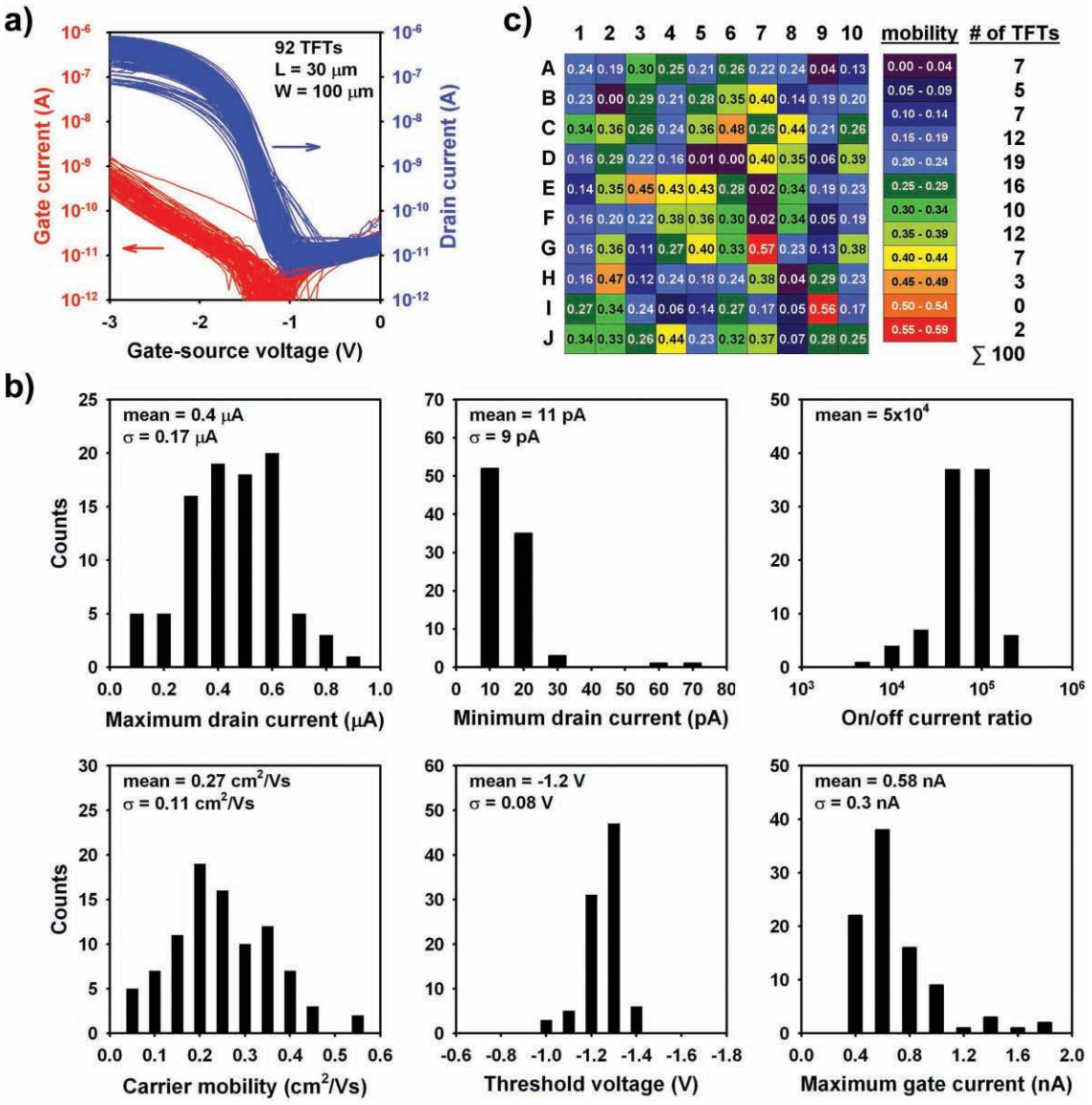

Figure 3. (a) Transfer characteristics of 92 functional DNTT transistors within an array of 100 TFTs fabricated on a 5-Euro note. (b) Statistical distribution of the maximum drain current, the field-effect mobility, the on/off ratio, and the maximum gate current of the 92 functional transistors. (c) Map of the transistor array showing the distribution of the field-effect mobility. The array has an area of 10×8 mm^2. Transistors A9, B2, D5, D6, E7, F7 and H8 are considered non-functional because their mobility is below 0.05 cm^2/Vs, and transistor D4 is non-functional because its on/off ratio is below 3×10^3.

To better understand the mechanisms that limit the device yield on banknotes we have looked for a correlation between the performance of a given TFT within the array and the location of distinct topographical features visible on the surface of the banknote. Figure 3c shows a map of the distribution of the TFT mobility within the array. Transistors A9, B2, D5, D6, E7, F7, and H8 are considered non-functional because their mobility is below 0.05 cm^2 V^{-1} s^{-1}, and transistor D4 is non-functional because it has an on/off ratio of less than 3×10^3. Six of these eight non-functional TFTs (D4, D5, D6, E7, F7, H8) are located in close proximity to each other near the center of the array, which suggests that there might be a common cause for the lack of performance of these devices, possibly related to an agglomeration of fibers at the surface of the banknote in this particular region. **Figure 4** shows a photograph and the current-voltage characteristics of each of the eight non-functional TFTs (A9, B2, D4, D5, D6, E7, F7, H8). For comparison, a photograph and the electrical characteristics of transistor G7, which has an excellent mobility (0.57 cm^2 V^{-1} s^{-1}) and on/off ratio (7×10^4), are also shown. In the photographs of some of the non-functional devices (A9, D4, D5, D6) large fibers that might be deemed responsible for the lack of performance are indeed clearly seen. On the other hand, no large fibers are visible in the photographs of some of the other

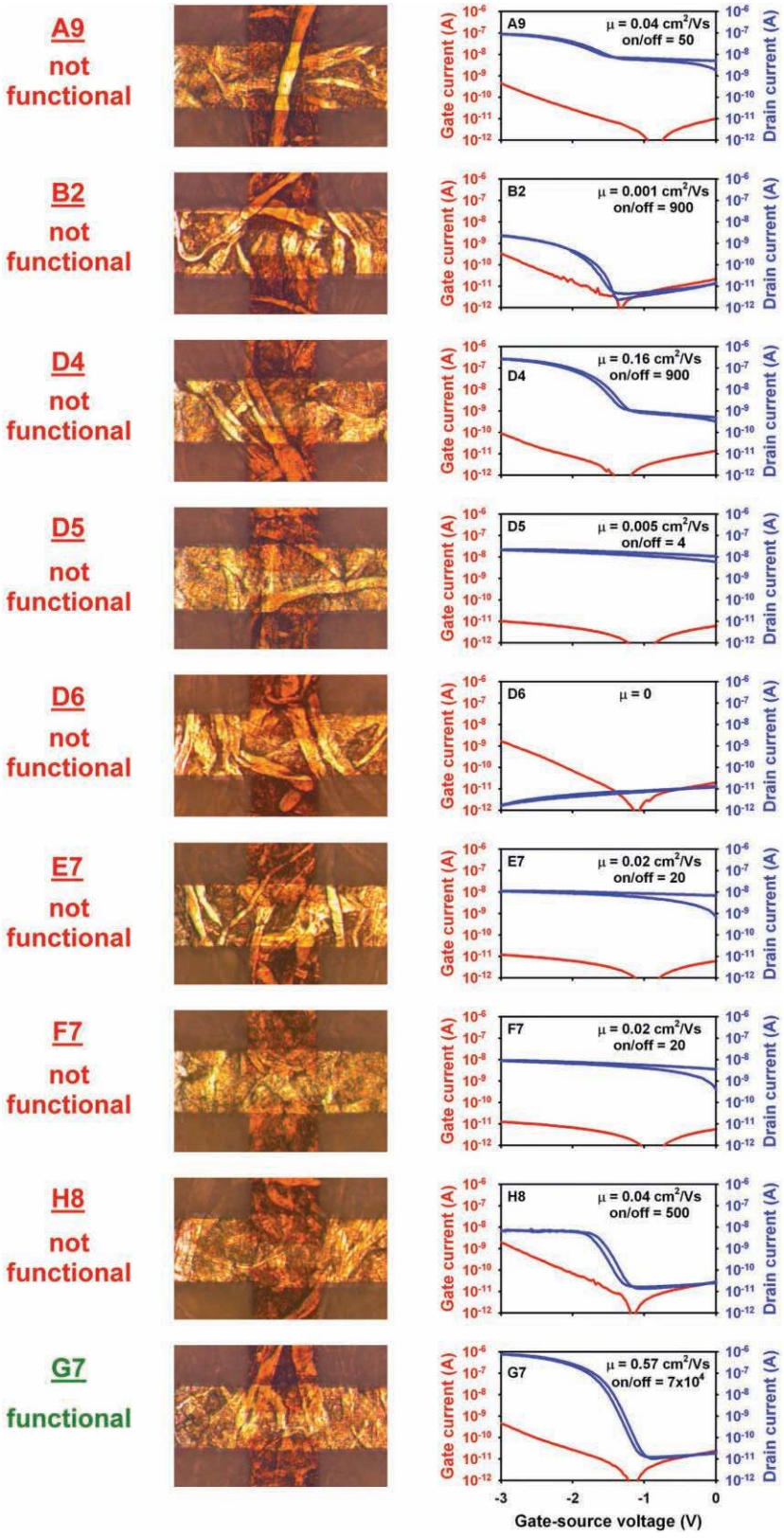

Figure 4. Photographs and current-voltage characteristics of eight non-functional transistors (A9, B2, D4, D5, D6, E7, F7, H8) and one functional transistor (G7) out of 100 DNTT transistors on a 5-Euro note. A clear correlation between the presence of large fibers and the transistor performance is not apparent.

non-functional TFTs (F7, H8). Interestingly, the photograph of the high-performance transistor (G7) clearly shows several large fibers, which apparently have no detrimental effect on the electrical performance of this device. Thus, a clear correlation between surface topography and TFT performance is not immediately apparent.

In order to assess the dynamic performance of organic TFTs on banknotes we fabricated unipolar inverters consisting of two DNTT TFTs (one acting as a drive transistor, the other as a saturated load device; see Figure S6). When operated with a supply voltage of 3 V, these inverters are capable of switching digital signals at frequencies of up to about 2 kHz (see Figure S6). This frequency is several orders of magnitude higher than the operating frequency previously reported for organic TFTs on paper[13,14] and is within an order of magnitude of the frequency of low-voltage organic TFTs on plastic substrates.[27]

Frequencies of a few kilohertz may already be sufficient for basic logic operations. However, as Figure S6 indicates, the small-signal gain, the output swing, and the noise margins of the unipolar circuits are quite small, which may lead to problems with the signal integrity in circuits of greater complexity.[30] Also, unipolar circuits have a relatively large static power consumption, since the load transistor is always conducting. These drawbacks are eliminated in complementary circuits, which employ p-channel and n-channel transistors.[31] **Figure 5** shows a photograph and the static transfer characteristics of a complementary inverter comprised of a F_{16}CuPc n-channel TFT and a DNTT p-channel TFT on a 5-Euro note. The static characteristics of these complementary inverters (supply voltage about 3 V, static power consumption <1 nW, small-signal gain about 100) are comparable to those of silicon complementary circuits fabricated on silicon membranes and transferred from a silicon wafer onto a flexible plastic substrate.[4] The maximum operating frequency of the organic complementary circuits is limited to a few hundred Hertz by the relatively small field-effect mobility of the F_{16}CuPc n-channel TFTs (see Figure S7). However, operating frequencies in the range of a few kilohertz are feasible by employing conjugated organic semiconductors with larger electron mobilities.[32–34]

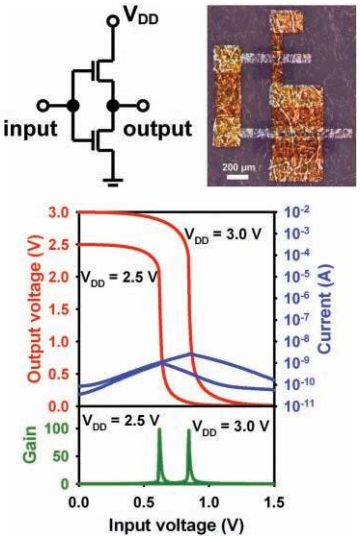

Figure 5. Circuit schematic, photograph, and static transfer characteristics of an organic complementary inverter on a 5-Euro note.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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Supporting Information

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1. Device Fabrication Process

The organic TFTs employ the inverted staggered (bottom-gate, top-contact) device structure and are fabricated directly on the surface of the banknotes (see Figure S1).

In the first step of the device process, the gate electrodes of the TFTs are defined by evaporating 70 nm thick aluminum through a polymer shadow mask (CADiLAC Laser, Hilpoltstein, Germany).

To create access to the gate electrodes, 50 nm thick gold is then evaporated through a second shadow mask in specific areas on the aluminum.

To form the gate dielectric, the banknote is then exposed to an oxygen plasma for a few seconds (plasma power: 150 W, duration: 15 s; increases the thickness of the native AlO_x layer from ~1.5 to 3.6 nm) and then immersed in a 2-propanol solution of *n*-octadecylphosphonic acid (from PCI Synthesis) for about one hour (results in a 2.1 nm thick SAM on the AlO_x surface).

50 nm of hexadecafluorocopperphthalocyanine ($F_{16}CuPc$; from Sigma Aldrich) and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) are then deposited in vacuum through a third and fourth shadow mask as the organic semiconductors for the n-channel and p-channel TFTs. During the semiconductor depositions the banknote is held at temperatures of 90 °C for the $F_{16}CuPc$ and 60 °C for the DNTT deposition, since this was found to give the best device performance.

TFTs and circuits are completed by evaporating 100 nm thick gold through a fifth shadow mask to define the source and drain contacts.

Except for the formation of the phosphonic acid SAM, this is an all-dry manufacturing process. The highest process temperature is 90 ºC. During the depositions, the banknote is always covered by a shadow mask, so the materials are deposited only where needed for the devices, and no processing is required to pattern the films or remove excess material. The formation of the AlO_x is specific to the aluminum surfaces, and the formation of the SAM is specific to the plasma-generated AlO_x surfaces, so these two materials also do not require post-growth patterning. Neither the oxygen-plasma exposure to form the thin AlO_x layer, nor the exposure to 2-propanol for the formation of the self-assembled monolayer, nor heating to 90 ºC during the semiconductor deposition cause any detectable damage to the banknotes.

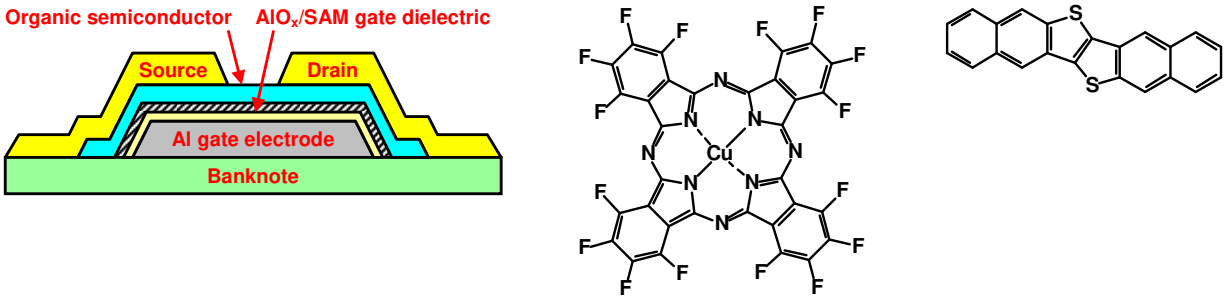


Figure S1. Left: Schematic cross-section of the organic thin-film transistors (TFTs). Center: Hexadecafluorocopperphthalocyanine ($F_{16}CuPc$), the semiconductor for the n-channel TFTs. Right: Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), the semiconductor for the p-channel TFTs.

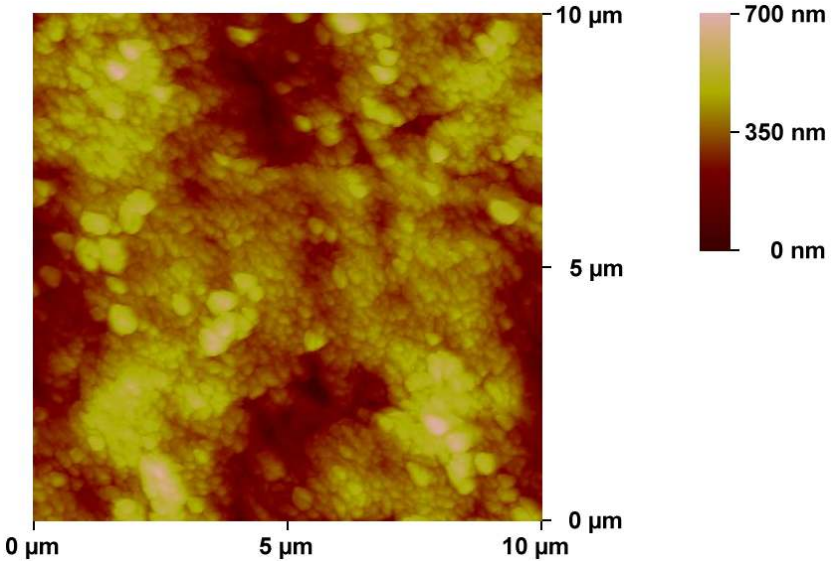
2. Electrical Characterization

All of the electrical measurements are performed in ambient air at room temperature under weak yellow laboratory light.

3. Microscopy Images

Figure S2 and Figure S3 show atomic force microscopy (AFM), cross-sectional scanning electron microscopy (SEM), and cross-sectional transmission electron microscopy (TEM) images of the surface of a banknote (The latter two are also shown in Figure 1 and are reproduced here for better clarity.)

Figure S2. Atomic force microscopy (AFM) image of the surface of a banknote.



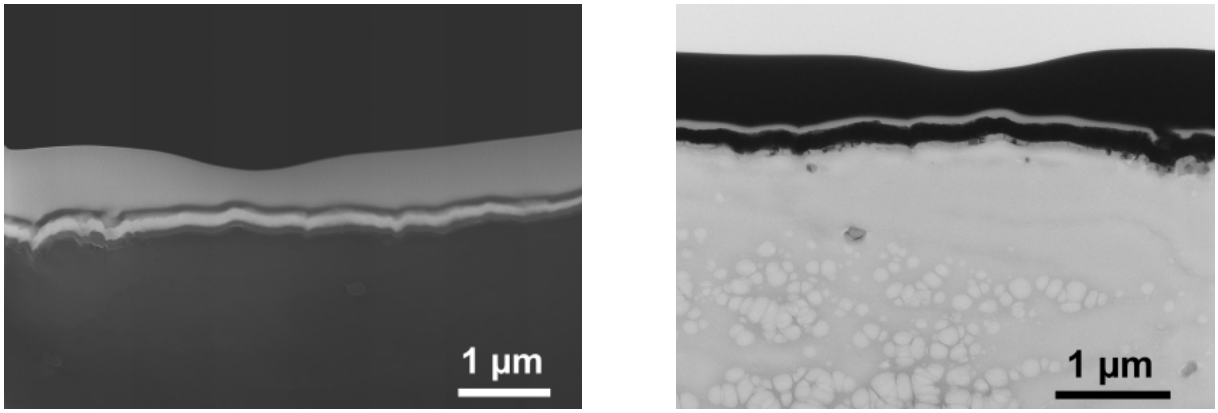


Figure S3. Cross-sectional scanning electron microscopy (SEM; left) and transmission electron microscopy (TEM; right) images of the surface of a banknote with an Al/AlO_x/SAM/Au capacitor.

4. Lateral Transistor Dimensions

The maximum frequency f_T at which a field-effect transistor can be operated is determined by its transconductance g_m and gate capacitance C_{gate}:

$$f_T = \frac{g_m}{2\pi C_{gate}}$$

where

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu C_{diel} W V_{DS}}{L}$$

and

$$C_{gate} \approx C_{diel} \; W(L + \Delta L)$$

so that

$$f_T = \frac{\mu V_{DS}}{2\pi L(L + \Delta L)} \qquad (1)$$

where I_D is the drain current, V_{GS} and V_{DS} are the gate-source and drain-source voltage, μ is the carrier mobility, W is the channel width, and C_{diel} is the gate dielectric capacitance per unit area (here: C_{diel} = 700 nF/cm^2).

It can be seen that transistor operation at high frequencies requires a small channel length (L) and gate-to-contact overlap (ΔL). Figure S4 shows photographs and electrical characteristics of DNTT transistors on a 5-Euro note with channel length and gate to source overlap ranging from 30 µm to 10 µm. All TFTs were patterned using manually aligned polymer shadow masks.

According to Equation (1), TFTs with channel length and gate overlap of 10 µm has a maximum frequency f_T of about 10 kHz.

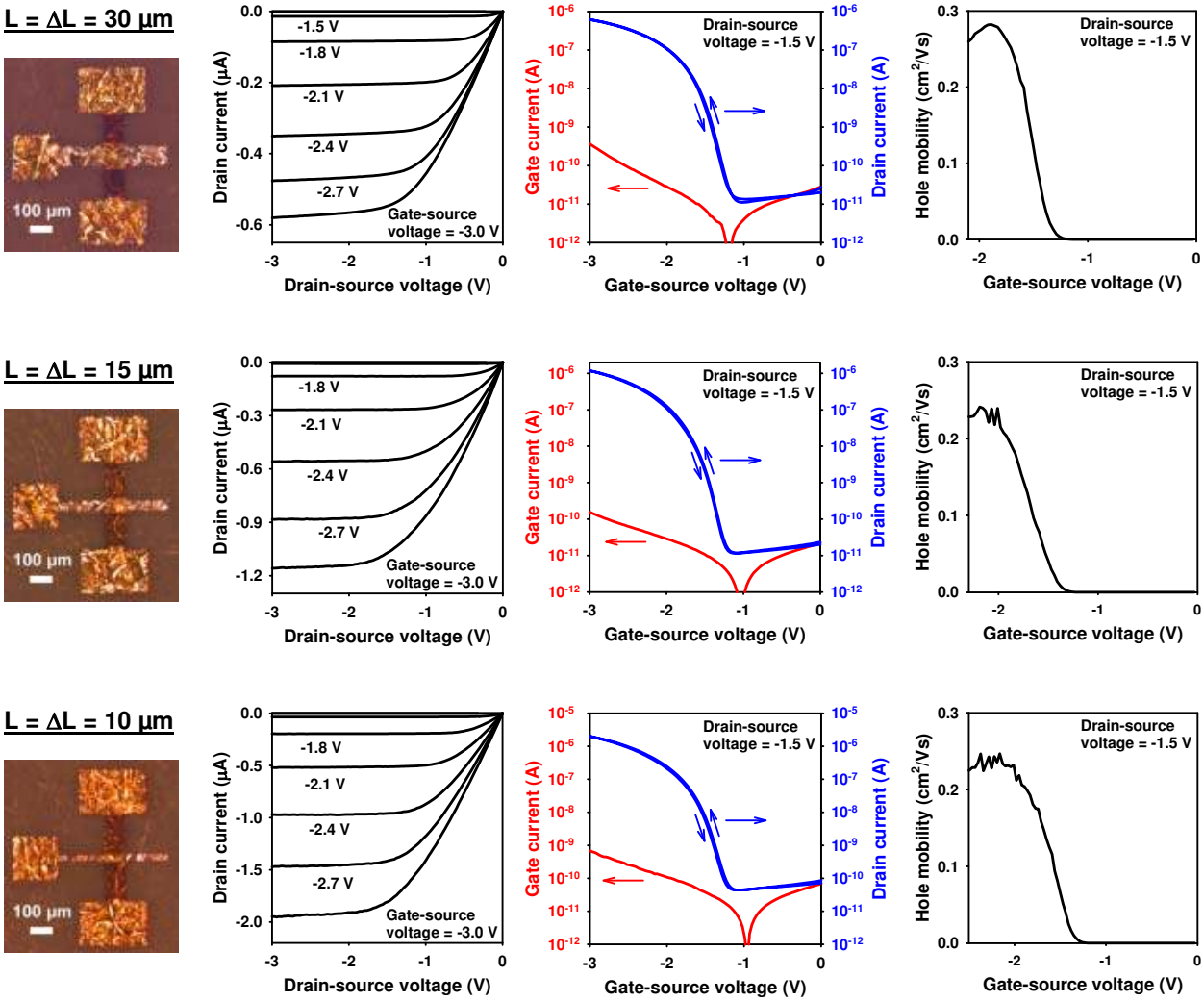
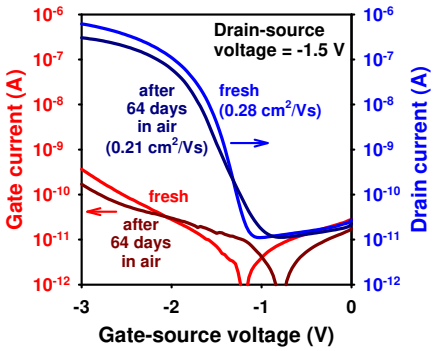


Figure S4. Current-voltage characteristics of DNTT TFTs with a channel length and a gate-to-contact overlap of 30 µm, 15 µm and 10 µm on a 5-Euro note. All three TFTs have a channel width of 100 µm. The carrier field-effect mobility is between 0.2 and 0.3 cm^2/Vs for all three TFTs.

Figure S5. Transfer characteristics of a DNTT TFT with a channel length of 30 µm and a channel width of 100 µm on a 5-Euro note measured immediately after fabrication ("fresh") and measured again after the banknote had been exposed to air at room temperature for 64 days. As can bee seen, the carrier mobility has decreased only slightly, from 0.28 to 0.21 cm^2/Vs, while the on/off ratio has decreased from 5×10^4 to 3×10^4. This confirms the excellent air-stability of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene.



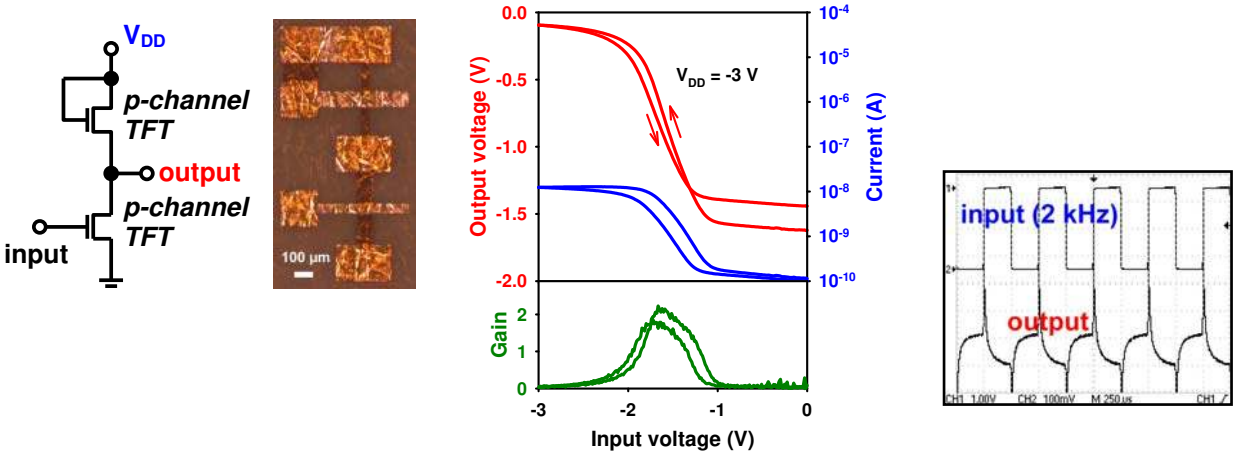


Figure S6. Circuit schematic, photograph, static voltage transfer characteristics, and dynamic switching characteristics of an organic unipolar inverter based on DNTT p-channel TFTs on a 5-Euro note. The inverter shows the correct logic function and responds to input signals with a frequency of a few kilohertz.

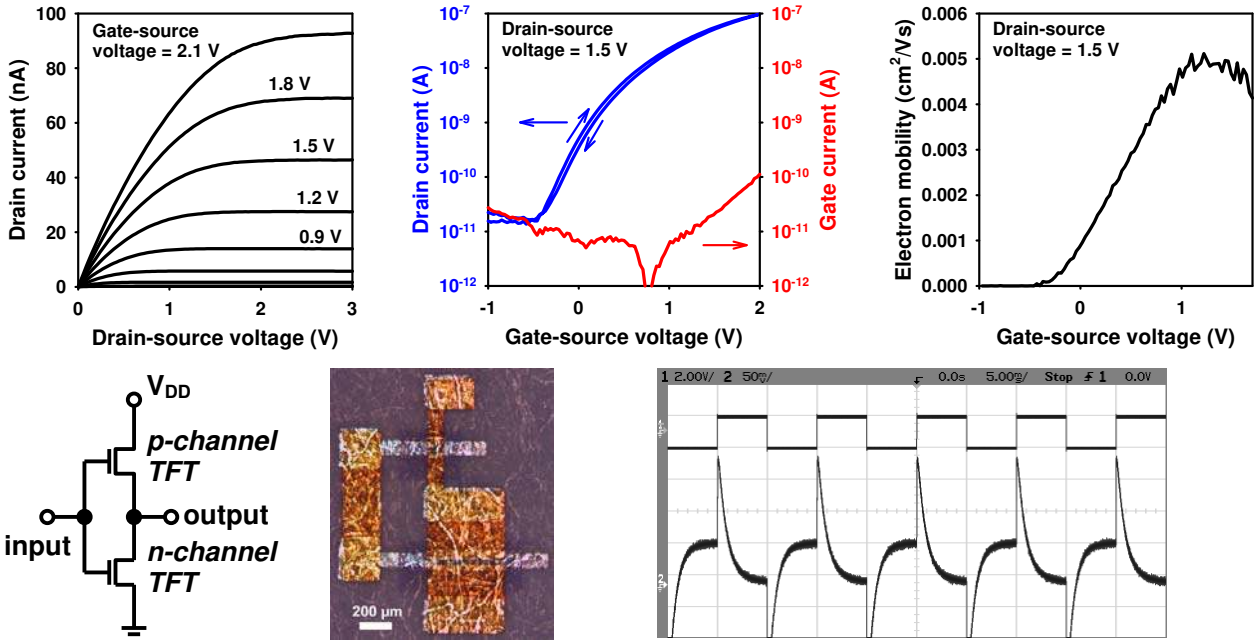


Figure S7. Top: Current-voltage characteristics of an $F_{16}CuPc$ n-channel TFT on a 5-Euro note. Bottom: Circuit schematic, microscope photograph, and dynamic switching characteristics of a complementary inverter based on organic p-channel and n-channel TFTs on a 5-Euro note. The inverter shows the correct logic function (see Figure 5) and responds to input signals with a frequency of a few hundred Hertz.

Figure S8. Organic TFTs have also been fabricated on US-dollar, Swiss-franc and Japanese-yen notes. This figure shows the electrical characteristics of p-channel TFTs with a channel length of 30 µm and a channel width of 100 µm using pentacene as the semiconductor. The carrier mobility of these TFTs is between 0.01 and 0.02 cm^2/Vs, and the on/off ratio is between 10^3 and 10^4.