ORGANIC FIELD-EFFECT TRANSISTORS ON NOVEL RENEWABLE SUBSTRATES

A Dissertation
Presented to
The Academic Faculty

By

Cheng-Yin Wang

In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2016

ORGANIC FIELD-EFFECT TRANSISTORS ON NOVEL RENEWABLE SUBSTRATES

Approved by:

Dr. Bernard Kippelen, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Gee-Kung Chang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Samuel Graham
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: October 25, 2016

To my family

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Bernard Kippelen for his support and guidance. Without him, I could not finish my PhD degree. I also would like to thank Dr. Oliver Brand, Dr. Saibal Mukhopadhyay, Dr. Gee-Kung Chang, and Dr. Samuel Graham for participating as my committee members giving evaluations and suggestions on my dissertation and oral presentation.

During my PhD study, I enjoyed the time working with all current and former Kippelen Research Group members. I am grateful for having help from all of them, especially our research scientist Dr. Canek Fuentes-Hernandez for mentoring me in many details. I truly appreciate the experience and lessons learning from him. I would like to thank our former group members in OFET subgroup: postdoctoral researchers Dr. Sanjeev Singh and Dr. Minseong Yun for training me at the very beginning, and group member Dr. Sangmoo Choi for helps on e-beam evaporation systems in IEN cleanroom and valuable discussions on my research. I also would like to thank support and assistance from all current and former colleagues: Dr. Yinhua Zhou, Dr. Talha Khan, Dr. Jaewon Shim, Dr. James Hsu, Dr. Amir Dindar, Dr. Michael Gaj, Dr. Keith Knauer, Dr. Ehsan Najafabadi, Dr. Asha Sharma, Alfred Ernst, Vladimir Kolesov, Wen-Fang Chou, Xiaojia Jia, Xiaoqing Zhang, Felipe Larrain, Victor Rodriguez Toro, and our administrative manager Tina Moseley.

Many valuable collaborations and team works during my PhD study were not only within our group, but also with other groups at Georgia Institute of Technology. Therefore, I would like to thank Dr. Raghunath Dasari and Dr. Yulia Getmanenko from

Dr. Seth Marder's group, Ankit Singh from Dr. Samuel Graham's group, and Dr. Boyi Fu from Dr. Elsa Reichmanis' group. I also would like to thank collaborations with Dr. Jeffrey Youngblood's group at Purdue University and Dr. Robert Moon at U.S. Forest Service.

This work was partially funded by United States Department of Agriculture, United States Department of Energy, Office of Naval Research, Bay Area Photovoltaic Consortium, and Samsung Display.

Last but not least, I want to thank my wife Yin-Chun Chen for her support from a long distance, my mother Mei-Ying Chen for investing and educating me, my memorable father Wen-Bi Wang, my sister Li-Jing Wang, and all my family. Without you, I would not be able to make all my achievements.

TABLE OF CONTENTS

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF SYMBOLS

C_D	The capacitance density of depletion region
C_{it}	The capacitance density of interface traps
C_{OX}	The capacitance density of oxide
D_{it}	Interface trap density
γ	Characteristic exponent
I_{DS}	Drain to source current
I_{ON}/I_{OFF}	On/off current ratio
k	Boltzmann constant
λ	Channel length modulation
L	Channel length
L_c	Characteristic channel length
μ	Carrier mobility
q	Elementary electron charge
R_c	Contact resistance
R_{ch}	Channel resistance
R_cW	Channel width-normalized contact resistance
R_{ON}	On-state resistance
R_{sh}	Sheet resistance
T	Kelvin temperature scale
V_{aa}	Mobility enhancement voltage
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage

V_{SS}	Subthreshold voltage
V_{TH}	Threshold voltage
W	Channel width

LIST OF ABBREVIATIONS

ALD	Atomic layer deposition
C_8-BTBT	2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene
CNC	Cellulose nanocrystal
CNF	Cellulose nanofiber
CYTOP	Poly [1,1,2,4,4,5,5,6,7,7-decafluor-3-oxa-1,6-heptadiene]
CVD	Chemical vapor deposition
DPh-DNTT	Dinaphtho[2,3- *b* :2 ′ ,3 ′ - *f*]thieno[3,2- *b*]thiophene
EA	Electron affinity
F_4TCNQ	Tetrafluoro-tetracyanoquinodimethane
F_6TCNNQ	1,3,4,5,7,8-hexafluorotetracyanonaphthoquinodimethane
HOMO	Highest occupied molecular orbital
IP	Ionization potential
IPA	Isopropanol
LUMO	Lowest unoccupied molecular orbital
$Mo(tfd)_3$	Molybdenum tris-[1,2-bis(trifluoromethyl)ethane-1,2-dithiolene]
NL	Nanolaminate
OFET	Organic field-effect transistor
OLED	Organic light-emitting diode
OPV	Organic photovoltaic
OSC	Organic semiconductor layer
PDMS	Poly-dimethlysiloxane
PFBT	2,3,4,5,6-pentafluorothiophenol

PTAA	Poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]
PTCDI	Perylene tetracarboxylic diimide
PVA	Polyvinyl alcohol
PVP	Polyvinylpyrrolidone
RH	Relative humidity
SS	Subthreshold swing
Tetralin	1, 2, 3, 4-Tetrahydronaphthalene
TFT	Thin-film transistor
TIPS-pentacene	6, 13-Bis(triisopropylsilylethynyl)pentacene
XPS	X-ray photoelectron spectroscopy

SUMMARY

With the increasing awareness of environmental impact from electronic waste and increasing demand for flexible electronic devices, novel substrates with both biodegradability and flexibility have been studied in various fields. To develop such electronic devices, organic electronic technology has attracted attention because of its low process temperature at a range of 60 to 100 °C which is compatible with substrates having these two features. Among organic electronic devices, organic field-effect transistors (OFETs) are an important building block because transistors can implement circuits to integrate with other organic electronic devices such as organic light-emitting diodes (OLEDs) and organic photovoltaics (OPVs).

This dissertation reports solution-processed high-performance top-gate OFETs with operational and environmental stability on novel renewable substrates. The first achievement is demonstrating top-gate OFETs with a bilayer CYTOP/Al_2O_3 gate dielectric on environmentally friendly renewable cellulose nanocrystal (CNC):glycerol substrates. OFETs were fabricated on water soluble CNC:glycerol substrates with a protection layer of Al_2O_3 by atomic layer deposition. OFETs with that protection layer have better operational and environmental stability compared to that of OFETs on bare CNC:glycerol substrates. The second achievement is reducing contact resistance of top-gate OFETs. By depositing 1.5 nm of $Mo(tfd)_3$ on source/drain electrodes, contact resistance can be 0.25 of that from contact electrodes using the conventional PFBT treatment. The third achievement is developing a nanolaminate structure comprised of Al_2O_3 and HfO_2 to replace Al_2O_3 in the gate dielectric bilayer in top-gate OFETs to improve their environmental stability while achieving comparable operational stability.

OFETs with a modified gate dielectric have comparable electrical properties, operational stability, and environmental stability compared to that of OFETs with CYTOP/Al_2O_3; furthermore, OFETs with a modified gate dielectric are functioning after storing in hot water at 95 °C for up to 1 h that is much longer than that of OFETs with the original bilayer gate dielectric. The last achievement is presenting top-gate OFETs with modified gate dielectric and reduced contact resistance on cellulose-based paper substrates. OFETs on this type of paper can achieve comparable electrical properties, operational stability, and bending characteristics by the proper choice of a buffer layer coated on top of the paper substrate.

In this dissertation, the development of OFETs on novel substrates have been described, and the future study is suggested.

CHAPTER 1

INTRODUCTION

1.1 Printed electronics

Electronic waste has been increasing dramatically with economic development for decades. With growing awareness of the environmental impact of electronic waste, the electronics industry is devoting a great deal of attention not only to its profitability but also to establishing environmentally friendly manufacturing processes such as printing techniques.

Electronic devices manufactured by printing techniques are referred as printed electronics. Printed electronic devices can be large, thin, light-weight, and flexible because they are processed from solution at temperatures near room temperature, and they can be fabricated on plastic substrates. The process of printing such electronics has several potential advantages including low production cost, mass production capability, and reduced environmental impact because it potentially avoids using traditional electronics subtractive manufacturing processes such as photolithography and vacuum processes for metallization and etching that consume more energy and materials.

These simplified processes are currently used to produce radio frequency identification tags and printed electrodes for Si solar panels [1, 2]. Novel products such as organic field-effect transistor (OFET) array-based sensors, wearable and bendable displays (electronic papers) using OFETs and organic light-emitting diodes (OLEDs) have been launched in to the market, and devices such as transparent displays and organic photovoltaics (OPVs), using printed electronics, are under development [3]. According to

an IDTechEX forecast, the market value of printed electronics is about $ 30 billion in 2015 and by 2025, is expected to be $ 70 billion [4].

1.2 An introduction to organic field-effect transistors

1.2.1 Organic semiconductors

Organic semiconductors are carbon-based organic materials that display semiconducting properties used as the transport layer in OFETs [5]. The semiconducting properties arise from interactions between carbon atoms. When two carbon atoms bind to form a molecule, the orbitals in each carbon atom can hybridize into sp, sp^2, and sp^3 orbitals. One example of a type of bond that can be formed between two carbon atoms is the bonding in an ethylene molecule. An illustration of such a molecule is presented in Figure 1. In the ethylene molecule, each carbon atom contains one p_z orbital and three sp^2 hybridized orbitals, which form coplanar σ bonds.

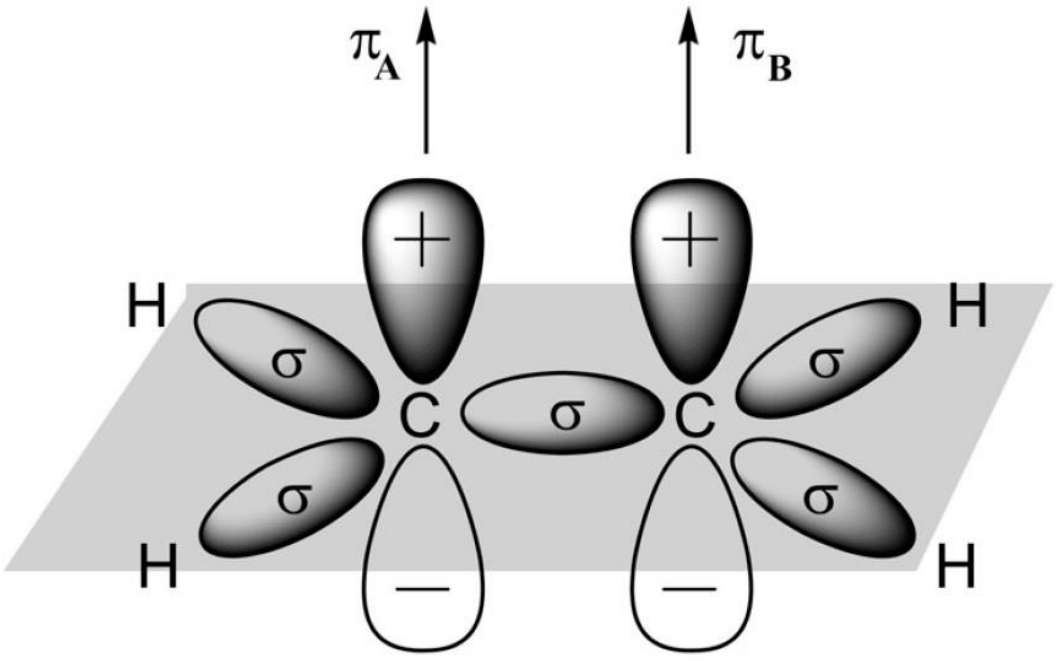


Figure 1. An ethylene molecule.

The linear superposition of wave functions of p_z electrons leads to the formation of two orbitals in molecules: a bonding orbital, referred to as π (the highest occupied molecular orbital, HOMO), and an antibonding orbital, referred to as π^* (the lowest unoccupied molecular orbital, LUMO), as shown in Figure 2. The σ bonding is stronger than the π bonding, and the electrons participating in this type of π bonding are more delocalized. Electrons on π bonds are generally referred to as π electrons. In organic molecules, σ bonds and π bonds are formed alternatively in structures known as conjugated structures, over which the π electrons are delocalized. Molecules displaying this type of structure are known as conjugated molecules. When molecules coexist in bulk materials, their intermolecular interactions lead to homogeneous broadening of these HOMO-LUMO energy states, forming energy bands. Between the HOMO and LUMO is a gap, which is only an approximation of the fundamental gap, defined as the difference between the ionization potential (IP) and the electron affinity (EA). The IP and EA correspond to the bottom of the conduction band and the top of the valence band. This energy band description of organic semiconductors is analogous to that of inorganic semiconductors.

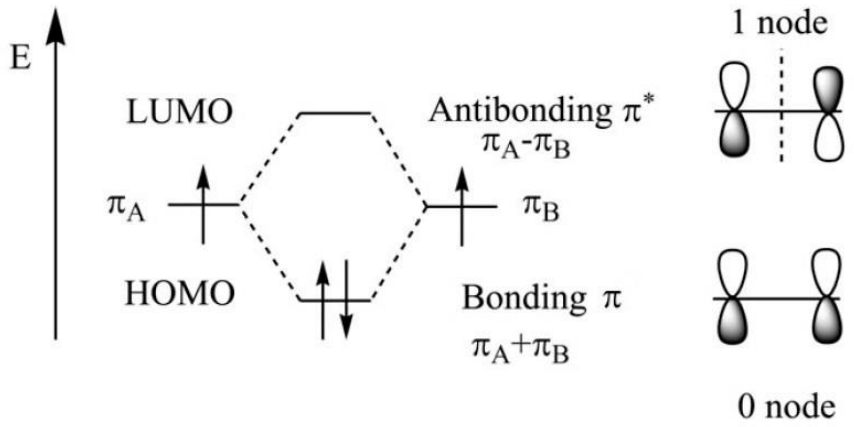


Figure 2. Bonding and antibonding orbitals.

1.2.2 The evolution of OFETs

The principle of operation of a field-effect transistor [6] was first proposed by Lilienfeld between 1926 and 1930. The field-effect transistor structure is illustrated in Figure 3: the source and the drain are connected to the two sides of the channel; the gate is isolated from the channel by an insulating layer. By applying the proper voltage on the gate electrode, the capacitor between the gate and the channel can modulate charges inside the channel. However, this idea had not been realized until the first field-effect transistor, a metal-oxide-semiconductor field-effect transistor [7], was demonstrated by Kahng and Atalla in 1960.

In the organic electronic field, the first highly conducting polymer, polyacetylene [8], was discovered in 1977 by Heeger, MacDiarmid, and Shirakawa, who were awarded the Nobel Prize in Chemistry in 2000. This discovery initiated plenty of research on conducting polymers, and the use of organic semiconductors for transistors started in the 1980's. Ebisawa was the first one to use polyacetylene [9] in OFETs with a small current modulation in 1982. The first OFET [10] was realized by Tsumura, Koezuka, and Ando in 1986. They demonstrated the first OFET with a polythiophene thin film. The carrier mobility of the first OFET was of the order of 10^{-5} cm^2/Vs and the threshold voltage was -13 V. Not only conducting polymers but also small molecules play important roles in organic electronics. The first small-molecule OFET [11], using alpha-sexithienyl film as an active layer, was demonstrated in 1989 by Horowitz *et al.* The carrier mobility was 3.3 $\times 10^{-4}$ cm^2/Vs, better than the first polymer OFET, and the threshold voltage was only -2 V. Over decades, the carrier mobility of OFETs has made a great progress on both p-channel materials to the range of 10 to 20 cm^2/Vs [12-15] and n-channel materials to the

range of 1 to 10 cm^2/Vs [16-18] respectively. Single crystal rubrene-based p-channel OFETs demonstrated carrier mobility on 10.4 to 11.2 cm^2/Vs [12, 13, 15], and n-channel OFETs also displayed high carrier mobility on small molecules such as PTCDI with 1.7 to 2.1 cm^2/Vs [16, 17] and C_{60} with 2.2 cm^2/Vs [18]. Furthermore, printed OFETs achieved high average carrier mobility at 16.4 cm^2/Vs (up to 31.3 cm^2/Vs) on single crystalline p-channel C_8-BTBT film [14] and on n-channel polymer P(NDI2OD-T2) with carrier mobility at 0.45 to 0.85 cm^2/Vs [19]. These evolution makes that OFETs can compete with a-Si and poly-Si thin-film transistors (TFTs).

1.2.3 The basic working principle of OFETs

An OFET is an electronic device with three terminals: a gate, a source, and a drain. As shown in Figure 3, an OFET consists of a channel composed of an organic semiconducting material between the drain and the source electrodes and separated from the gate electrode by a gate dielectric layer. The basic principle of an OFET is similar to that of a conventional transistor based on inorganic field-effect transistors. A field-effect transistor is a voltage-controlled electronic device. With a voltage applied between the gate and source electrode (V_{GS}), a voltage drop between the gate and source electrodes controls the current flowing through the channel between the source and drain electrodes. In case of an ideal n-channel OFET, when V_{GS} is below a certain value, known as the threshold voltage V_{TH}, no current flows between the source and the drain electrodes, and the transistor is turned off. When V_{GS} is larger than V_{TH}, current flows between the source and the drain, and the transistor is turned on.

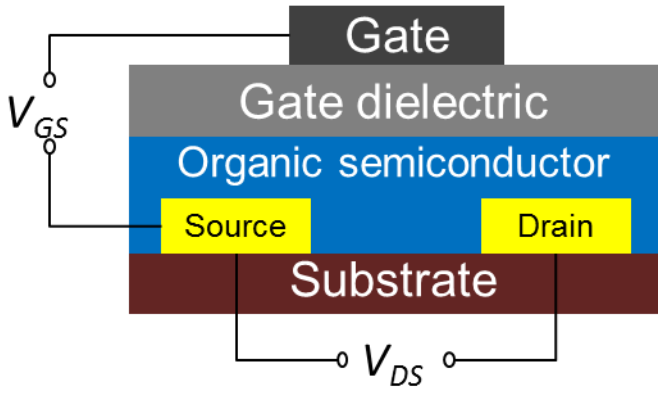


Figure 3. Schematic representation of an OFET.

An OFET can display three regimes of operation: the cut-off regime, the linear regime, and the saturation regime. All of the regimes are determined by relationships between the V_{GS}, V_{TH}, and the drain-to-source voltage V_{DS}. When $V_{GS} < V_{TH}$, OFETs are in the cut-off regime, and charges are not induced to form the channel, so drain to source current I_{DS} equals zero. When $V_{GS} > V_{TH}$ and $V_{GS} - V_{TH} > V_{DS}$, OFETs are in the linear regime, where increased V_{GS} induces a charge density in the channel, and current I_{DS} can flow, which increases linearly with V_{DS}. In this regime the current is given by [20]:

$$I_{DS} = \mu C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{2}\right]. \qquad (1)$$

where μ is carrier mobility, C_{ox} is the capacitance density of the gate oxide layer (in our case is gate dielectric layer), W is the channel width, L is the channel length. As V_{DS} increases, a transition from the linear regime to the so-called saturation regime occurs when the voltage drop between the drain and the gate, $V_{GS} - V_{DS}$, at the drain end of the channel equals V_{TH}. Under this circumstance, $V_{GS} - V_{DS}$ at the drain end of the channel is barely above the threshold, a condition referred to as "pinch-off." When $V_{DS} > V_{GS} - V_{TH}$, the pinch-off point approaches the source end of the channel, and carriers are swept into the pinch-off region at a saturation drift velocity because of the high electric field along

the channel. When $V_{GS} > V_{TH}$ and $V_{GS} - V_{TH} \leq V_{DS}$, OFETs operate in the saturation regime, where current I_{DS} does not increase with V_{DS} but with $V_{GS} - V_{TH}$, and is given by [20]:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu C_{OX}\left(V_{GS} - V_{TH}\right)^2. \quad (2)$$

From the current-voltage relations discussed above, we can investigate many important parameters of OFETs such as the carrier mobility (μ), V_{TH}, the on/off current ratio, (I_{on}/I_{off}), and the contact resistance, (R_c). Carrier mobility μ and threshold voltage V_{TH} are extracted in the saturation regime: V_{TH} is first extracted by linear extrapolation from $V_{GS} - V_{TH}$ versus the square root of the I_{DS} plot; μ will then be extracted from equation (2) with known channel width W, channel length L, gate dielectric capacitance density C_{ox}, I_{DS}, and $|V_{GS}| - |V_{TH}|$. On/off current ratios I_{on}/I_{off} can be calculated by measuring the off-state I_{DS} and maximum on-state I_{DS}. Contact resistance R_c can be extracted in the linear regime of OFETs with different W/L ratios by using the transfer length method. According to this method, the on-state resistance R_{ON} is extracted as V_{DS} approaches 0 V using the following expression [21]:

$$R_{ON} = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{DS}\to 0} = R_{ch} + 2R_c = R_{sh}\frac{L}{W} + 2R_c, \quad (3)$$

where R_{ch} is the channel resistance and R_{sh} is the sheet resistance of the channel. The ordinate in the plot of R_{ON} vs. L when L equals zero corresponds to $2R_c$. High μ, high I_{on}/I_{off}, low $|V_{TH}|$, and low R_c are the most common indicators of a high-performance OFET.

1.2.4 More parameters and modeling of OFETs

In addition to the basic working principal of OFETs, more parameters are taken into account when it comes to the real world. The first thing will be the subthreshold slope (SS) coming from the leakage current from the source to the drain when gate voltage is below but close to the threshold voltage. SS can be extracted from the transfer characteristic and is defined as:

$$SS \equiv \frac{dV_{GS}}{d(\log(I_{DS}))} \tag{4}$$

and it is approximately [22]:

$$SS \approx ln10 \frac{kT}{q}\left[1 + \frac{C_D + C_{it}}{C_{OX}}\right] \tag{5}$$

where k is Boltzmann constant, T is temperature in Kelvin scale, q is elementary electron charge, C_{ox} is the capacitance density of the gate oxide layer (in our case is gate dielectric layer), C_D is the capacitance of the semiconductor depletion region, and C_{it} is the capacitance of interface traps equals to qD_{it} where D_{it} is the interface trap density. Since there is no depletion region in OFETs, C_D is zero in equation (5) and the interface trap density can be extracted from equation (5) and given as [22]:

$$D_{it} \approx \left[\frac{qSSlog(e)}{kT} - 1\right]\frac{C_{OX}}{q} \tag{6}$$

In reality, equation (3) and (4) cannot completely describe the current-voltage characteristics of OFETs, for examples: 1) drain current will still increase while OFETs are in the saturation region, therefore the transition from triode region to saturation region and channel length modulation should be considered; 2) the transition below and above threshold will not always be abrupt, therefore subthreshold swing should be considered, too; 3) contact resistance is not negligible on OFETs, therefore the output characteristics

may not be linear in linear region. There have been several compact models consistent with equation (3) and (4) to describe the current-voltage characteristics of OFETs. Three representative compact models were selected and discussed in Kim *et. al.* [23]: Marino *et. al.* [24, 25] focusing on a practical below-to-above threshold transition and linear-to-saturation transition by a small number of parameters, Estrada *et. al.* [26, 27] focusing on the use of a power-law relationship between mobility and gate overdrive voltage, and Li *et. al.* [28] focusing on the potential barrier between grains in a polycrystalline organic film. Based on the emphasized aspect, the model of Marion *et. al.* is chosen to fit OFET characteristics here. In their models, empirical fitting parameters are mostly eliminated, and developed models are also in close correspondence to physicals, parametric, and limiting models for current-voltage and mobility characteristics. The mobility is assumed to follow a power-law dependence featuring the characteristic exponent γ and the mobility enhancement voltage V_{aa}. The choice of a power-law mobility is related to the charge-transport through localized states that have exponential density-of-states. By applying modified carrier mobility in the derivation (not discussed here) of current-voltage equations of OFETs, the final current-voltage equation is given as:

$$I = \frac{W}{L}\frac{\mu_0}{{V_{aa}}^{\gamma}} C_{OX} \frac{[f(V_G,V_D)]^{\gamma+2}-[f(V_G,V_S)]^{\gamma+2}}{\gamma+2}(1+\lambda|V_D-V_S|) \qquad (7)$$

where λ is the channel length modulation parameter, and the effective gate overdrive function is given by:

$$f(V_G,V) = V_{SS} ln\left\{1+e\left[-\frac{(V_G-V_T)-V}{V_{SS}}\right]\right\} \qquad (8)$$

where V_{SS} is the subthreshold voltage.

Theories used in these models are based on charge drift in the presence of tail-distributed traps (TDTs) [29] and variable range hopping (VRH) [30]. TDTs assumes a significant portion of charge is localized in the exponential tail, and the mobile charge attributed to the conduction or the valence band is only a portion of the total charge, and the effective mobility becomes proportional to the ratio of the free-to-trapped charge. VRH does not separate between free and localized charges, and excess charge is induced in the states by the gate bias voltage in terms of Gauss' law. Therefore, both theories define the dependence of mobility on gate bias voltage.

1.2.5 OFET geometry

As shown in Figure 4, OFETs can be realized in two main geometries: bottom- and top-gate geometries. In the so-called bottom-gate geometry the OFET is comprised of a gate electrode at the bottom of a transistor on top of which is a gate dielectric layer, an organic semiconductor layer, and source/drain electrodes. In the top-gate geometry the OFET is comprised of source/drain electrodes at the bottom, an organic semiconductor layer on top, a gate dielectric layer, and a gate electrode. The bottom-gate OFET geometry is the most commonly used, in part because it prevents potential damage to the organic semiconductor layer that may occur if a gate dielectric is solution-processed onto it [31]. However, bottom-gate OFETs have an organic semiconductor layer exposed to the environment, which often leads to reduced environmental and operational stability. To improve the stability of bottom-gate OFETs in air or harsher environments such as high temperature and humidity, either an environmental barrier layer [32] that protects the organic semiconductor layer or a stable organic semiconductor layer [33] that can withhold damage from the environment must be used.

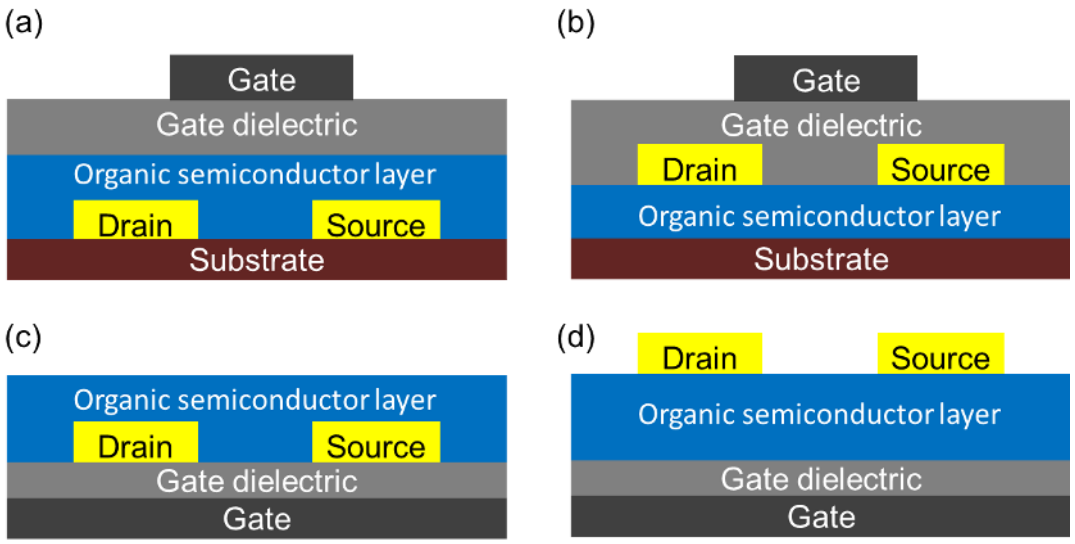


Figure 4. OFET geometry: (a) Top-gate bottom-contact. (b) Top-gate top-contact. (c) Bottom-gate bottom-contact. (d) Bottom-gate top-contact.

In contrast to bottom-gate OFETs, top-gate OFETs, in which a gate dielectric is deposited on top of the organic semiconductor layer, can improve environmental stability in air or harsher environments without an extra protection layer. To prevent damage to the organic semiconductor layer when gate dielectric forming on top of it, fluorinated polymers such as CYTOP have been used. CYTOP is highly chemically stable and hydrophobic, and it dissolves in fluorinated solvents that will not dissolve most organic semiconductor materials. In Hwang *et al.*, top-gate OFETs with a bilayer CYTOP/Al_2O_3 gate dielectric have shown high environmental and operational stability in air for over two years and under oxygen plasma treatment for five min at 750 W [34]. These OFETs also have displayed recoverable performance on μ and V_{TH} after systematic investigation under exposure to air, oxygen plasma, and water immersion [35].

An important feature of OFET geometries are substrates. The conventional substrates of OFETs and organic electronics are rigid materials such as Si and glass substrates. However, flexible, foldable, and even renewable substrates have been

developed for various applications and purposes. Among these substrates, paper is the preferred substrate because it is low-cost, recyclable, and produced from natural feedstock [36] (i.e., it is derived from trees). However, paper is porous, introducing a challenge for solution-based fabrication of organic electronics on top of it; and compared to glass or plastic, this substrate limits the performance of organic electronics. In contrast to traditional cellulosic material such as paper, cellulose nanocrystal (CNC), an emerging material also derived from trees, has been an attractive new material because it can be processed into freestanding films with low surface roughness, good transparency, a low coefficient of thermal expansion, and high thermal stability [37]. Several reports have demonstrated that the performance of organic electronic devices such as OPVs [38, 39] and OLEDs [40] on CNC substrates is comparable to the performance of such devices on glass or plastic substrates.

1.3 Organization of this dissertation

Chapter 1 introduces printed electronics and OFETs, and Chapter 2 describes the experimental methodology including details of OFET fabrication and equipment used for that. Chapter 3 describes stable low-voltage operation top-gate OFETs on CNC:glycerol. Chapter 4 describes top-gate OFETs using modified bilayer gate dielectric with comparable performance to achieve better environmental stability. Chapter 5 describes a method to reduce contact resistance of OFETs. Chapter 6 describes OFETs on paper. Chapter 7 provides conclusions and future work.

CHAPTER 2

EXPERIMENTAL METHODOLOGY

2.1 Device fabrication

This chapter describes fabrication and measurements for OFETs and capacitors. In the first part of this chapter, an overview will introduce process details of organic electronics, and the differences with conventional lithography will be described; evaporation methods will also be introduced such as e-beam evaporation, thermal evaporation, and atomic layer deposition. In the second part of this chapter, OFET measurements, the measurement system and frequently used characterization will be described. In the third part of this chapter, capacitor measurements will be described.

2.1.1 Overview

For organic device fabrication, additive process is widely used because organic materials usually cannot survive in conventional semiconductor processes such as solvent cleaning, wet/dry etching, chemicals for lithography, etc. In the process used in this dissertation, glass substrates for OFET fabrication were only cleaned at the beginning of the fabrication; for novel substrates other than glass, the cleaning step was skipped to avoid potential damages on substrates. The cleaning steps consisted of putting glass substrates in acetone, distilled water, and isopropanol in a sonicator for five min in each step. The set-up for the cleaning process is shown in Figure 5. After substrate cleaning, source/drain electrodes were patterned through shadow masks. The source/drain electrodes were evaporated by either e-beam evaporation or thermal evaporation. A picture of shadow masks is shown in Figure 6. With shadow masks attached on

substrates, metal was only deposited on the open area. After source/drain electrode deposition, contact treatment can be applied at this stage to decrease the energy barrier between an organic semiconductor layer and source/drain electrodes. On top of the source/drain electrodes was the organic semiconductor layer. The preparation of semiconductor layers in this study used spin-coating and then annealing of the organic semiconductor layer.

Figure 5. A Branson sonicator for substrate cleaning.

The organic semiconductor layer was followed by a bilayer gate dielectric layer. The bilayer gate dielectric layer was comprised of a spin-coated and annealed polymer dielectric, CYTOP, and a metal-oxide dielectric layer deposited by atomic layer deposition (ALD) at 110 °C. The last step was the gate electrode deposition on top of the gate dielectric. The gate electrodes were deposited by thermal evaporation because e-beam evaporation may damage the organic semiconductor layer. Patterning of gate electrodes was also done by shadow masks.

For capacitor fabrication, everything was the same except for the organic semiconductor layer. The purpose of capacitor fabrication was to measure the capacitance

density of the OFET gate dielectric layer and to evaluate the quality of the gate dielectric layer. Therefore, layers of structure from the bottom to the top were bottom electrodes, bilayer gate dielectric, and top electrodes. Electrodes were patterned through shadow masks and bilayer dielectric was first spin-coated and then deposited by ALD.

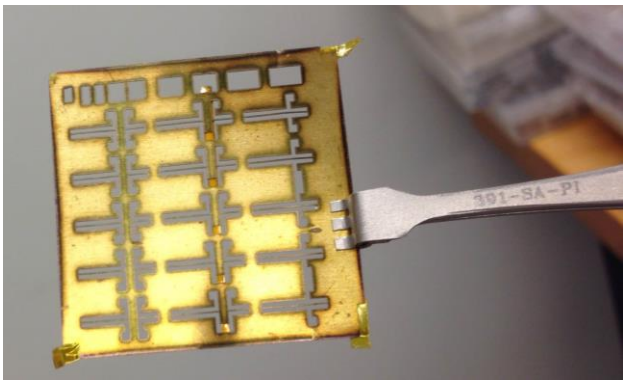


Figure 6. A shadow mask for source and drain electrodes of OFETs.

2.1.2 Electron beam evaporation

The electron beam (e-beam) evaporator used in this study for source/drain electrode deposition was a Denton Explorer. An e-beam system uses high voltage (kV) electron beam to bombard materials under high vacuum (10^{-5} to 10^{-7} torr) with a water cooling system underneath the source pocket [41]. The electron beam is generated by an electron gun using the thermionic emission of electrons produced by an incandescent filament. The direction of the electron beam is controlled by a magnetic field. Materials are heated up to the melting point for evaporation by the bombardment. During the deposition process, the material is heated regionally only at the area bombarded by electron beam, and the rest of the source is still solid. Therefore, this method is more sufficient, applicable for high melting point metals and oxides compounds, and creates less contamination. However, X-rays generated during the electron beam hitting the sources may cause device damage. That is the reason that the e-beam system is only used

for source/drain electrode fabrication before the formation of the organic semiconductor layer. A schematic of an e-beam system is shown in Figure 7.

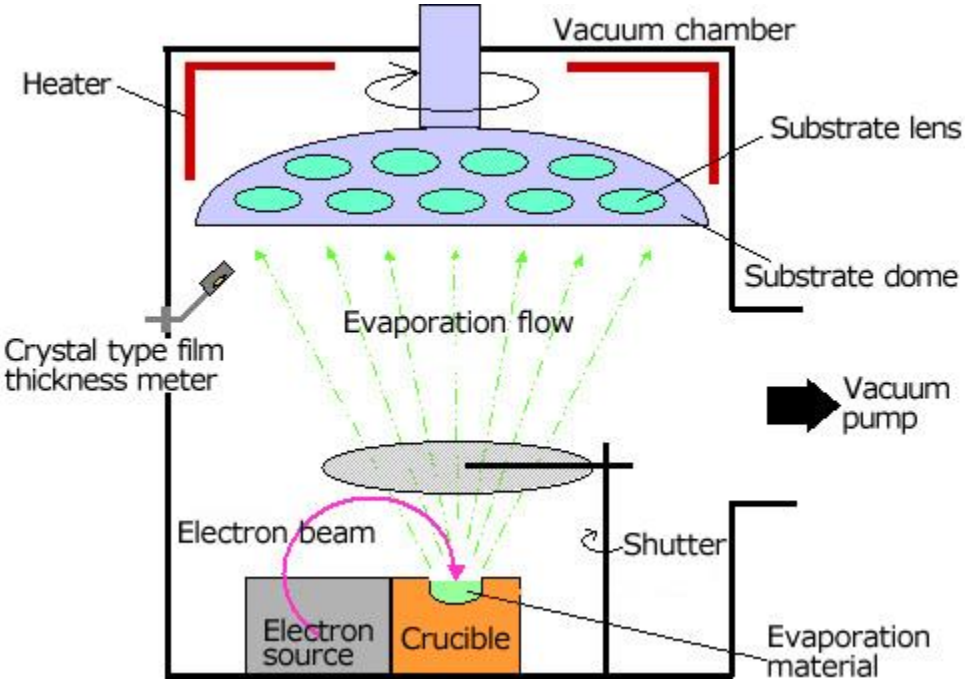


Figure 7. A schematic of e-beam evaporator system (JEOL Ltd.) [42].

2.1.3 Thermal evaporation

The thermal evaporation system used in this study is a SPECTROS 200 system from Kurt J. Lesker. It is connected to an MBraun glovebox avoiding exposure to the atmosphere. Typical vacuum condition of the deposition is below 10^{-7} torr. Thermal evaporation is a resistive heating technique using a tungsten boat carrying a material [41]. The material is heated by the heat generated from injecting current through the tungsten boat. After the material reaches its melting point, it vaporizes and deposits on targeted samples. The advantage of this technique is that it won't generate X-rays during the deposition, so it will not cause potential damage to devices. Therefore, thermal evaporation can be used in not only source/drain electrode deposition, but also for the deposition of the gate electrode after organic material formation on the organic electronic

devices. However, it cannot use high melting point materials because heating up the whole tungsten boat is not efficient for raising the temperature above 1000 °C, and potential contamination is a possibility because parts other than the materials are also heated. A schematic of a thermal evaporation system is shown in Figure 8.

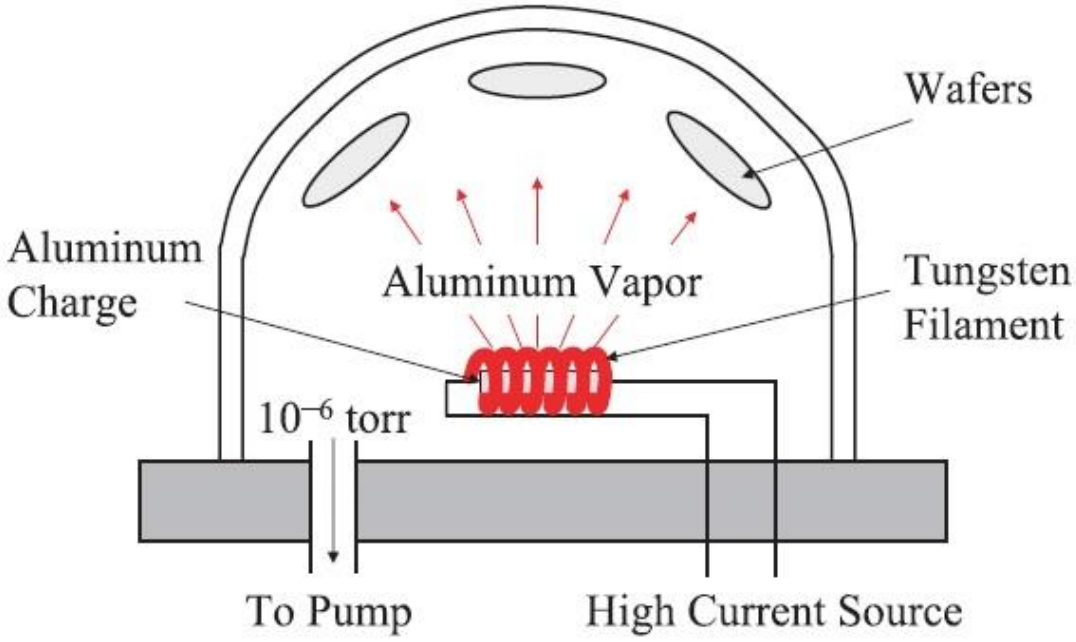


Figure 8. A schematic of thermal evaporator [41].

2.1.4 Atomic layer deposition

The atomic layer deposition (ALD) system used here is a Savannah S200 ALD from Ultratech Inc. (Cambridge NanoTech Inc.) ALD provides precise control down to the atomic scale. The principle of atomic layer deposition is similar to chemical vapor deposition (CVD) except the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction [41]. The sequence of ALD starts from a pulse of water vapor and then a pulse of a metal-organic precursor. An example of ALD for Al_2O_3 deposition is shown in Figure 9. A layer of Al_2O_3 forms as

described: In the pulse of water vapor, water adsorbs on the substrate surface and then forms a hydroxyl group (Figure 9 (a)); another pulse of precursor, in this case trimethyl aluminum ($Al(CH_3)_3$), flows in and interacts with the hydroxyl group to have bonding between an oxygen atom and an aluminum atom, and a methyl group forms a bonding with hydrogen from a hydroxyl group to yield a by-product, methane (Figure 9 (b)). After a layer of Al_2O_3 forms, another pulse of water vapor is introduced (Figure 9 (c)), this time water adsorbs on aluminum atoms, and oxygen atoms bonded with aluminum atoms replace all methyl groups connected to aluminum (Figure 9 (d)). Repeated cycles work as described above to form a dielectric.

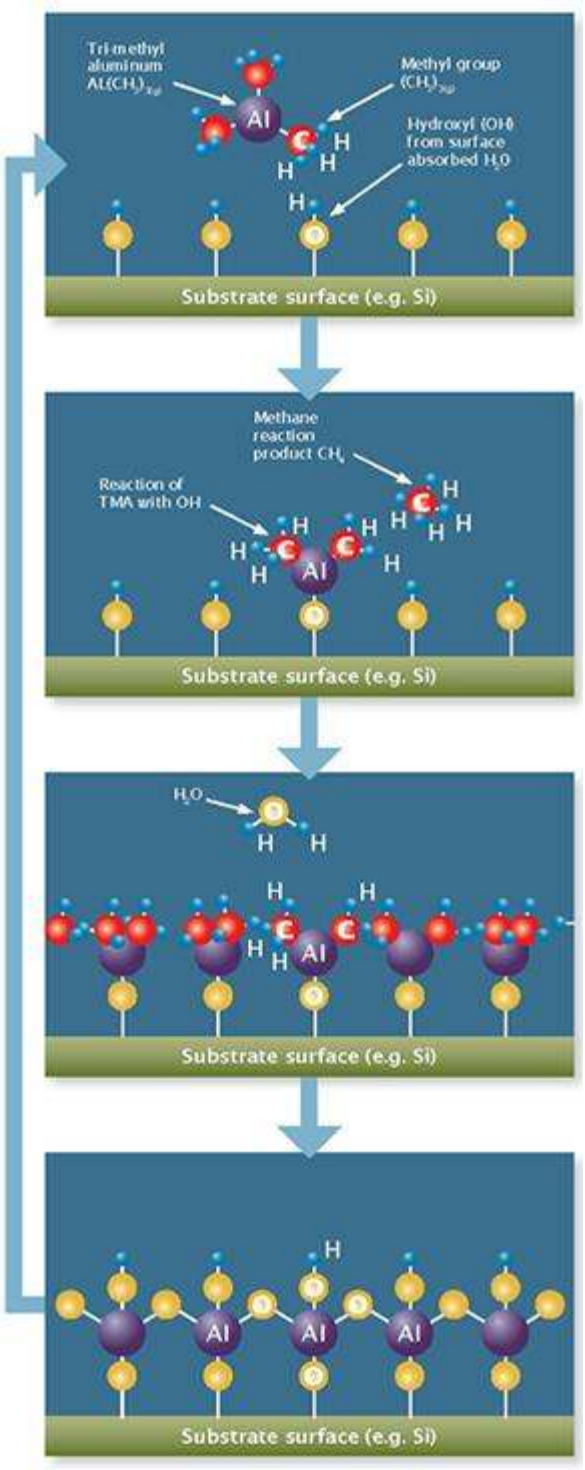


Figure 9. An illustration of ALD process of Al_2O_3 (Ultratech Inc.) [43].

2.2 OFET measurements

The measurement set-up of OFET characterization uses a Signatone probe station in a MBraun glovebox. The probe station is connected to an Agilent E5272A system for electrical characterization and to an Agilent 4284A for capacitance characterization. Agilent systems are connected to a computer for remote control by LabVIEW programs. A picture of this measurement set-up is shown as Figure 10.

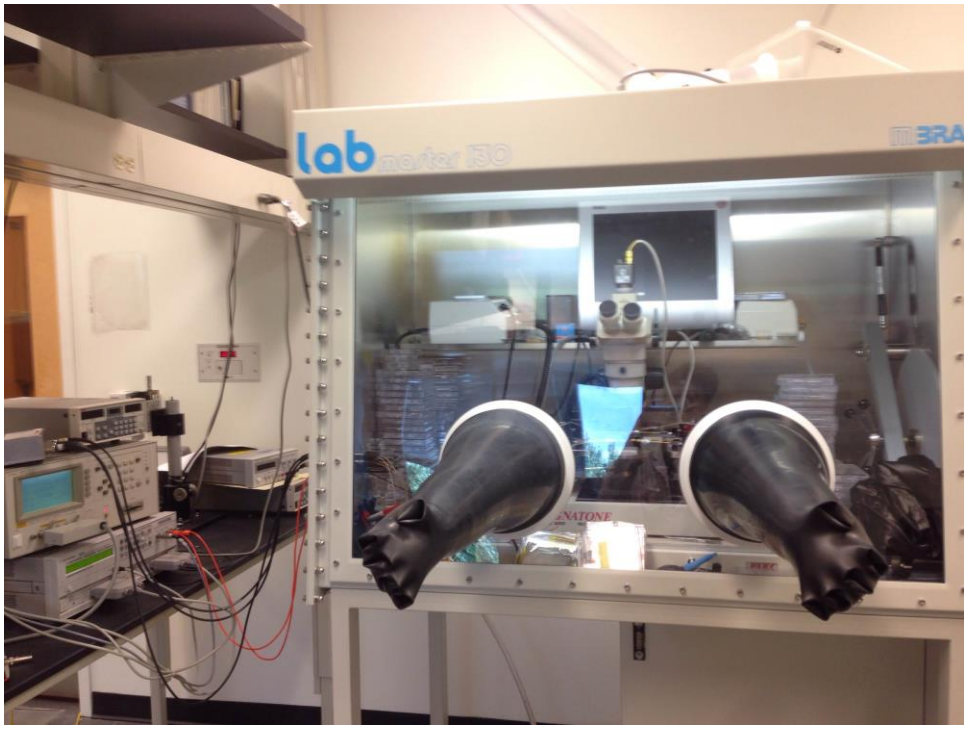


Figure 10. The OFET characterization set-up.

Characterization of OFETs used in this study includes transfer characteristics, output characteristics, DC bias stress measurements, and repeated scans of transfer characteristics.

2.2.1 Transfer characteristics

The transfer characteristics are drain-to-source current as a function of gate voltage at a certain drain-to-gate voltage. An example is shown in Figure 11. OFETs are

usually measured from off-state (low gate voltage) to on-state (high gate voltage) then on-state to off-state to observe if fabricated OFETs have hysteresis, and the quality of OFETs can be determined. The carrier mobility can be extracted by putting the slope of the linear fitting of the square root of drain current as a function of gate voltage into Equation (2). From the same linear fitting, the threshold voltage can be extracted by the intercept of the gate voltage axis. The on/off current ratio can be extracted by dividing on-state drain current by off-state drain current.

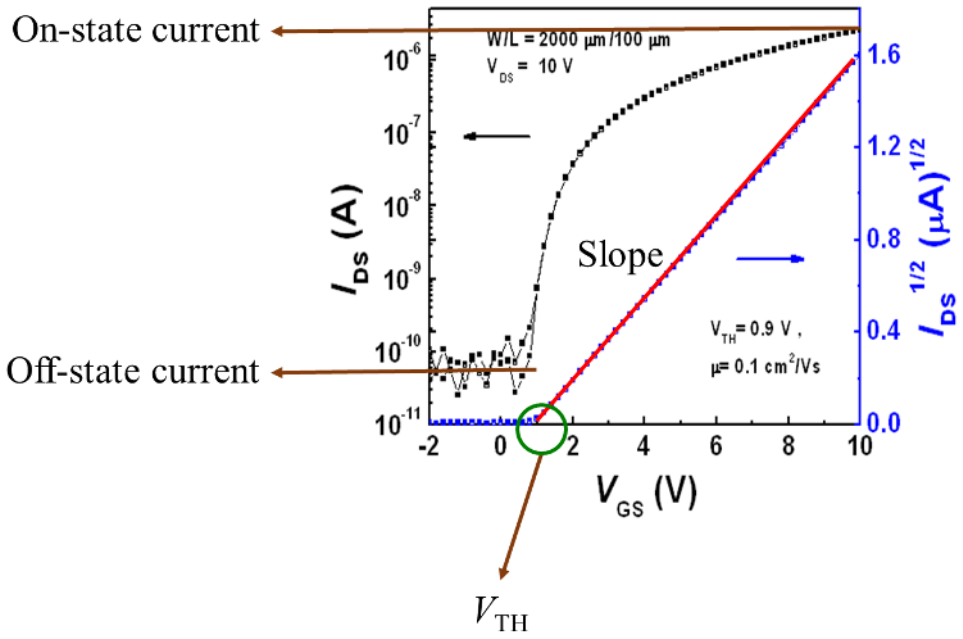


Figure 11. An example of transfer characteristics.

2.2.2 Output characteristics

The output characteristics are drain-to-source current as a function of drain-to-source voltage at different gate-to-source voltage. An example is given in Figure 12. From this plot, on-resistance can be extracted by the slope of tangents from each curve at a given drain-to-source voltage as described in Equation (3). With different channel widths at a channel length, different on-resistance changes linearly with different channel

widths. The intercept of resistance when channel width equals to zero represents the sum of the contact resistance of a source and a drain.

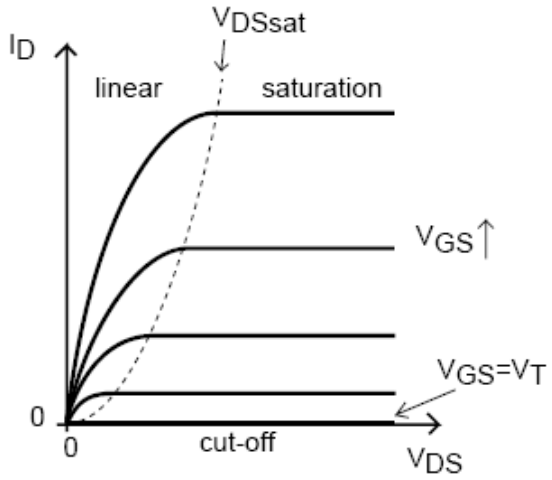


Figure 12. An example of output characteristics.

2.2.3 DC bias stress

The DC bias stress test here is to monitor the drain-to-source current variation at on-state. It is an indicator of the operational stability of OFETs. An example of this characteristic is shown in Figure 13.

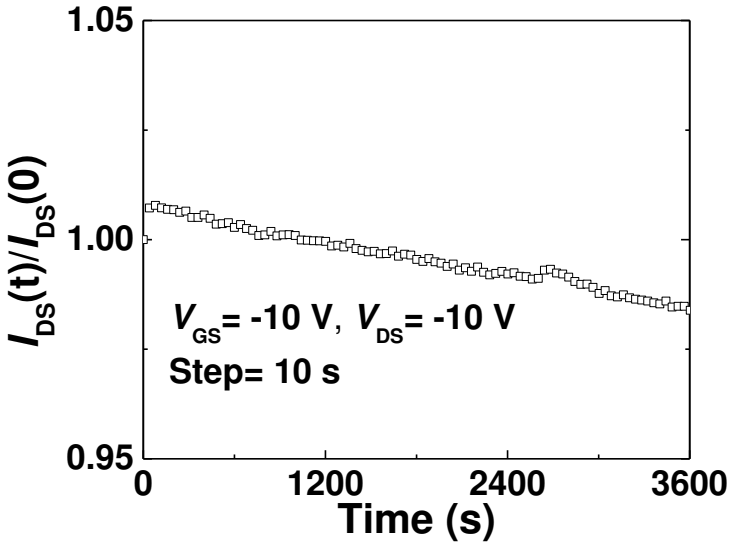


Figure 13. An example of DC bias stress of an OFET at on-state.

2.2.4 Repeated transfer characteristics

The repeated transfer characteristic is another indicator of operational stability of OFETs. It is usually conducted continuously from off-state to on-state to observe if OFETs are stable or degraded during repeated scans.

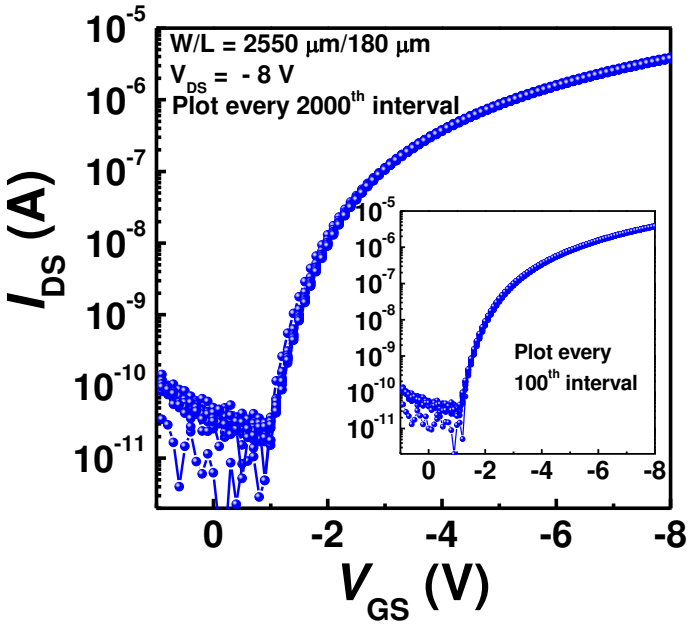


Figure 14. An example of repeated transfer characteristics.

2.3 Capacitor measurements

To investigate the quality of capacitors, there are four frequently used measurements to evaluate capacitors. The first measurement is to measure capacitance as a function of applied DC voltage at several given frequencies as shown in Figure 15. In this case, the stability of capacitance will be evaluated at a range of DC biases with several given frequencies.

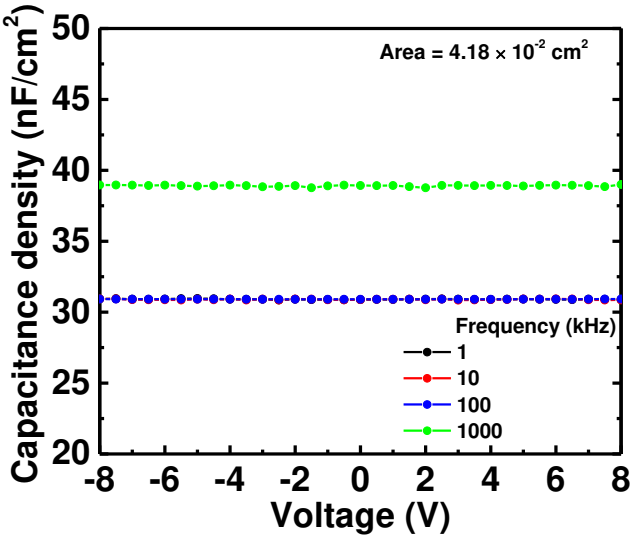


Figure 15. An example of measured capacitance at different frequencies under a range of applied DC voltages.

In Figure 16, the second measurement is to measure capacitance as a function of frequency at zero bias. In this case, the quality of a capacitor will be evaluated because the capacitance is usually unstable at high frequency.

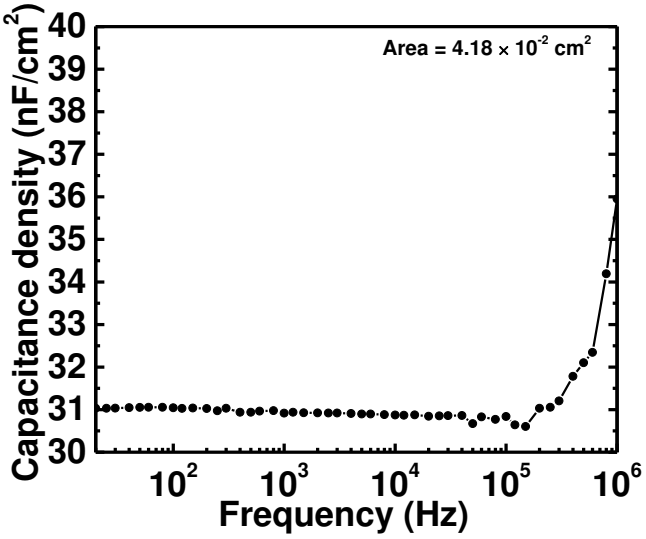


Figure 16. An example of measured capacitance as a function of frequency at zero bias.

In Figure 17, the third measurement is to measure capacitors with various areas at a given frequency and a given bias. In this case, capacitance will be in a linear relation

with areas of capacitors, and the slope of this linear relation is capacitance density. With this value extracted, carrier mobility can be calculated through Equation (3) in page 6.

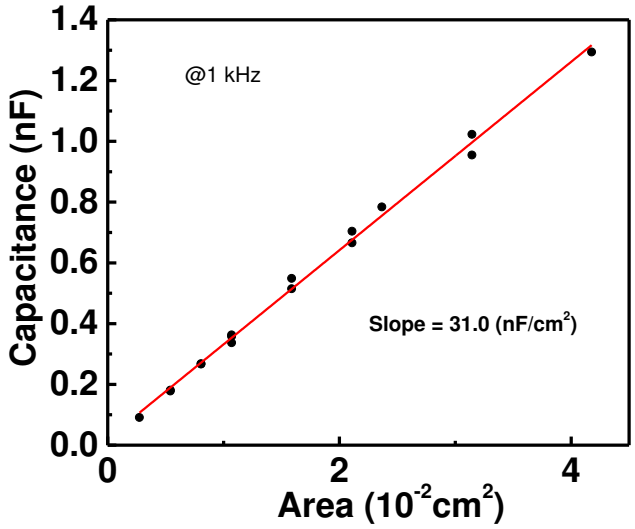


Figure 17. An example of capacitance measured at different areas.

In Figure 18, the last measurement is the current density of a capacitor as a function of applied electric field. It provides a direct observation on a capacitor for its breakdown electric field which is an indicator of the quality of a dielectric.

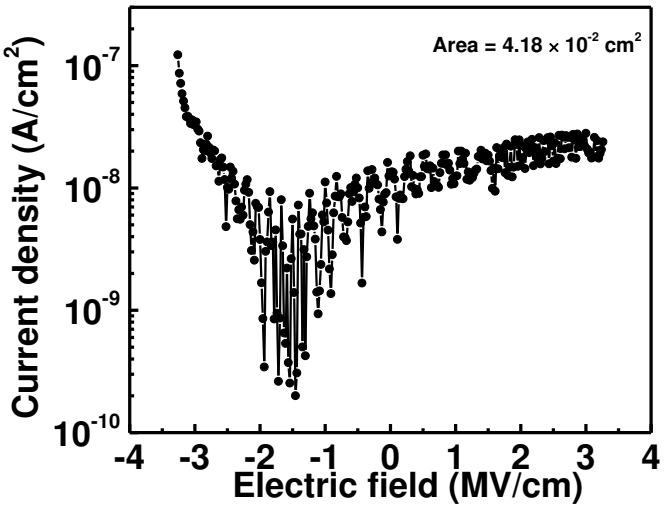


Figure 18. An example of the vertical breakdown field measurement for a capacitor.

CHAPTER 3

OFETS ON CELLULOSE NANOCRYSTAL SUBSTRATES

3.1 Introduction

OFETs have the potential for low-cost fabrication and flexibility over large areas which make them important building blocks for the development of flexible electronic applications. With growing awareness of the environmental impact of electronic waste, there is a need for new substrates for emerging flexible organic printed electronic technologies with a small environmental footprint. The replacement of conventional substrates, such as glass and plastic, with substrates made from abundant and environmental-friendly materials can make the recycling and/or disposal of new engineered products potentially more efficient and less polluting. Although OFETs are typically fabricated on glass or plastic substrates, paper would be the preferred substrate [36] because of its low cost, recyclability, and the use of natural materials derived from renewable feedstock. However, the fabrication of electronic components on paper presents several challenges resulting from the high porosity of traditional cellulosic materials, their high surface roughness, and complex surface chemistry. Consequently, performances of OFETs fabricated from solution on paper continue to be limited compared to devices fabricated on glass or plastic substrates.

In recent years, cellulose nanomaterials derived from sustainable feedstock, such as cellulose nanofibers (CNFs) and CNCs, have emerged as an attractive new class of materials for flexible electronic applications because they can be processed into free-standing and flexible films that display low surface roughness, good transparency, a low coefficient of thermal expansion and high thermal stability [37]. Several reports exist on

organic electronic devices such as OFETs [44-48], OPVs [38, 39, 49-51], and OLEDs [40, 52-55] fabricated on cellulose nanomaterial substrates. OFETs fabricated on CNF-based substrates have shown good flexibility and transparency [44, 45], and a majority of studies focused on processes using evaporation [46-48] and ink-jet printing [56, 57]. In addition to be a substrate, cellulose materials were also employed as a gate dielectric [58-62] for OFETs. To date, only a few reports demonstrated stability tests [44] and improvements are still needed in lowering the threshold voltage and increasing carrier mobility using cellulose as a part of the OFETs. Solution-processed OFETs containing cellulose with a low threshold voltage [63] and a high carrier mobility with environmental stability remains a goal to be achieved.

In this chapter, stable low-voltage operation top-gate OFETs are demonstrated. OFETs were fabricated on water soluble CNC:glycerol substrates protected by ALD-grown Al_2O_3. The carrier mobility of fabricated OFETs has an average value of 0.11 cm^2/Vs and a highest value of 0.23 cm^2/Vs. Operational and environmental stability will be demonstrated. For comparison, OFETs on bare CNC:glycerol were also fabricated and measured. The OFETs structure used here was reported by our group [34, 35].

3.2 Design of experiments

The advantage of this recyclable substrate is its water solubility at room temperature. However, it is also its disadvantage because a droplet of water can form a hole on bare CNC:glycerol within seconds as shown in Figure 19 (a). A proposed solution is to deposit a layer of ALD-grown Al_2O_3 on top of CNC:glycerol to protect the substrate, and Figure 19 (b) shows a droplet of water staying on the protected CNC:glycerol without dissolving it to make a hole. After deciding to add a protection

layer for potential damages, the wettability of tetralin, the solvent we used for the organic semiconductor, was verified by conducting contact angle measurements of tetralin on bare CNC:glycerol and CNC:glycerol with ALD-grown Al_2O_3. The results in Figure 20 show that tetralin wets on both CNC:glycerol and CNC:glycerol with ALD-grown Al_2O_3; that confirms the film formation on this novel substrate.

(a) (b)

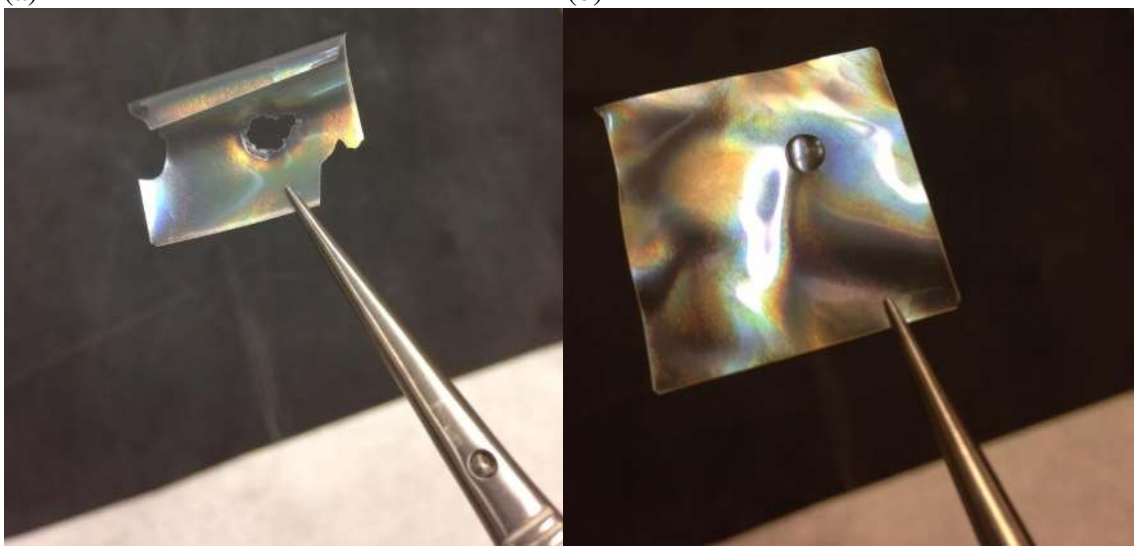


Figure 19. A water droplet on (a) Bare and (b) Al_2O_3 protected CNC:glycerol.

In this section, top-gate OFETs with a bilayer CYTOP/Al_2O_3 gate dielectric will be characterized. These OFETs used a solution-processed semiconductor channel layer made of a blend of TIPS-pentacene and PTAA fabricated on recyclable CNC:glycerol substrates. These OFETs exhibited low operating voltage between 0 to -10 V, low threshold voltage in the range of -2 V, an average field-effect mobility of 0.11 cm^2/Vs, and good shelf and operational stability in ambient. In addition to protecting substrates from solution process, the barrier layer of Al_2O_3 was grown by ALD directly onto the CNC:glycerol substrates, which was also expected to improve the operational stability in ambient air. This same layer was reported contributing stable OFETs in air, therefore it

may protect the organic semiconductor film from moisture and other chemicals that can either permeate through or diffuse out of the substrate.

(a) (b)

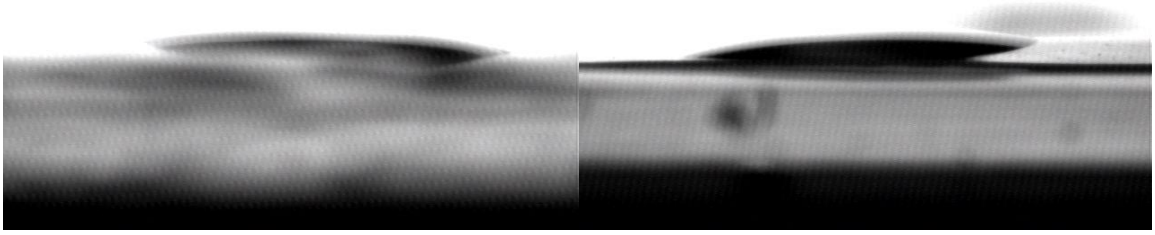


Figure 20. Tetralin on (a) Bare and (b) Al_2O_3 protected CNC:glycerol.

3.3 Device fabrication

OFETs were fabricated in top-gate bottom-contact geometry, as shown in Figure 21. First, CNC:glycerol substrates were prepared as described in Zhou *et. al.* [38]. OFETs fabricated on bare CNC:glycerol substrates, will be referred to hereafter as D1 devices. OFETs fabricated on CNC:glycerol substrates coated with 300 cycles of ALD-grown Al_2O_3 at 110 °C (Savannah 100 ALD system, Cambridge Nanotech Inc.), will be referred to as D2 devices.

D1- and D2-type OFETs were fabricated as follows: a 2 mm-thick layer of PDMS (Gelest OE 41 with 1:1 weight ratio) was cast onto 3.8 cm by 3.8 cm glass substrates to hold the CNC:glycerol substrates. CNC:glycerol substrates were attached on top of the PDMS film and secured by Kapton tape at the edges, and 50 nm-thick Au source/drain electrodes were deposited through a shadow mask using an electron-beam deposition system (Denton Explorer), at a deposition rate of 1.0 Å/s and an initial pressure of 9.0×10^{-7} Torr. A TIPS-pentacene (Sigma Aldrich) and PTAA (Sigma Aldrich) blend solution was used as the organic semiconducting layer. The (1:1 weight ratio) TIPS-

pentacene:PTAA solution was dissolved in anhydrous tetralin, (Sigma Aldrich) at a concentration of 30 mg/ml. The TIPS-pentacene:PTAA blended solution was spin-coated at 500 rpm for 10 s (acceleration of 500 rpm/s) and ramped to 2,000 rpm for 20 s (acceleration of 1,000 rpm/s) to yield a ca. 70 nm-thick layer [64]. Spin coated films were then thermally annealed at 100 °C for 15 min on a hot plate in a N_2-filled glove box. The preparation of a bilayer gate dielectric was starting from diluting CYTOP (Asahi Glass, CTL-809M) with a solvent (Asahi Glass, CTL-SOLV180) to a concentration of 2% by volume.

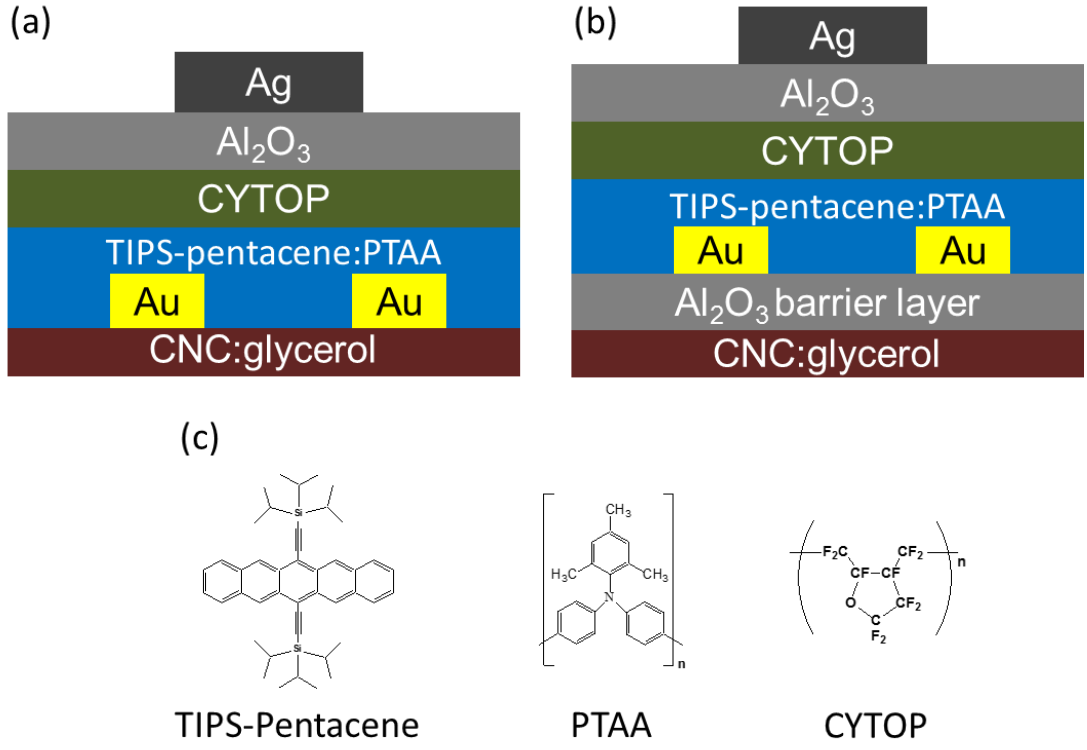


Figure 21. (a) Cross-section of OFETs on bare CNC:glycerol substrates, D1. (b) Cross-section of OFETs on CNC:glycerol substrates with an Al_2O_3 barrier layer, D2. (c) Chemical structures of the compounds and polymers used in the OFETs.

A layer of CYTOP was spin-coated on top of the organic semiconducting layer at 3,000 rpm for 60 s (acceleration of 10,000 rpm/s) to yield a ca. 35 nm-thick layer [64]. Samples were then thermally annealed at 100 °C for 10 min on a hot plate in a N_2-filled

glove box. After that, 500 cycles of ALD-grown Al_2O_3 were deposited at 110 °C to yield a ca. 40 nm-thick layer [64]. Later, 100 nm-thick Ag gate electrodes were deposited through a shadow mask in a thermal evaporator (Kurt J. Lesker, SPECTROS) with initial pressures below 1.0×10^{-6} Torr and at an average deposition rate of 1.0 Å/s.

3.4 Device characterization

D1- and D2-type OFETs were characterized in a N_2-filled glove box (O_2 and H_2O < 0.1 ppm, 25 °C) and at ambient conditions (25 °C and 20% to 40% RH) using an Agilent E5272A source/monitor unit. The operational stability was investigated by performing 1,000 continuous scans of the transfer characteristic and by applying a DC bias stress (V_{GS} = -10 V, V_{DS} = -10 V) for 60 min inside a N_2-filled glove box and at ambient conditions. To investigate environmental stability, devices were stored at ambient conditions and measured periodically over a period of 16 days.

3.4.1 Pristine condition in nitrogen

Figure 22 displays the transfer and output characteristics of representative D1- and D2-type OFETs. Maximum carrier mobility values of 0.13 cm^2/Vs and 0.23 cm^2/Vs were extracted from the transfer characteristics (in the saturation regime) of devices D1 and D2, respectively. Figure 22 also shows the transfer characteristics of the D1- and D2-type OFETs kept in N2 for one month. In the D1 OFET, the carrier mobility decreased to 0.08 cm^2/Vs, while in the D2 OFET the carrier mobility remained unchanged with a value of 0.23 cm^2/Vs. The decreased mobility in the D1 OFET suggests that chemical or physical interactions occur between the substrate and the organic semiconductor. However, these interactions are clearly suppressed in the D2 OFET. The threshold

voltage of D1- and D2-type OFETs does not change more than 0.1 V within this time frame.

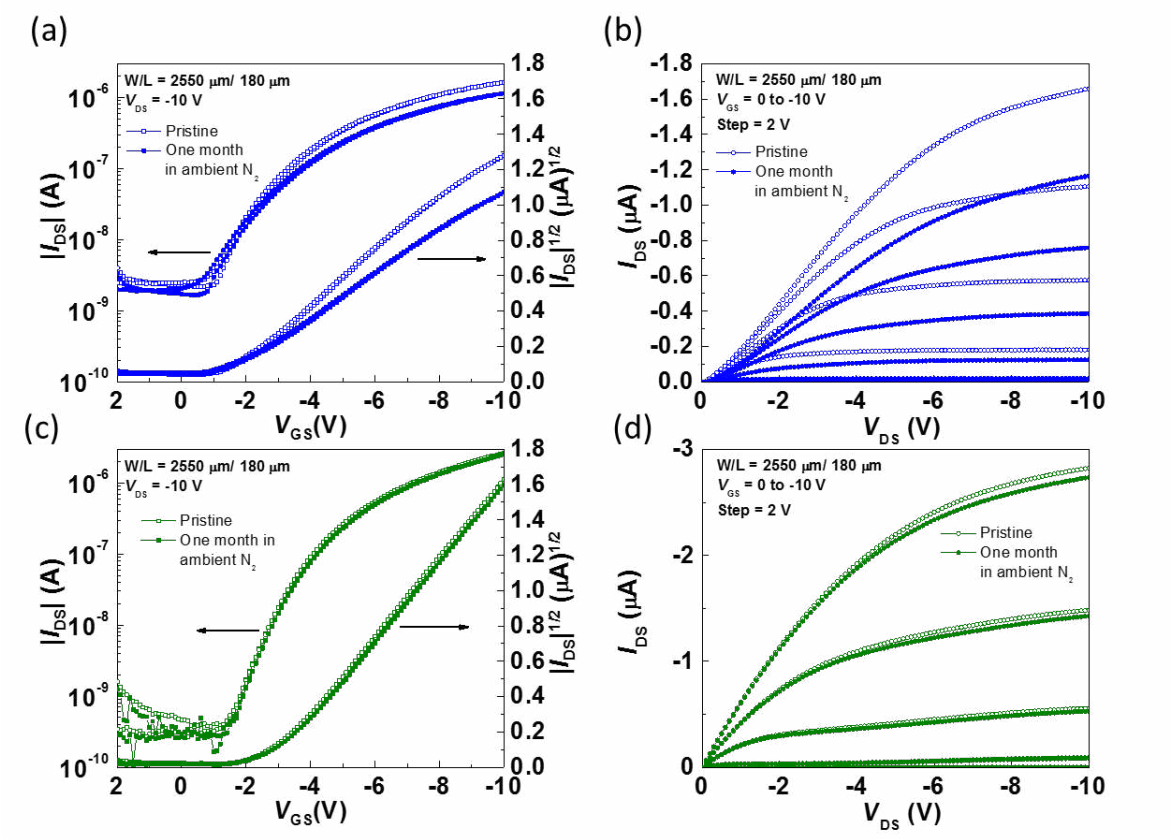


Figure 22. (a) Transfer characteristics of a D1-type OFET before and after one month in N_2. (b) Output characteristics of a D1-type OFET before and after one month in N_2. Larger current with larger $|V_{GS}|$, V_{GS} from 0 to -10 V, the step is 2 V. (c) Transfer characteristics of a D2-type OFET before and after one month in N_2. (d) Output characteristics of a D2-type OFET before and after one month in N_2. Larger current with larger $|V_{GS}|$, V_{GS} from 0 to -10 V, the step is 2 V.

Table I displays average values of carrier mobility μ, average variation of carrier mobility, threshold voltage V_{TH}, and on/off current ratio I_{on}/I_{off} measured on the D1- and D2-type OFETs with labeled dimensions and yield at pristine condition in N_2, storing in N_2 for one month, and storing in ambient for 6 days on D1-tpye OFETs and 16 days on D2-type OFETs.

Label	Barrier layer	Measurement time	W/L	C_{in} (nF/cm^2)	μ (cm^2/Vs)	Ave. % change of μ	V_{th} (V)	I_{ON}/I_{OFF}
D1	None	Pristine in N_2	2550 μm /180 μm Average (6/6 devices)	31.0	0.06 (±0.03)	NA	-1.0 (±0.4)	4.8 x 10^2
		After one month in N_2			0.06 (±0.02)	-7.2	-0.8 (±0.4)	5.8 x 10^2
		6 days at ambient conditions			N/A			
D2	300 cycles of ALD Al_2O_3	Pristine in N_2	2550 μm /180 μm Average (8/8 devices)		0.11 (±0.08)	NA	-2.1 (±0.7)	2.4 x 10^3
		After one month in N_2			0.11 (±0.08)	-2.8	-2.2 (±0.7)	2.7 x 10^3
		16 days at ambient conditions			0.17 (±0.12)	45.1	-0.3 (±0.4)	2.2 x 10^2

Table I. Device dimensions, average mobility, average threshold voltage, and average on/off current ratio of OFETs.

To identify the interactions between the substrate and the organic semiconductor layer, we conducted X-ray photoelectron spectroscopy (XPS) measurements on bare CNC:glycerol substrates (D1') and CNC:glycerol substrates with an ALD-grown Al_2O_3 barrier layer (D2'). Figure 23 displays the binding energy spectra measured by XPS, wherein clear differences are observed between the spectra obtained for the two substrates. First, Al2p and Al2s peaks are detected on D2' because of the Al_2O_3 barrier layer deposited by ALD. More notably, sulfur and sodium peaks are detected on D1', but not on D2'.

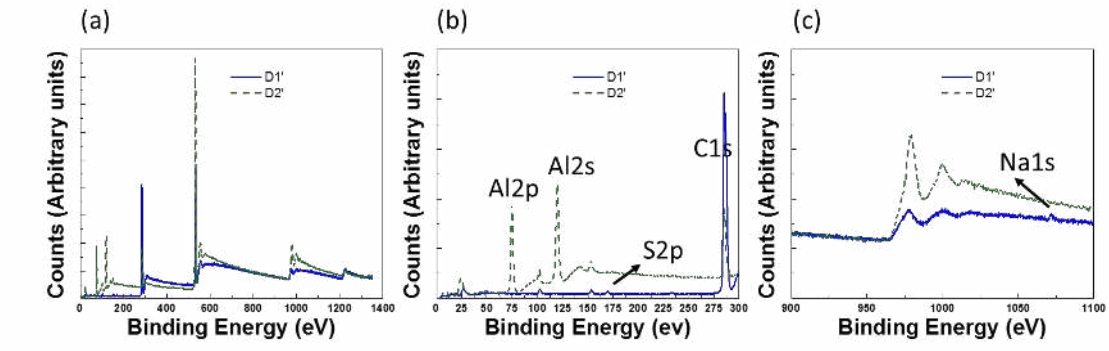


Figure 23. Binding energy spectra from XPS of a bare CNC:glycerol (D1') substrate and a CNC:glycerol (D2') substrate with ALD-grown Al_2O_3. (a) Binding energy from 0 to 1,400 eV. (b) Zoomed-in 0 to 300 eV region of binding energy. (c) Zoomed-in 900 to 1,100 eV region of binding energy.

The presence of sulfur suggests that sulfate half-esters are on the surface of the CNCs:glycerol substrates as a result of the sulfuric acid hydrolysis process used for the CNC production. Sulfate half-esters hydrolyzed by water during casting of the CNC:glycerol film could produce negatively charged sulfates that would act as hole traps, which may explain the decreased mobility values observed in D1 devices after being stored in N_2 for one month, as shown in Figure 22, thus eliminating the possibility that these effects could be caused by oxygen or water from the ambient. In contrast, the mobility displayed by D2 devices stored under the same conditions remained unchanged, as shown in Figure 22. On the other hand, the presence of sodium on the surface of the CNC:glycerol substrate suggests the presence of sodium cations which may be very mobile and could lead to an increased channel conductivity. However, in pristine devices, the off current in both types of devices originates from the gate-to-drain leakage current as displayed in Figure 24 (a) and (c). The slightly larger value of gate-to-drain leakage current in D1 devices therefore indicates that the quality of the bilayer gate-dielectric and the semiconductor layer is affected by the direct fabrication of top-gate OFETs on bare CNC:glycerol substrates. The presence of sodium is an unintended consequence of the addition of glycerol to the CNC films, which improves its mechanical properties. Furthermore, we have to keep in mind that glycerol is a dipolar molecule which may be mobile, and as such, could affect the threshold voltage values [65] and operational stability of devices directly fabricated on CNC:glycerol substrates. In summary, the improved shelf stability, under N_2, and performance characteristics displayed by D2 devices, as compared to D1 devices, arises from the passivation of the chemical species present on the CNC:glycerol surface that results from the deposition of the Al_2O_3 barrier

layer. In the following discussion, we will show that the presence of this passivation layer has further consequences for the environmental and operational reliability of top-gate OFETs.

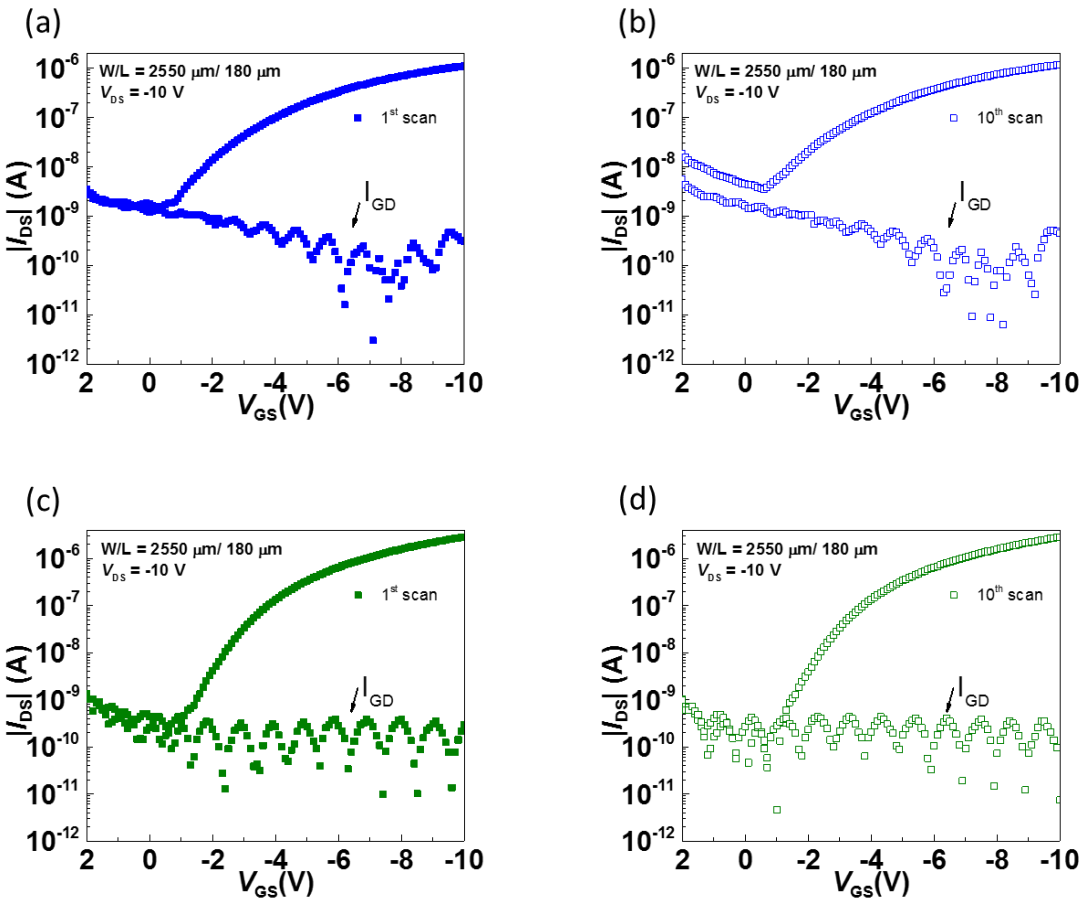


Figure 24. (a) Transfer characteristics and the gate leakage of the D1-type OFET at first scan. (b) Transfer characteristics and the gate leakage of the D1-type OFET at tenth scan. (c) Transfer characteristics and the gate leakage of the D2-type OFET at first scan. (d) Transfer characteristics and the gate leakage of the D2-type OFET at tenth scan.

3.4.2 Operational stability in nitrogen and air

Figure 25 displays the results of scanning 1,000 times of transfer characteristics on both the D1- and D2-type OFETs inside a N_2-filled glove box and at ambient conditions. D1 devices display two distinctive effects in both environments: 1) a reduction in the magnitude of the threshold voltage and 2) an increased off-current. As

displayed on Figure 24 (b), the increased off-current is not attributed to an increased gate-to-drain leakage current but to an increased channel conductivity which probably arises from the diffusion of sodium cations upon device operation. On D2 devices, the off-current increase is greatly suppressed, particularly in air, and variations of the transfer characteristics are primarily associated with smaller reductions in the magnitude of the threshold voltage than the ones observed in D1 devices. Hence, the presence of the Al_2O_3 barrier layer prevents the increase of the channel conductance and leads to more stable transfer characteristics on D2 devices than on D1 devices, in both N_2 and ambient conditions. This can be seen from the summary of extracted carrier mobility, threshold voltage, and on-off current ratio in Figure 26.

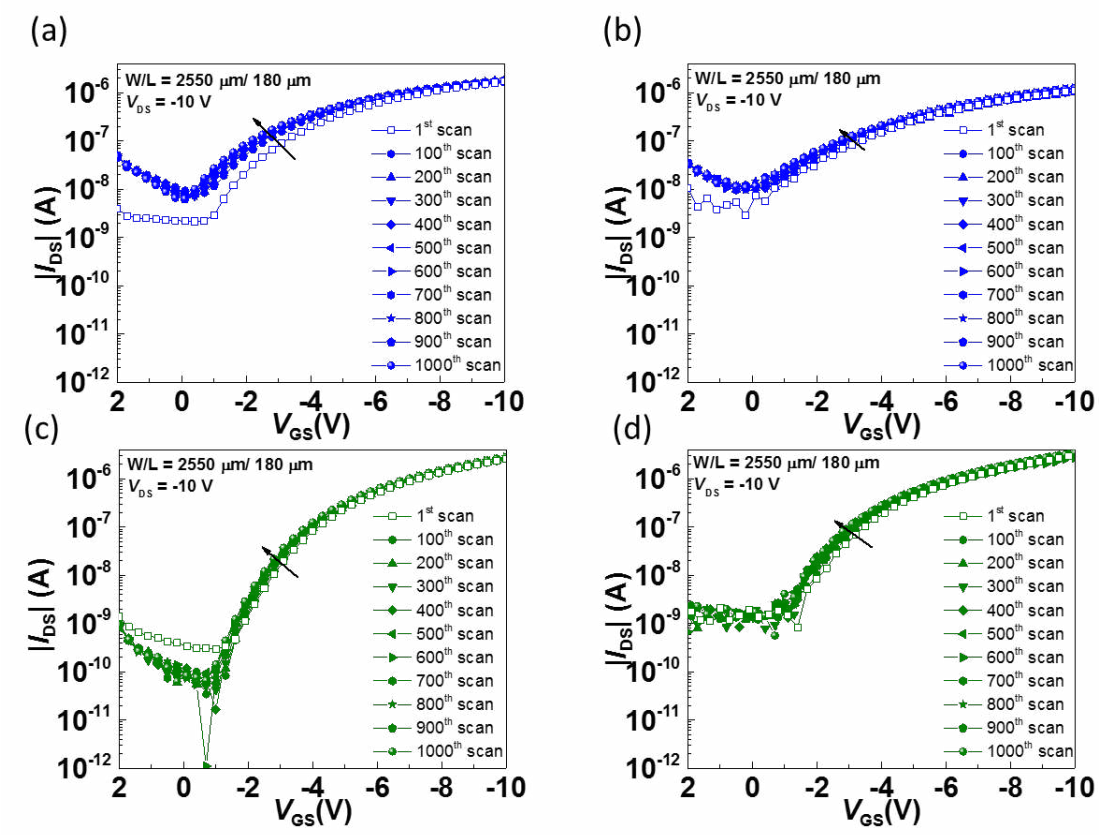


Figure 25. (a) 1,000 cycles of transfer characteristics measured in N_2 on the D1-type OFET. (b) 1,000 cycles of transfer characteristic measured at ambient conditions on the D1-type OFET. (c) 1,000 cycles of transfer characteristics measured in N_2 on the D2-type OFET. (d) 1,000 cycles of transfer characteristics measured at ambient conditions on the D2-type OFET.

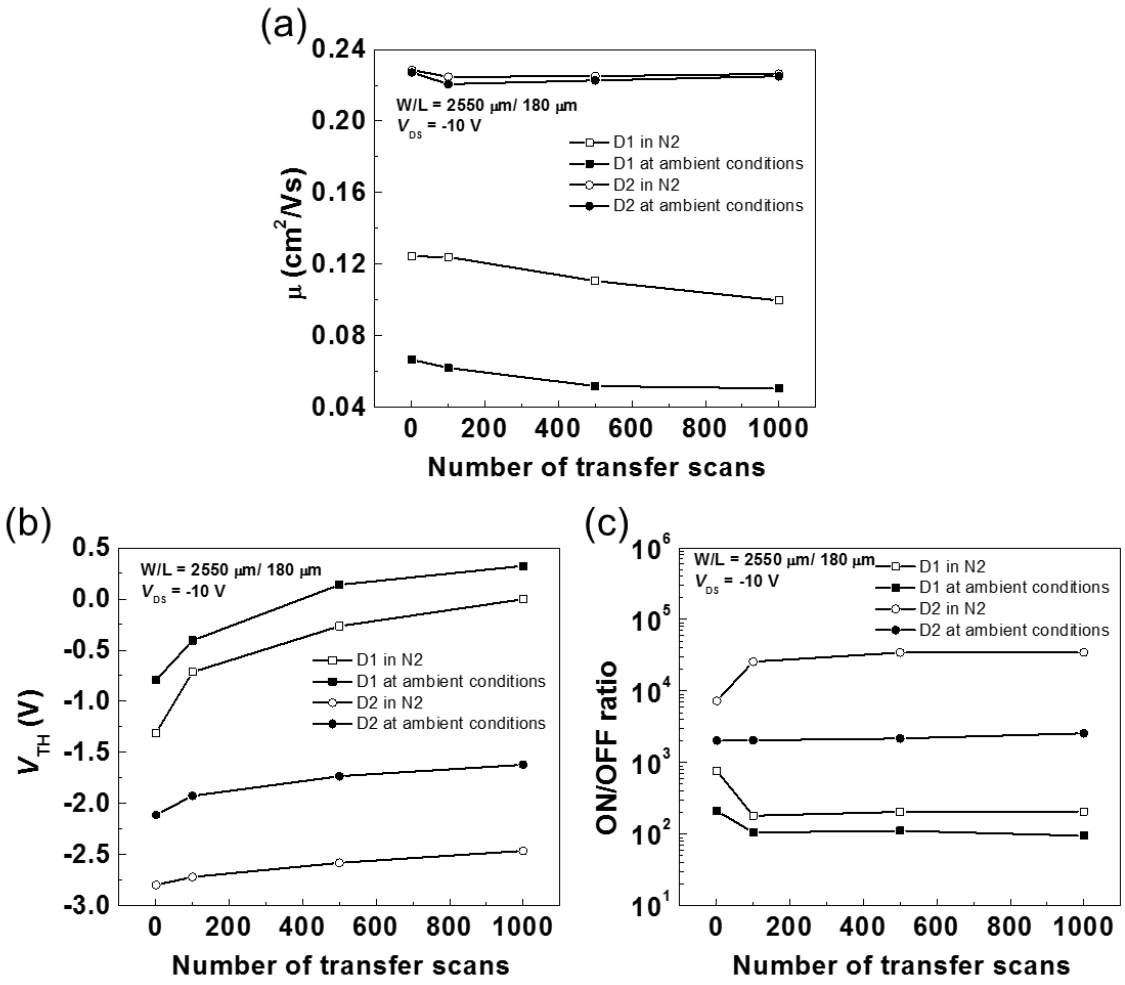


Figure 26. Extracted parameter values from measurements at ambient conditions after storing in N_2 for one month. (a) Mobility. (b) Threshold voltage. (c) On/off current ratio.

To further investigate the operational stability of D1- and D2-type OFETs in N_2 and ambient conditions, DC bias stress tests were also carried on the same devices for 1h. V_{DS} and V_{GS} were both biased at -10 V. Figure 27 shows that after 1 h of biasing under these conditions, the source-to-drain current of both devices increased. Consistent with the relative reductions in the magnitude of the threshold voltage observed in cycling experiments, D1 devices display a higher increase in the source-to-drain current than D2 devices, in both N_2 and ambient conditions. As we have discussed in the past [34], the

reduction of $|V_{TH}|$ observed is consistent with the presence of mobile dipoles, such as glycerol, which have a stronger effect in D1 devices than in D2 devices.

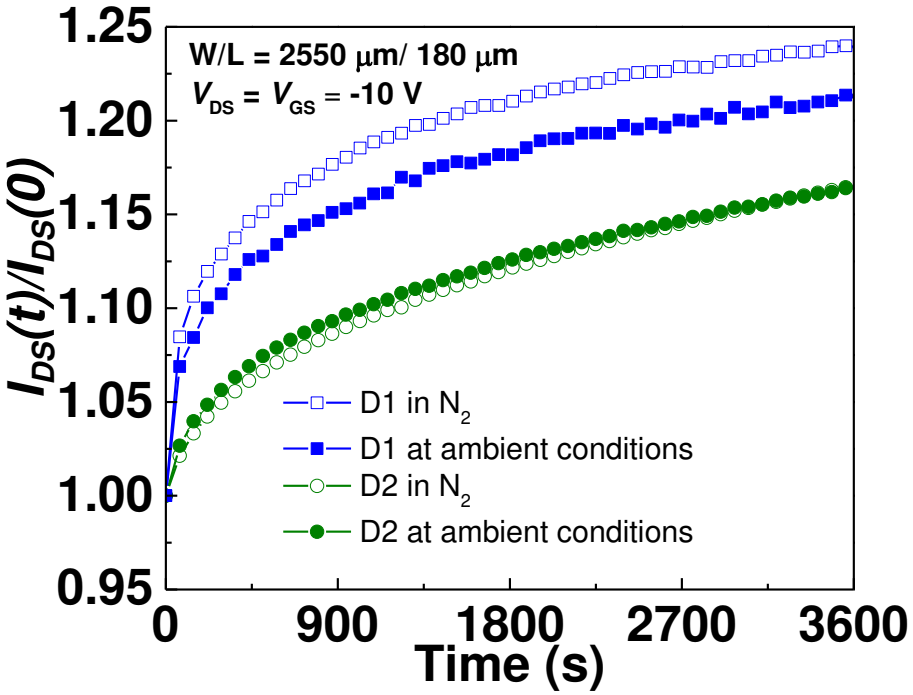


Figure 27. Turn-on DC bias stress measurement measured both in N_2 and at ambient conditions on D1- and D2-type OFETs.

3.4.3 Environmental stability in air

Finally, shelf environmental stability tests of D1 and D2 were conducted. Figure 28 shows electrical characteristics of D1- and D2-type OFETs stored at ambient conditions. The off-current in D1 OFETs increased 1,000 times to the same level as on-current within 6 days. Meanwhile, the off-current of D2 OFETs increased only 100 times after 16 days at ambient conditions. This indicates that the Al_2O_3 barrier layer also improves the shelf environmental stability of OFETs on CNC:glycerol substrates, and provides a route towards optimizing the stability of these types of OFETs. The

performance of D2 devices is comparable to the performance of OFETs with identical geometry fabricated on glass [34, 35] or plastic substrates [66].

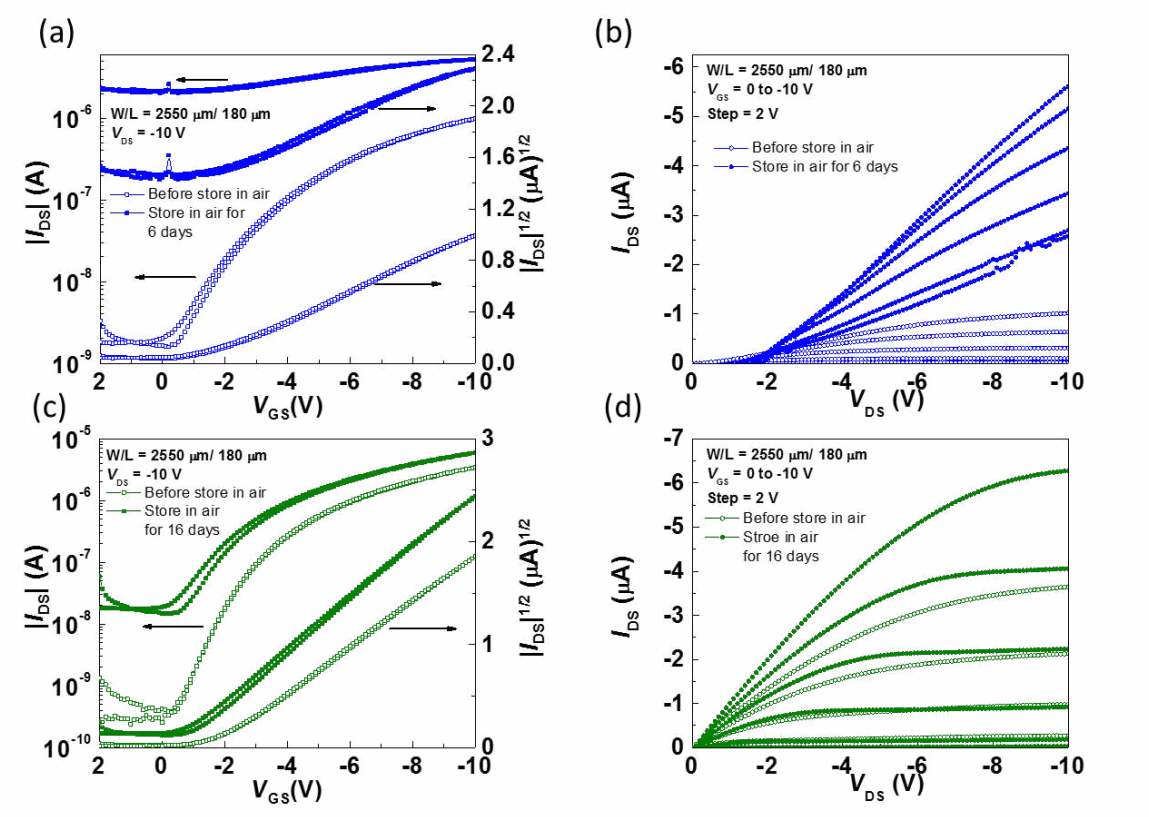


Figure 28. (a) Transfer characteristics of the D1-type OFET before and after storage at ambient conditions for 6 days. (b) Output characteristics of the D1-type OFET before and after storage at ambient conditions for 6 days. (c) Transfer characteristics of the D2-type OFET before and after storage at ambient conditions for 16 days. (d) Output characteristics of the D2-type OFET before and after storage at ambient conditions for 16 days.

3.5 Device modeling

The software for device modeling is Advanced Design System (ADS) from Keysight Technologies, and equation (7) is used to fit the current-voltage characteristics of OFETs. Equation (7) applied here is from Marinov *et. al.* [24, 25] having fitting parameters such as carrier mobility μ, threshold voltage V_{TH}, the characteristics exponent γ, mobility enhancement voltage V_{aa}, subthreshold slope SS, and the channel length modulation parameter λ where μ and V_{TH} were extracted from our experimental data.

Figure 29 displays the fitting of the OFET on base CNC:glycerol substrates shown in Figure 22. Extracted μ and V_{TH} were 0.13 cm^2/Vs and -1.5 V. Fitted SS is 0.74 V/decade, and the corresponding interface trap density, between gate dielectric and organic semiconductor layer, D_{it} calculated by equation (6) is 2×10^{12} cm^{-2}. Empirical parameters such as V_{aa}, γ, and λ are 40 V, 0.11, and 0.03 respectively. The current-voltage characteristics at large gate bias do not follow the model can be explained by the effectiveness of ions from CNC:glycerol substrates found in XPS. These impurities contribute the lower current compared to the model.

(a) (b)

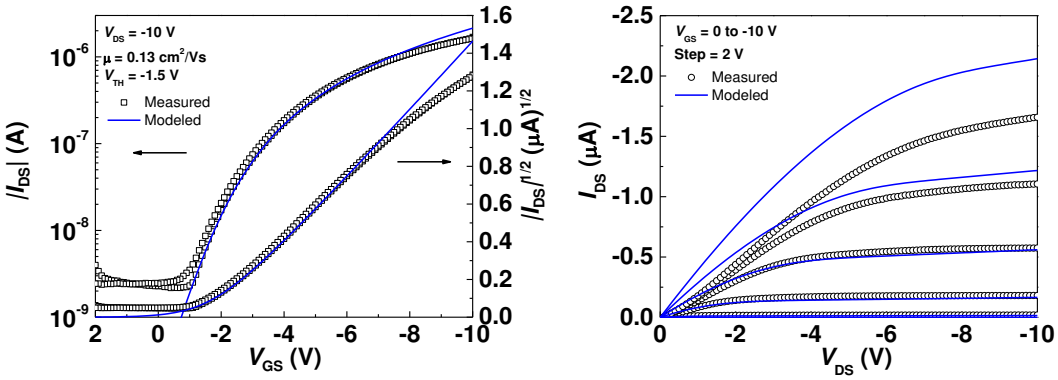


Figure 29. (a) Fitting of transfer characteristics on a D1-type OFET. (b) Fitting of output characteristics on a D1-type OFET.

Meanwhile Figure 30 displays the fitting of the OFET on CNC:glycerol with an ALD-grown Al_2O_3 buffer layer shown in Figure 22. Extracted μ and V_{TH} were 0.23 cm^2/Vs and -2.8 V. Fitted SS is 0.74 V/decade, and the corresponding interface trap density D_{it} calculated by equation (6) is 2×10^{12} cm^{-2}. Empirical parameters such as V_{aa}, γ, and λ are 40 V, 0.11, and 0.039 respectively. The current-voltage characteristics follow the model with similar empirical parameters and support our claim that the buffer/barrier

layer protects organic semiconductor layer by preventing the diffusion of ions from CNC:glycerol substrates.

(a) (b)

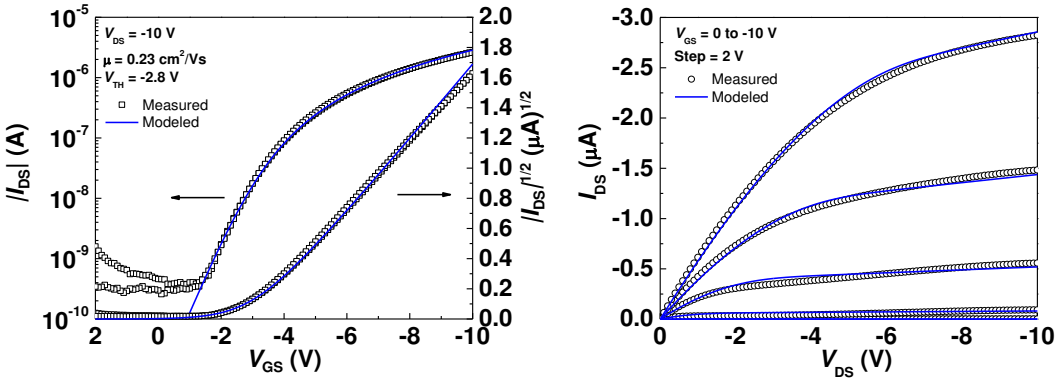


Figure 30. (a) Fitting of transfer characteristics on a D2-type OFET. (b) Fitting of output characteristics on a D2-type OFET.

3.6 Summary

In this section, we have demonstrated top-gate OFETs on CNC:glycerol substrates with a solution-processed semiconductor layer that operates at low voltages with good shelf and operational stability. We have found that the key to achieving top-gate OFETs with stable characteristics is to isolate the organic semiconductor layer from the chemical species in the substrate. We have achieved that by deposition of a thin layer of ALD-grown Al_2O_3, which is also clearly shown to lead to much improved environmental stability. XPS data and device modeling support our assumption. While the thickness and barrier properties of this layer can be further optimized, our results show that such a barrier will be needed to achieve OFETs with stable performance when fabricated on substrates with poor oxygen and water barrier properties.

CHAPTER 4

NANOLAMINATE GATE DIELECTRIC OF OFETS

4.1 Introduction

OFETs could enable flexible displays [67, 68], wearable electronics [69], and sensors [70, 71]. OFETs with state-of-the-art performance now surpass that of thin-film amorphous silicon transistors [72]. As the performance of OFETs continues to improve, studies that focus on the environmental stability of high performance OFETs [19, 32, 33, 73, 74] become critical to assessing potential applications. To date, OFETs with a top-gate geometry display superior environmental stability over OFETs with a bottom gate geometry. This is because chemical or physical interactions between reactant molecules in the environment, such as oxygen and water, and the organic semiconductor channel layer lead to changes (reversible or irreversible) in the electrical properties of an OFET. Indeed, this intrinsic sensitivity has been used to realize chemical and biological OFETs sensors, which underscore the need for environmental barriers if OFET-based applications are to display stable operation.

Although environmental barriers have been used to encapsulate bottom-gate OFETs that, for example, operate even after immersion in 100 °C water using a bilayer of parylene and gold [32], most efforts have been concentrated in improving the environmental stability of organic semiconductor layers from a synthetic chemistry perspective. However, OFETs with top-gate geometry have been shown to display improved environmental stability over bottom gate OFETs [19] even in the absence of encapsulation layers because the top-gate gate dielectric also acts as an environmental barrier. Indeed, we and others have demonstrated that properly engineered gate dielectric

layers can yield n- or p-channel top-gate OFETs [34, 75], OFET-based sensors [76] and circuits [64] with remarkable long-term operational and environmental stability, even under aqueous conditions. The bilayer gate dielectric in such OFETs is comprised of an amorphous fluoropolymer layer, CYTOP, and layer of Al_2O_3 synthesized by ALD. However, in the context of corrosion, single layers of Al_2O_3 by ALD have been investigated and found to be easily corroded in humid environments [77], and single layers of other metal oxides such as TiO_2 [77] and ZrO_2 [78, 79] by ALD showing similar performance on organic electronics protection. Furthermore, the barrier properties of a single metal-oxide layer by ALD have also been found to be significantly inferior to those displayed by ALD nanolaminates (NLs) wherein ultrathin layers [77-80], a few tens of nanometer to a few nanometers thick, of two different metal oxides are intercalated to form a thicker layer. Therefore, NL layers are denser and have low water vapor transmission rate [81] which improves the barrier properties. In the context of OFETs, the use of NLs by ALD as gate dielectrics have been reported in bottom-gate OFETs [82], but not in the context of top-gate OFETs.

This chapter reports on the properties top-gate OFETs with a bilayer gate dielectric comprising a NL layer (Al_2O_3 and HfO_2 by ALD) and an amorphous fluoropolymer layer, CYTOP. We show that the use of such an NL layer yields OFETs with a comparable level of performance, operational and environmental stability compared to OFETs with a CYTOP/Al_2O_3 bilayer gate dielectric we have previously reported, but that in addition, are able to sustain immersion in hot water at 95 °C for up to 1 h.

4.2 Design of experiments

Because of this highly stable top-gate OFET structure, there is potential to apply it for medical applications, which require sterilization usually by steam, dry heat, or simply in boiling water at atmosphere. However, a single layer of ALD-grown Al_2O_3 has been shown to be less resistive than a combination of metal oxides [80] in water corrosion tests. In addition, a NL structure, alternating nanometer-thick layers of two materials for periods, has displayed excellent properties for encapsulation of OPVs [83] and OLEDs [78, 79]. ALD-grown HfO_2 will be chosen because of its availability, characteristics, and stability. To validate OFETs with a CYTOP/NL bilayer gate dielectric that can survive in harsher environments, OFETs with CYTOP/ Al_2O_3 and CYTOP/NL will be fabricated on 3.8 cm by 3.8 cm Corning glass substrates (Eagle 2000). The details of device fabrication will be described in the next section.

4.3 Device fabrication

Top-gate OFETs were fabricated with a bottom-contact geometry on glass substrates as shown in Figure 31. Source/drain electrodes comprised of Ti/Au 6/70 nm were deposited in a Denton Explorer E-beam system through a shadow mask at a deposition rate of 1.0 Å/s and at an initial pressure of 1.0×10^{-5} Torr. On top of the source and drain electrodes a layer of pentafluorobenzenethiol (PFBT) (Sigma Aldrich) was formed by immersion in a 10 mmol PFBT solution for 15 min in a N_2-filled glove box, followed by rinsing in pure ethanol for a few seconds and annealing on a hot plate for 5 min at 60 °C to dry it. A TIPS-pentacene and PTAA blend (1:1 weight ratio) was used as the organic semiconducting layer. TIPS-pentacene and PTAA blend were dissolved in 1, 2, 3, 4-Tetrahydronaphthalene anhydrous, 99%, (Sigma Aldrich) at a

concentration of 30 mg/ml. A 70 nm-thick [64] layer of TIPS-pentacene and PTAA was spin-coated onto source and drain electrodes at 500 rpm for 10 s (acceleration of 500 rpm/s) and ramped to 2,000 rpm for 20 s (acceleration of 1,000 rpm/s). Spin-coated films were then annealed at 100°C for 15 min on a hot plate in a N_2-filled glove box. A bilayer gate dielectric was fabricated by diluting CYTOP (Asahi Glass, CTL-809M) with solvent (Asahi Glass, CTL-SOLV180) to concentration of 2% by volume. A layer of CYTOP was spin-coated on top of the organic semiconducting layer at 3,000 rpm for 60 s (acceleration of 10,000 rpm/s) to yield a ca. 35 nm-thick layer [64]. Samples were then annealed at 100 °C for 10 min on hot plate in a N_2-filled glove box. After that, an Al_2O_3 and HfO_2 NL was deposited in a Savannah 100 ALD system at 100°C. The NL comprised 200 cycles of Al_2O_3 on CYTOP to serve as a nucleation layer, followed by five cycles of Al_2O_3 and five cycles of HfO_2 repeated 20 times, which yielded a ca. 38 nm-thick layer. 100 nm-thick Ag or Au gate electrodes were then deposited through a shadow mask in a SPECTROS thermal evaporator with initial pressures below 1.0×10^{-6} Torr and at an average deposition rate of 1.0 Å/s. Reference OFETs with CYTOP/Al_2O_3 bilayer gate dielectric were also fabricated as previously reported [34].

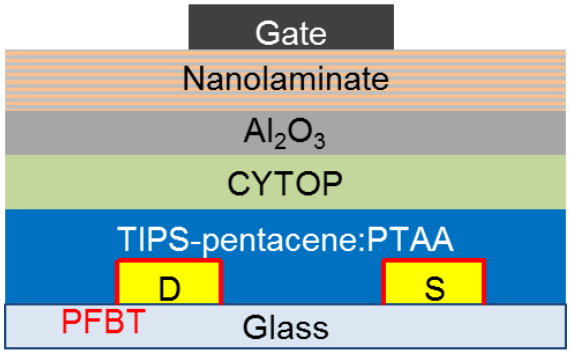


Figure 31. The device structure of top-gate OFETs with CYTOP/NL gate dielectric.

4.4 Device characterization

OFET devices were characterized in a N_2-filled glove box (O_2 and H_2O < 0.1 ppm, 25°C) and at ambient conditions (25°C and 20 to 40% RH) using an Agilent E5272A source/monitor unit. The environmental stability was investigated by storing OFETs in an environmental chamber under different conditions as will be described next and transferred to a N_2-filled glove box for characterization. OFETs were also immersed in water at 95 °C and their properties characterized under ambient conditions after different immersion times. The barrier properties of the CYTOP/NL bilayer were also characterized by immersion in water at 95 °C on samples comprising Ca sensors deposited on glass and encapsulated using CYTOP/Al_2O_3 or CYTOP/NL bilayers fabricated as previously described. Photo images were taken during the hot water test to monitor the degradation rate of calcium under the two types of bilayer dielectric.

4.4.1 Pristine condition in nitrogen

The transfer characteristic of top-gate OFETs with CYTOP/NL bilayer gate dielectrics and Au gate electrodes are shown in Figure 32. Average hole mobility values of 0.92 ± 0.22 cm^2/Vs and average threshold voltage values of -1.9 ± 0.5 V where found on these OFETs. These values are comparable to those displayed by top-gate OFETs with CYTOP/Al_2O_3 bilayer gate dielectric.

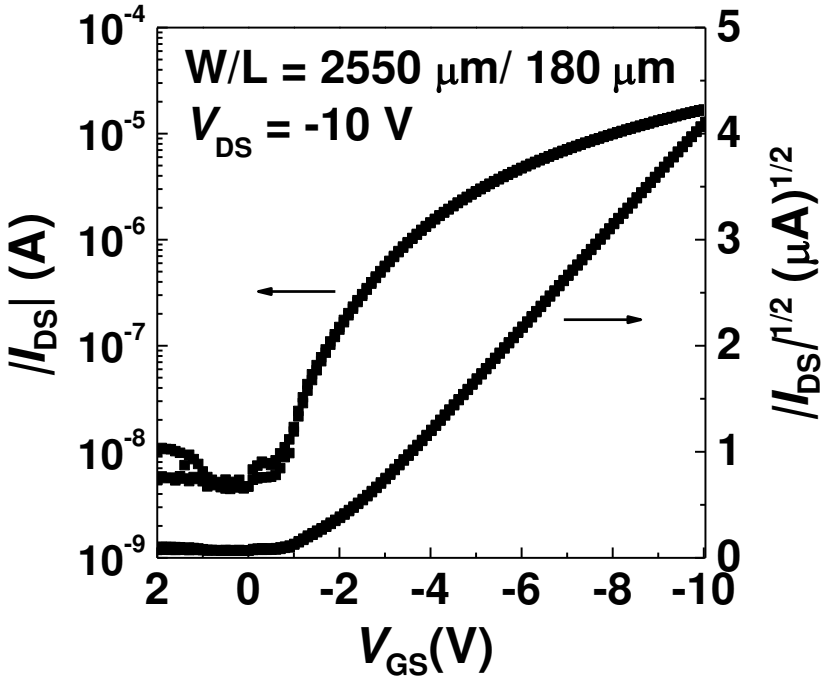


Figure 32. Transfer characteristics of OFETs with CYTOP/NL gate dielectric.

4.4.2 Environmental stability in various critical conditions

Then, we subjected top-gate OFETs through the following conditions of environmental exposure: ambient air for 30 days; vacuum annealing at 100 °C for 16 h; damp air (50 °C and 80% RH for 24 h); vacuum annealing at 100 °C for 16 h; ambient air for 24 h; immersion in distilled water at room temperature for 16 h; vacuum annealing at 100 °C for 16 h; ambient air for 24 h; vacuum annealing at 100 °C for 16 h; immersion in 50 °C distilled water for 16 h; and vacuum annealing at 100 °C for 16 h. Figure 33 displays the evolution of the charge mobility, threshold voltage, and the number of operating OFETs after different conditions of environmental exposure. This data is consistent with previous reports on the environmental stability of top-gate OFETs with CYTOP/Al_2O_3 bilayer gate dielectric [74] in that the mobility values remain nearly

constant and the threshold voltage values decrease after vacuum annealing and increase with exposure to humid atmospheres. Throughout these experiments, five out of seven OFETs remained working.

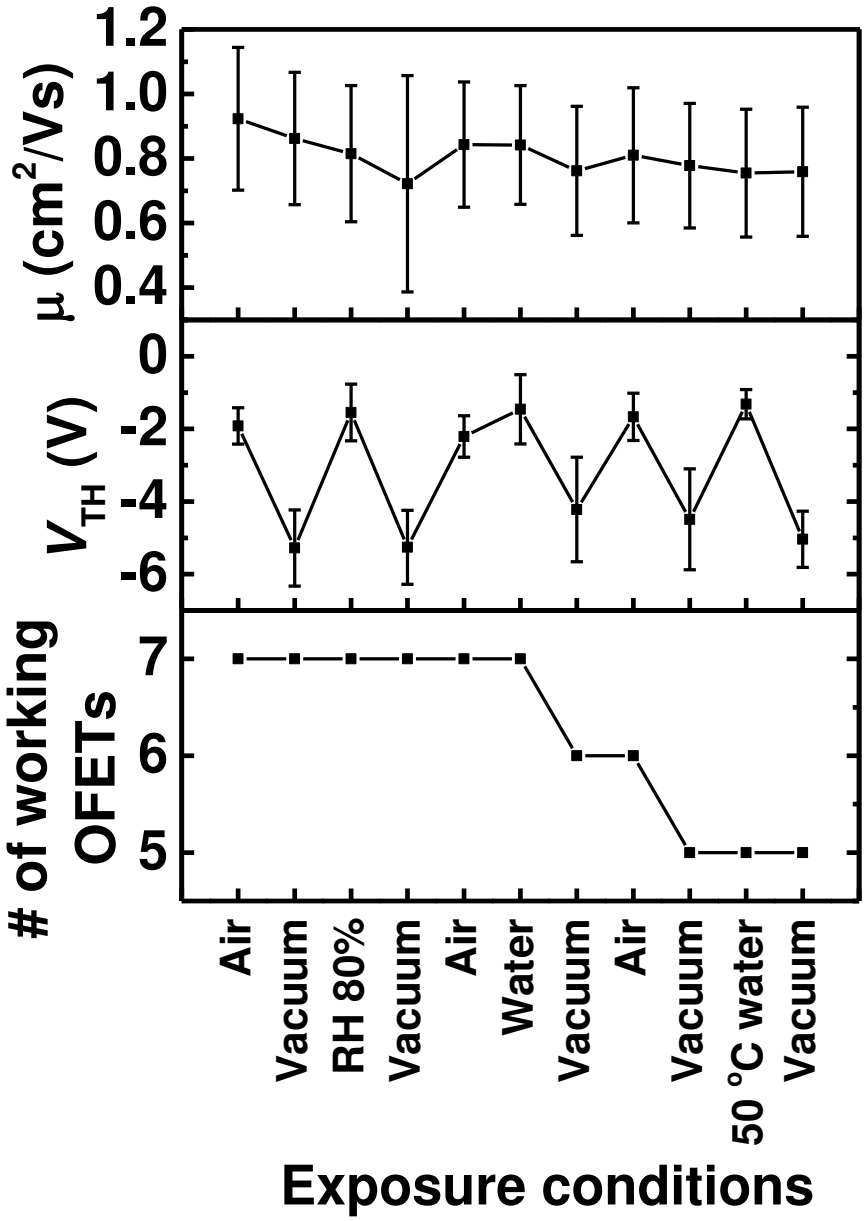


Figure 33. Performance of top-gate OFETs exposed to various environments.

4.4.3 Operational stability in air

Next, a new batch of top-gate Ref-OFETs and NL-OFETs were fabricated. Figure 34 displays a comparison of typical transfer characteristics measured in air-exposed devices. NL-OFETs displayed average hole mobility values of 0.71 ± 0.14 cm^2/Vs and average threshold voltage values of 0.1 ± 0.4 V. Ref-OFETs displayed average hole mobility values of 0.64 ± 0.12 cm^2/Vs and average threshold voltage values of 0.0 ± 0.4 V. The performance of both types of devices is comparable and within the range of batch-to-batch variations.

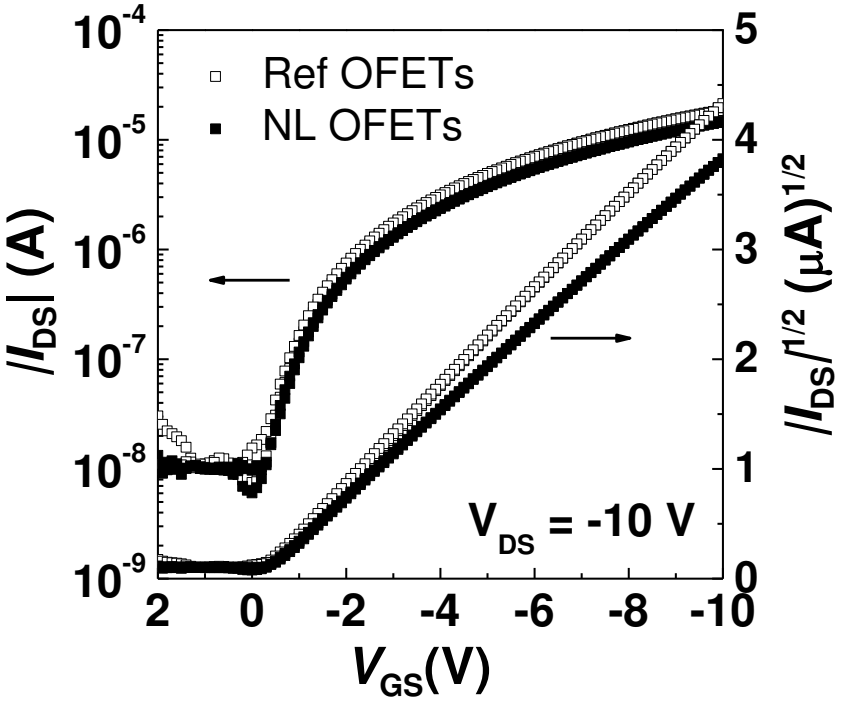


Figure 34. Transfer characteristics of Ref- and NL-OFETs with Ag gate.

Figure 35 displays DC bias stress characteristics for 1h on top-gate Ref-OFETs and NL-OFETs. In this measurement, the step is 10 s and gate-to-source voltage and drain-to-source voltage are both at -10 V. Negligible on-current variation observed on

both Ref-OFETs and NL-OFETs in the DC bias stress measurement for 1 h showing CYTOP/NL bilayer gate dielectric provides the same operational stability as that of CYTOP/Al_2O_3 provided.

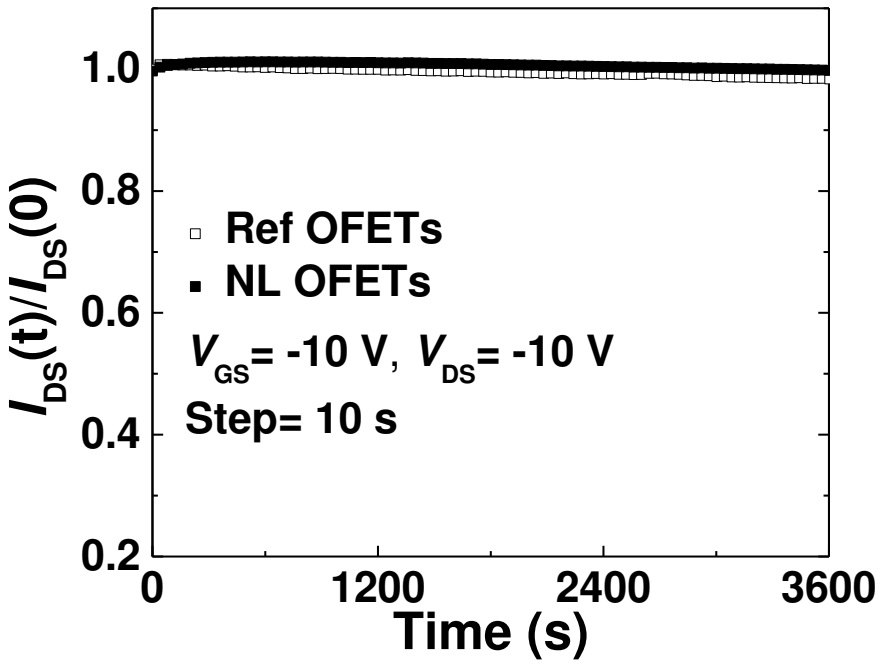


Figure 35. DC bias stress in air for 1 h on Ref- and NL-OFETs with Ag gate.

4.4.4 Environmental stability in hot water at 95 °C

We immersed both types of OFETs into 95 °C water, to avoid boiling, and their transfer characteristics monitored in air as a function of immersion time. Figure 36 displays the charge mobility and threshold voltage values as well as the number of functional OFETs as a function of immersion time, revealing major differences in device stability. First, the electrical properties of ref-OFETs remain stable in 95 °C water for two min and irreversibly get damaged after three min of immersion. In contrast, NL-OFETs display stable characteristics for over 16 min in 95 °C water, after which the threshold

voltage values decrease monotonically at least up to 1 h of immersion time. Remarkably, throughout the entire 1 h of immersion time, the average hole mobility values remain stable and in the range between 0.5 to 0.7 cm^2/Vs. With 50% of the NL-OFET remaining functional after these harsh conditions of environmental exposure, it is clear that the CYTOP/NL bilayer does offer superior barrier properties over the CYTOP/Al_2O_3 bilayer.

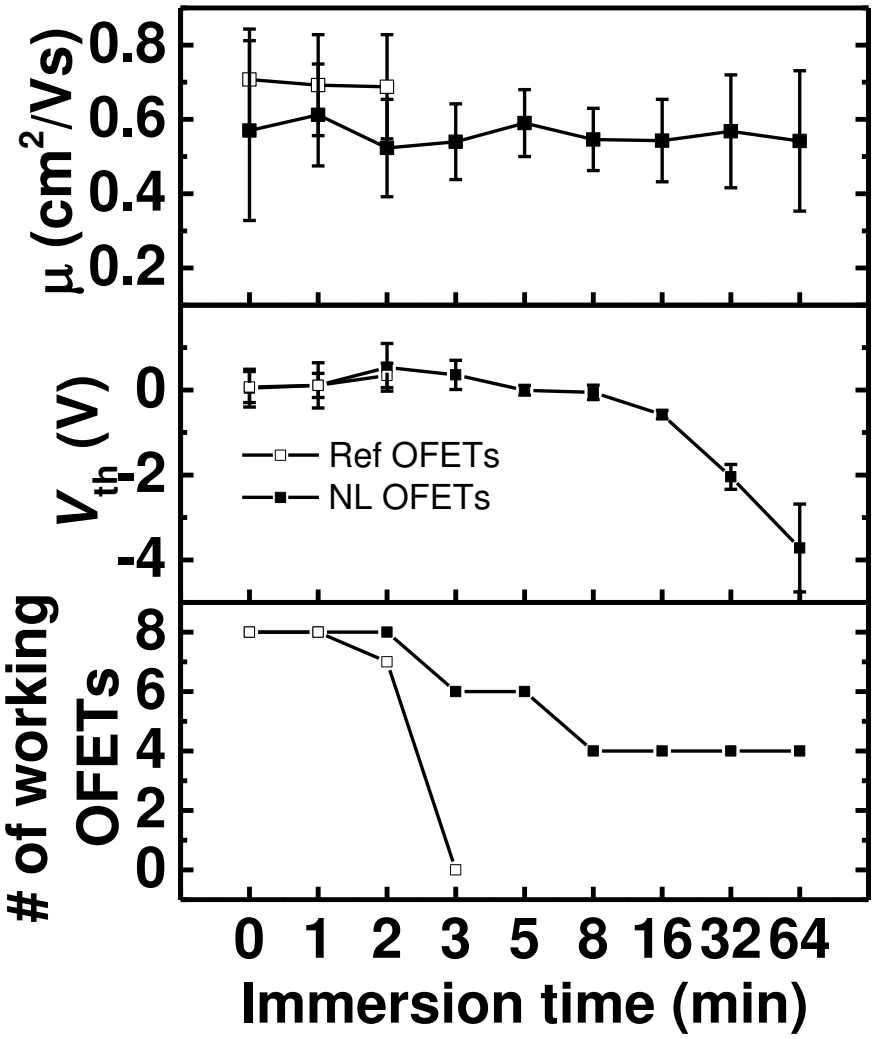


Figure 36. Extracted carrier mobility, threshold voltage, and the number of working OFETs.

To further investigate the barrier properties and to provide insight into the failure mechanism, we conducted similar immersion experiments on samples with Ca sensors encapsulated by either CYTOP/Al_2O_3 or CYTOP/NL bilayers. The cross section is shown as Figure 37.

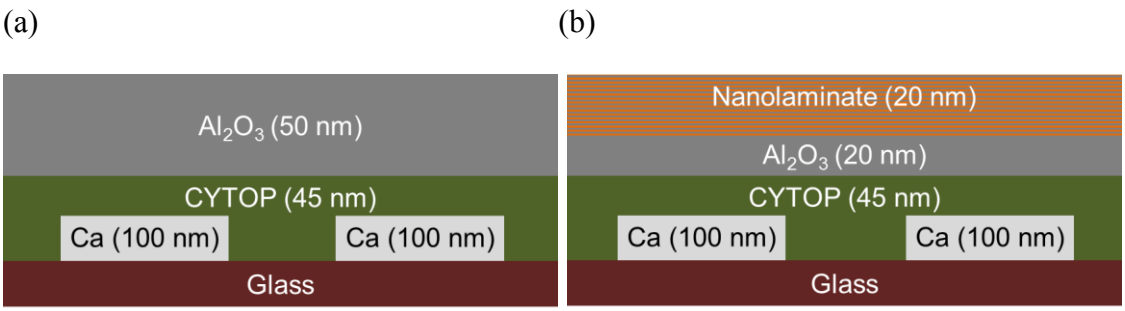


Figure 37. Ca encapsulated by (a) CYTOP/Al_2O_3 and (b) CYTOP/NL.

The degradation of calcium is easily recognized because it becomes transparent as it is oxidized. Figure 38 (a), (b), and (d) display photographs of the calcium sensors after 30 s and three min of immersion time in water at 95 °C which reveal the sudden disappearance of the Ca sensors encapsulated with a CYTOP/Al_2O_3 bilayer after three min of immersion. In contrast, the degradation of the Ca sensors encapsulated with a CYTOP/NL bilayer is much slower and inhomogeneous, arising from point defects in the sample, resulting in several areas of Ca throughout the substrate after three min of immersion. In contrast, on a sample having a CYTOP/NL bilayer, oxidized Ca was observed only on areas with particles and defects in the metal-oxide layer. These observations are consistent with recently published studies where we have found that the residual stress of ALD layers is the primary mechanism of mechanical failure due to the propagation of cracks that start around areas of concentrated stress (i.e. around particles and defects) [84]. The NL layer is then believed to lead to a superior solution for

encapsulation under harsher environments without changing transistor electrical and operational characteristics.

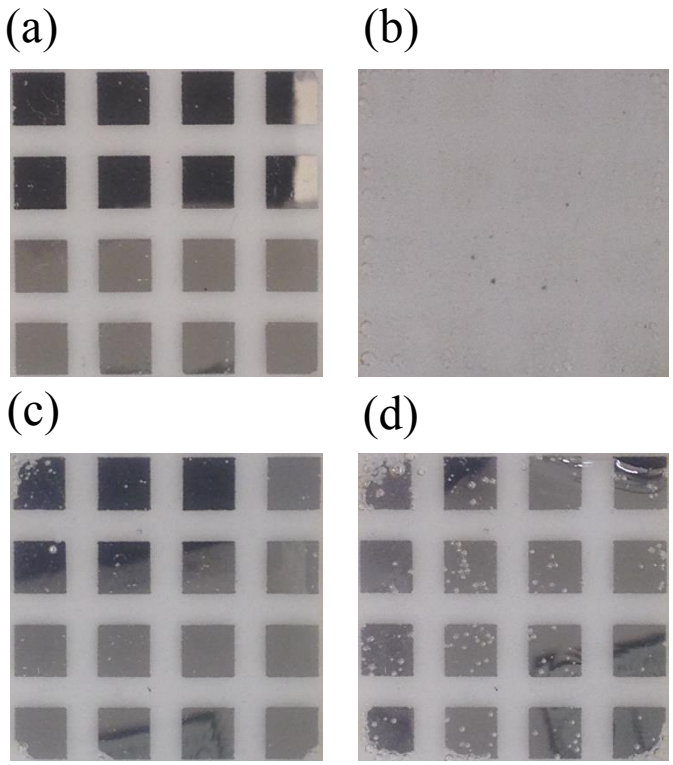


Figure 38. Photographs of encapsulated 100 nm Ca samples with (a) Encapsulated by CYTOP/Al_2O_3 in water at 95 °C for 30 s (b) Encapsulated by CYTOP/Al_2O_3 in water at 95 °C for 3 min (c) Encapsulated by CYTOP/NL in water at 95 °C for 30 s (d) Encapsulated by CYTOP/NL in water at 95 °C for 3 min.

4.5 Device modeling

The software for device modeling in this section is also ADS from Keysight Technologies, and the same equation (7) applied here is from Marinov *et. al.* [24, 25] is used to fit the current-voltage characteristics of OFETs. Figure 39 displays the fitting of the Ref-OFET shown in Figure 34. Extracted μ and V_{TH} were 0.66 cm^2/Vs and -0.1 V. Fitted SS is 0.30 V/decade, and the corresponding defect density D_{it} calculated by equation (6) is 9×10^{11} cm^{-2}. Empirical parameters such as V_{aa}, γ, and λ are 10 V, 0, and

0.016 respectively. The non-linearity of measured output characteristics at low drain-to-source bias voltage in Figure 39 (b) can be attributed to current injection barrier on source and drain contacts discussed in details in Chapter 5. In the same figure of Figure 39 (b), measured data follow the model at high drain-to-source bias voltage indicates that current-voltage characteristics follow the model again after overcome the injection barrier on source and drain contacts.

(a) (b)

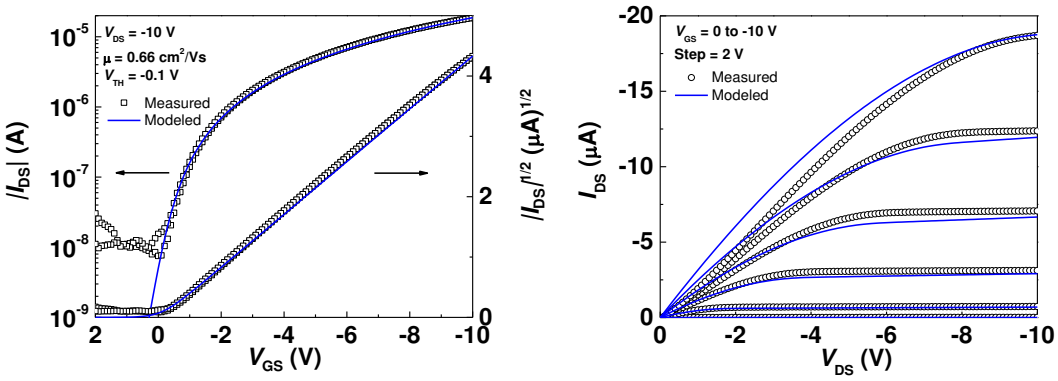


Figure 39. (a) Fitting of transfer characteristics on a Ref-OFET. (b) Fitting of output characteristics on a Ref-OFET.

Meanwhile Figure 40 displays the fitting of the NL-OFET shown in Figure 34. Extracted μ and V_{TH} were 0.49 cm^2/Vs and -0.3 V. Fitted SS is 0.40 V/decade, and the corresponding defect density D_{it} calculated by equation (6) is 1×10^{12} cm^{-2}. Fitted empirical parameters such as V_{aa}, γ, and λ are 10 V, 0, and 0.016 respectively are the same as the Ref-OFET. Similar injection barrier is also shown in Figure 40 (b) and will be discussed in details in Chapter 5. The representative Ref-OFET and NL-OFET have similar extracted and fitted parameters displaying that environmental stability is improved while preserving the electrical characteristics.

(a) (b)

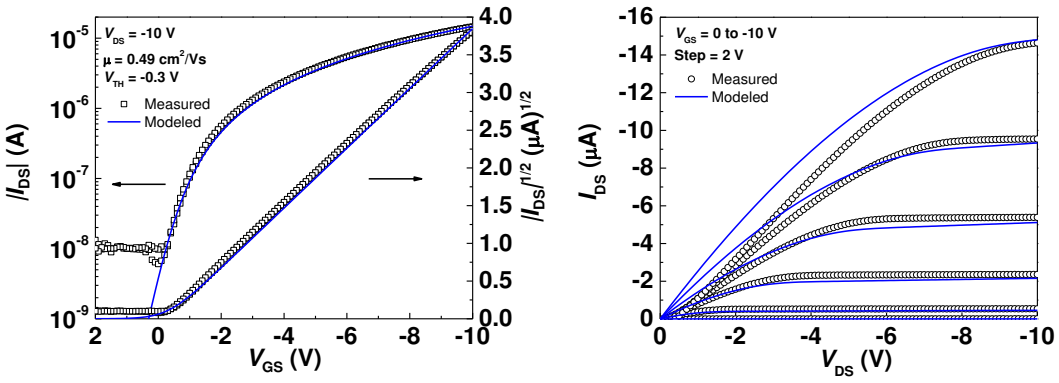


Figure 40. (a) Fitting of transfer characteristics on a NL-OFET. (b) Fitting of output characteristics on a NL-OFET.

4.6 Summary

We have demonstrated enhanced stability of top-gate OFETs by using CYTOP/NL to replace CYTOP/Al_2O_3 gate dielectric which also served as a barrier layer. The electrical characteristics of the original (CYTOP/Al_2O_3) and the modified (CYTOP/NL) structure are comparable in terms of mobility, threshold voltage, on/off current ratio, and stability in different environments. OFETs with CYTOP/NL gate dielectric further show even better stability in 95 °C water over 1 h with functional OFETs. This contrasts with OFETs having a CYTOP/Al_2O_3 gate dielectric which can only sustain in 95 °C water for less than three min. These results can be rationalized by the fact that nanolaminate structures display better environmental barrier properties compared to a single metal-oxide layer. Device modeling was also performed and indicating a current injection barrier existing in the source and drain contacts that can be improved to elevate device performance. We believe that these results contradict conventional wisdom that OFETs can only be robust to harsh environments providing that the structure of the device and the choice of materials are judicious.

CHAPTER 5

REDUCTION OF CONTACT RESISTANCE IN OFETS

5.1 Introduction

Despite significant progress in the development of high mobility organic semiconductors and OFETs with high operational and environmental stability [34, 35, 75], limitations still exist in reducing the size of OFETs since their performance becomes limited by parasitic contact resistance. The contact resistance is related to the existence of energetic barriers for the injection of charge carriers at the source/drain contacts and resistive power losses that may occur between the contact and the channel. Reductions of the energetic barriers at the contacts have been achieved by contact doping in both n-channel [18, 85, 86] and p-channel [87-102] OFETs. In case of p-channel OFETs, contact doping has been implemented using: F_4TCNQ [90-95], derivatives such as F_6TCNNQ [96], transition metal oxides such as MoO_3 [97-99], $Mo(tfd)_3$ [100-102], and $FeCl_3$ [87-89]. In most cases, contact doping has been implemented in bottom-gate top-contact OFET geometries by co-evaporation of the dopant and the organic semiconductor layer or direct evaporation of the dopant on the contact area. A drawback of the bottom-gate OFETs geometry is that it leaves the organic semiconductor layer exposed to the ambient, and consequently poor, environmental stability.

Our group and others have shown that the use of top-gate OFET geometries greatly improve their operational and environmental stability [34, 35, 75, 103, 104]. In particular, we have shown that top-gate OFETs using a bilayer CYTOP/Al_2O_3 gate dielectric comprising a ca. 40 nm-thick CYTOP on top of which is a ca. 40 nm-thick ALD-grown Al_2O_3 layer leads to both n-channel [75] and p-channel [34, 35] OFETs with

excellent stability. Top-gate OFETs with the bilayer CYTOP/Al_2O_3 gate dielectric offer a suitable platform for the development of chemical and biological sensors [105] and complex electronic circuits [64]. However, previous demonstrations of p-channel top-gate OFETs with bilayer CYTOP/Al_2O_3 gate dielectrics have relied on the use of PFBT modified Au source/drain electrodes. PFBT is primarily used to increase the work function of Au and improve the wetting of acene-based channel layers but leads to appreciable contact resistance-caused effects such as high threshold voltage values (typically larger than ca. -2.0 V, on pristine devices [34, 35]) and nonlinear behavior on the output characteristics at low drain-to-source voltage values.

Contact doping on top-gate OFETs has been scarcely reported in the literature. In p-channel top-gate C_8-BTBT-based OFETs, it has been shown that $FeCl_3$ doped source/drain electrodes lead to 10 to 20 times lower contact resistance values than the ones displayed by OFETs with undoped electrodes [89]. Zhou *et al.* also showed that polyethylenimine-coated Au source/drain electrodes significantly reduce the threshold voltage in n-channel transistors [106].

5.2 Design of experiments

To develop high-performance OFETs, reducing the contact resistance is part of my study. The same top-gate OFETs on glass substrates with TIPS-pentacene:PTAA as the active layer and bilayer CYTOP/Al_2O_3 as gate dielectric have been used. Comparative studies of the contact resistance displayed by top-gate bottom-contact TIPS-pentacene:PTAA OFETs were carried out in devices with source/drain electrodes using bare Au, PFBT treated Au, and $Mo(tfd)_3$ coated Au. The results shows that using

$Mo(tfd)_3$ coated Au electrodes leads to a huge decrease in contact resistance compared to the widely used PFBT Au modification approach.

5.3 Device fabrication

Top-gate OFETs with three types of device geometry are shown in Figure 41. A1-type OFETs correspond to devices with bare Au source/drain electrodes; A2-type OFETs correspond to devices with PFBT-treated Au source/drain electrodes; A3-type OFETs correspond to devices with $Mo(tfd)_3$-coated Au source/drain electrodes.

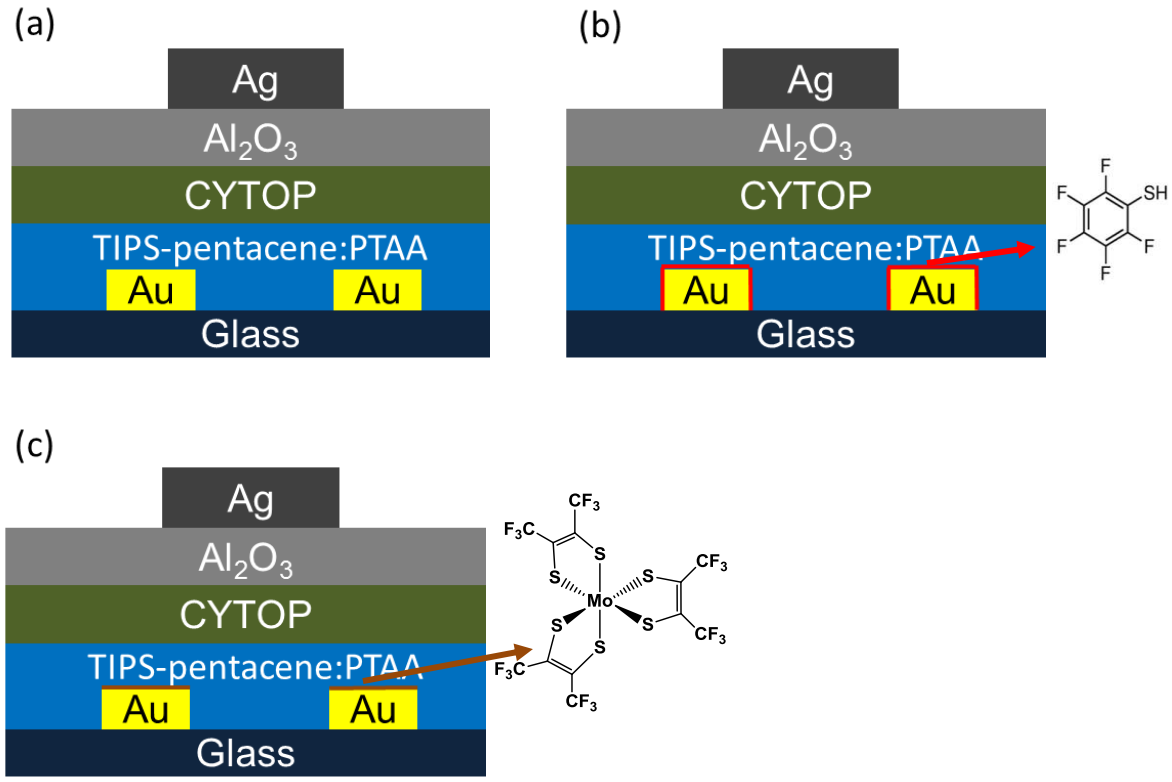


Figure 41. (a) A1, top-gate TIPS-pentacene:PTAA OFETs with bare Au as source/drain electrodes. (b) A2, top-gate TIPS-pentacene:PTAA OFETs with PFBT treated Au as source/drain electrodes and the chemical formula of PFBT. (c) A3, top-gate TIPS-pentacene:PTAA OFETs with $Mo(tfd)_3$ coated Au as source/drain electrodes and the chemical formula of $Mo(tfd)_3$.

OFETs were fabricated as the following: A layer of 50 nm-thick Au source/drain electrodes were deposited through a shadow mask on cleaned 3.8 cm by 3.8 cm Corning

glass substrates (Eagle 2000) in a Denton Explorer e-beam system at a deposition rate of 1.0 Å/s at an initial pressure below 1.0×10^{-5} Torr. After deposition of the source/drain metal electrodes, the substrates were transferred to a N_2-filled glovebox. For A1-type OFETs, the electrodes consisted of untreated bare Au electrodes. For A2-type OFETs, the Au source/drain electrodes were treated with PFBT by first dipping the samples in a 10 mmol PFBT solution in ethanol (Sigma-Aldrich) for 15 min and rinsing into pure ethanol for one min to remove excess PFBT molecules. After rinsing, samples were dried on a hot plate at 60 °C for five min. For A3-type OFETs, a layer of 1.5 nm-thick $Mo(tfd)_3$ was deposited onto the Au source/drain electrodes through a shadow mask. For all devices, the fabrication procedure of organic semiconductor layer coating, bilayer gate dielectric coating and deposition, and gate electrodes deposition are the same as description below. A TIPS-pentacene (Sigma Aldrich) and PTAA (Sigma Aldrich) blend solution was used as the organic semiconducting layer. The (1:1 weight ratio) TIPS-pentacene:PTAA solution was dissolved in anhydrous tetralin, (Sigma Aldrich) at a concentration of 30 mg/ml. The TIPS-pentacene:PTAA blended solution was spin-coated at 500 rpm for 10 s (acceleration of 500 rpm/s) and ramped to 2,000 rpm for 20 s (acceleration of 1,000 rpm/s) to yield a ca. 70 nm-thick layer [64]. Spin-coated films were then thermally annealed at 100 °C for 15 min on a hot plate in a N_2-filled glove box. A bilayer gate dielectric was started from diluting CYTOP (Asahi Glass, CTL-809M) with Asahi Glass, CTL-SOLV180 to a concentration of 2% by volume. A layer of CYTOP was spin coated on top of the organic semiconducting layer at 3,000 rpm for 60 s (acceleration of 10,000 rpm/s) to yield a ca. 35 nm-thick layer [64]. Samples were then thermally annealed at 100 °C for 10 min on a hot plate in a N_2-filled glove box. After that, 500 cycles of ALD-

grown Al_2O_3 were deposited at 110 °C to yield a ca. 40 nm-thick layer [64]. Later, 100 nm-thick Ag gate electrodes were deposited through a shadow mask in a thermal evaporator (Kurt J. Lesker, SPECTROS) with initial pressures below 1.0×10^{-6} Torr and at an average deposition rate of 1.0 Å/s.

5.4 Device characterization

A1, A2, and A3-type OFETs were characterized inside a N_2-filled glove box (O_2 and H_2O < 0.1 ppm, 25°C) using an Agilent E5272A source/monitor unit. Figure 42 displays a comparison between the transfer and output characteristics measured on the best A1-, A2- and A3-type OFETs with different *W* to *L* ratios.

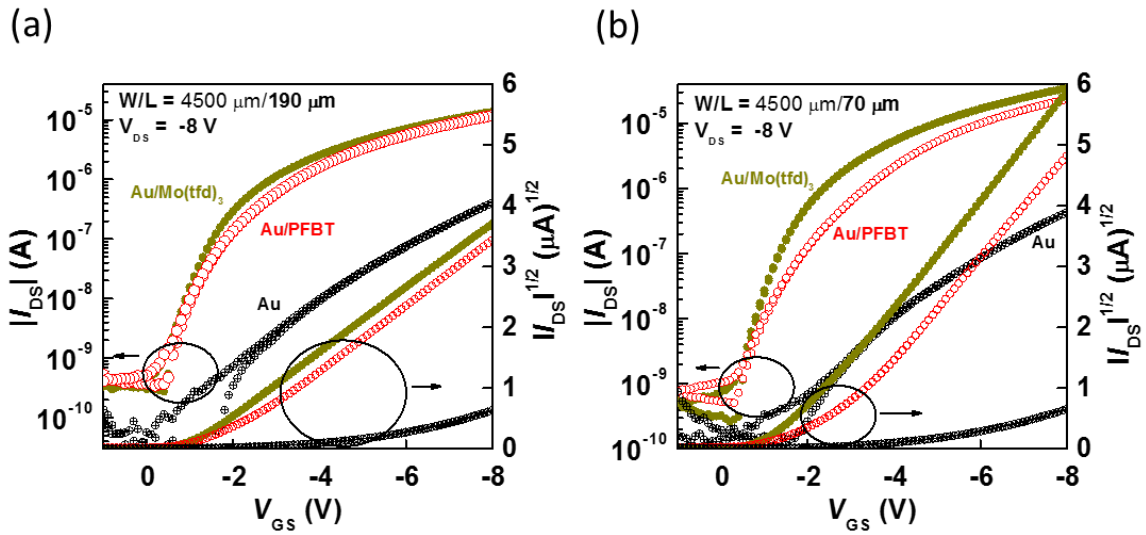


Figure 42. (a) Transfer characteristics of bare Au, PFBT-treated Au, and $Mo(tfd)_3$-coated Au OFETs with *W/L* = 4500 μm/190 μm. (b) Transfer characteristics of bare Au, PFBT-treated Au, and $Mo(tfd)_3$-coated Au OFETs with *W/L* = 4500 μm/70 μm.

Figure 42 (a) displays the transfer characteristics of OFETs with *W/L* = 4500 μm/190 μm, wherein the on-current value found in an A1-type OFET, I_{DS} (-8V) = 0.4 μA (average 0.3 ± 0.1 μA), is significantly smaller when compared to values found in A2-type OFETs, I_{DS} (-8V) = 11.8 μA (average 10.5 ± 1.0 μA) and A3-type OFETs, I_{DS} (-8V)

= 13.7 μA (average 12.3 ± 1.6 μA). At this point, it is worth noting that the transfer characteristics of A1-type OFETs differ so drastically from the square law approximation that values of carrier mobility and threshold voltage cannot be extracted from the transfer curves. As summarized, differences in the on-current values between A2- and A3-type OFETs can be attributed to reduced threshold voltage found on A3-type OFETs, -0.9 ± 0.1 V, compared to threshold voltage found on A2-type OFETs, -1.8 ± 0.2 V. As shown in Figure 42 (b), a similar trend is found in OFETs having W/L = 4500 μm/70 μm, wherein the on-current value at -8V displayed by a representative A3-OFET is higher, I_{DS} (-8V) = 35.2 μA (average 30.4 ± 3.4 μA), than the value of I_{DS} (-8V) = 23.2 μA (average 19.9 ± 2.0 μA) displayed by A2-OFETs and much higher than on-current value displayed by A1-OFETs , I_{DS} (-8V) = 0.4 μA (average 0.3 ± 0.1 μA). As before, the transfer characteristics of A1-type OFETs do not allow extractions of mobility and threshold values using the square law approximation. Here again, the higher on-current value on A3-type OFETs than A2-type OFETs is assigned to a reduced average threshold voltage of -1.4 ± 0.1 V, compared to threshold voltage found in A2-type OFETs, -2.7 ± 0.3 V.

Figure 43 summarizes the average values of carrier mobility μ, and threshold voltage V_{TH} for A2- and A3-type OFETs having different channel length values of L = 70, 110, and 190 μm with a channel width value W = 4500 μm. In Figure 43 (a), the average values of carrier mobility in A2- and A3-type are statistically comparable in all devices; however, statistically significant differences in the average values of threshold voltage in Figure 43 (b) are clearly observed. A3-type OFETs with lower average values of threshold voltage improve charge injection at the source/drain electrodes when

compared to devices having PFBT-treated Au source/drain electrodes, A2-type OFETs, or with devices having pristine Au source/drain electrodes, A1-type OFETs.

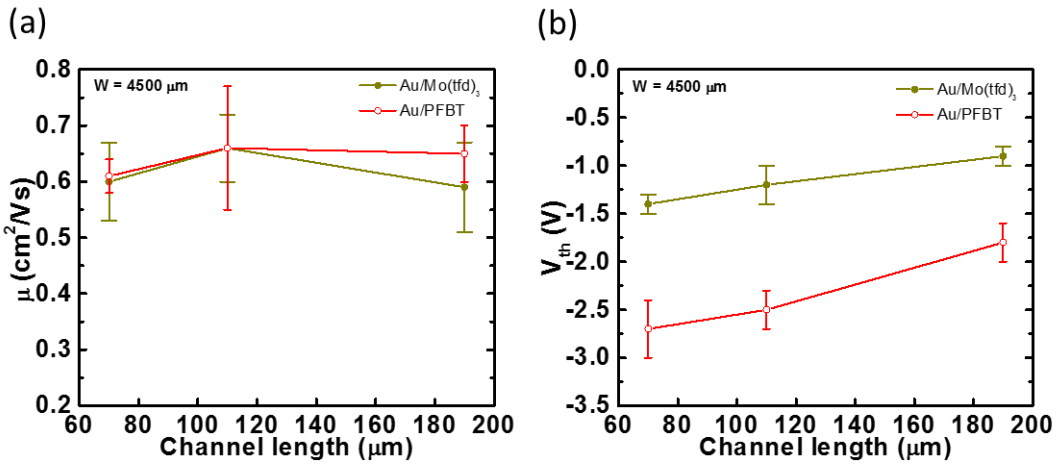


Figure 43. (a) Mobility of PFBT-treated Au and $Mo(tfd)_3$-coated Au OFETs at different channel lengths. (b) Threshold voltage of PFBT-treated Au and $Mo(tfd)_3$-coated Au OFETs at different channel lengths.

It is also known that contact resistance produces a parasitic nonlinear dependence of the I_{DS} when V_{DS} values approach 0 V. These effects are readily observed on the output characteristics of A1- and A2-type devices displayed on Figure 44. These figures also show that the linearity of I_{DS} at V_{DS} values approaching 0 V is greatly improved in A3-type OFETs. Contact resistance value R_c on each type of OFETs can be calculated from the output characteristics of OFETs having different *W/L* rations using the transfer length method. First, the on-current R_{ON} as V_{DS} approaches 0 V is extracted according to equation (3) (see chapter 1) and that is reproduced below [21, 107, 108]:

$$R_{ON} = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{DS}\to 0} = R_{ch} + 2R_c = R_{sh}\frac{L}{W} + 2R_c \ , \qquad (3)$$

where R_{ch} is the channel resistance, and R_{sh} is the sheet resistance of the channel. The ordinate in the plot of R_{ON} vs. L when L equals zero corresponds to $2R_c$.

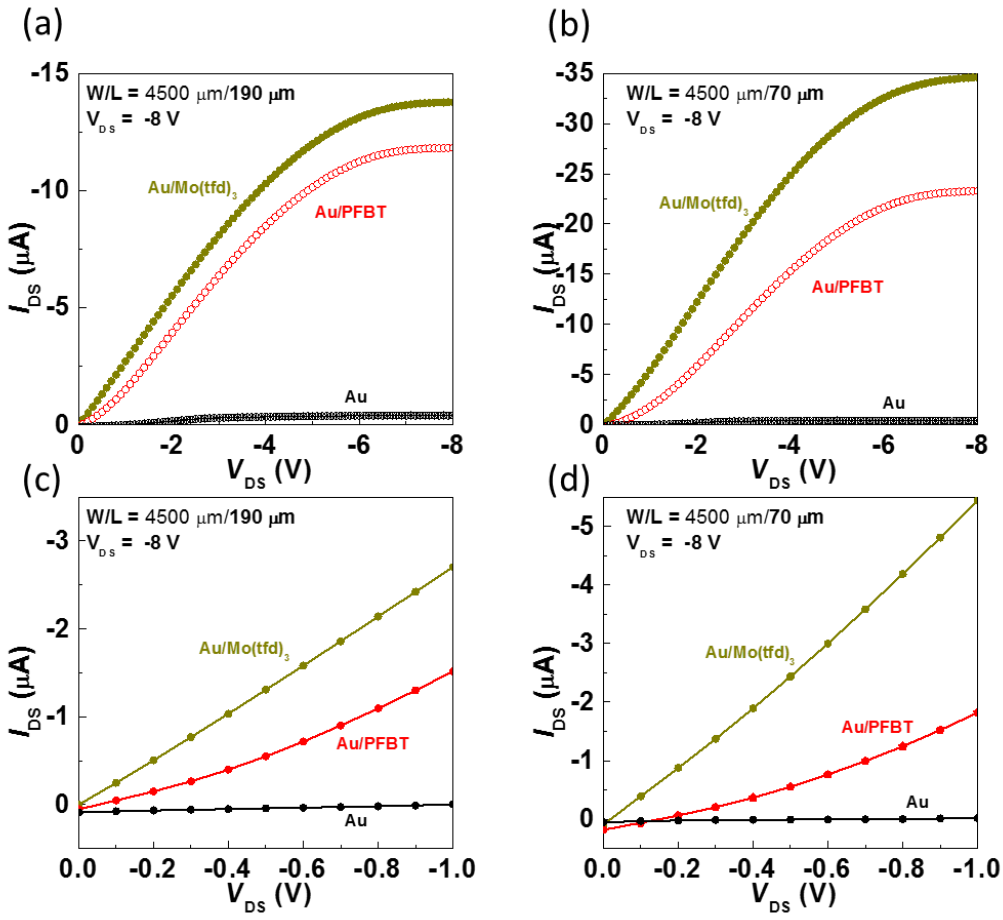


Figure 44. (a) On-state output characteristics of bare Au, PFBT-treated Au, and $Mo(tfd)_3$-coated Au OFETs with *W/L* = 4500 μm/190 μm. (b) On-state output characteristics of bare Au, PFBT-treated Au, and $Mo(tfd)_3$-coated Au OFETs with *W/L* = 4500 μm/70 μm. (c) A zoom-in plot of (a). (d) A zoom-in plot of (b).

As displayed on Figure 45, the normalized contact resistance R_cW on A2- and A3-type OFETs was extracted following this method at V_{GS} = -4, -6, and -8 V. In A3-type OFETs, this method yields nearly constant average R_cW values of 42 and 34 kΩcm, at -4V and -8V respectively. In contrast, in A2-type devices, average R_cW values of 335 kΩcm and 156 kΩcm were determined at -4V and -8V, respectively. These results clearly show a significant reduction of parasitic contact resistance in OFETs having $Mo(tfd)_3$-coated Au source and drain electrodes. To further illustrate this point, we can extract a characteristic channel length value, L_c, for which $R_{ch} = 2R_c$, at fixed V_{GS}. For a channel

width W of 4500 µm and V_{GS} at -8 V, L_c equals to 103 µm for A3-type OFETs, while for A2-type OFETs L_c equals to 345 µm. This suggests that OFETs size could be reduced by a factor of ca. 3.4 before parasitic contact resistance starts dominating device performance by using Au/Mo(tfd)$_3$ source and drain electrodes when compared to OFETs using Au/PFBT electrodes.

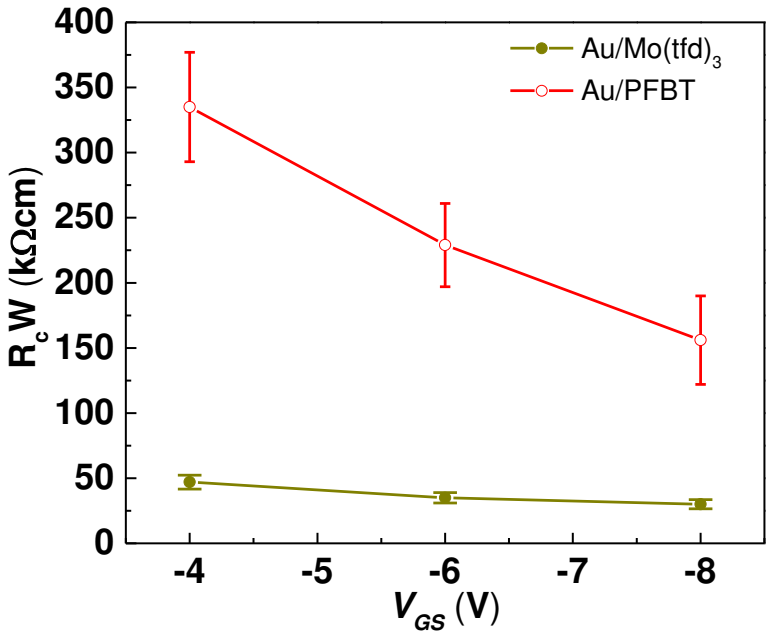


Figure 45. Normalized contact resistance of PFBT-treated Au and Mo(tfd)$_3$-coated Au OFETs at V_{GS} = -4, -6, and -8 V.

It should be pointed out that a decrease in the contact resistance may arise from reduction of the injection barrier at the electrodes and/or from increased conductivity of the organic semiconductor around the electrode region. Preliminary analysis was done after this discovery. The work function value from another batch of bare Au, Au/PFBT, and Au/Mo(tfd)$_3$ has been measured by using a Kelvin probe placed in a nitrogen-filled glovebox, and found values of 4.94 ± 0.04, 5.43 ± 0.01 and 5.47 ± 0.02 eV, respectively.

Having these values in mind, it is worth pointing out that energy level alignment at interfaces involving organic semiconductors can be complex and hard to predict. However, it is well established that if the work function of an electrode is higher than a certain critical value, known as the pinning level, the energetic barrier height at the contact remains fixed. For instance, Davis and co-workers [109] measured the work function of samples comprising a thin TIPS-pentacene film on conductive substrates having different work function values ranging from 3.7 to 5.2 eV. They found that the work function of the substrate/TIPS-pentacene samples remained pinned at 4.8 ± 0.1 eV for conductive substrates displaying work function values larger than 4.8 eV. The IP value for PTAA is 5.2 eV from Logan and co-workers [110]. From the above points, it is reasonable to conclude that the differences in the work function values between bare Au, Au/PFBT, and Au/$Mo(tfd)_3$ are not responsible for the drastic decrease in the contact resistance. Instead, the reduction of contact resistance values observed in OFETs using Au/$Mo(tfd)_3$ electrodes might be primarily attributed to a combination of increase in work function of the Au electrode and p-doping of the semiconductor layer induced by $Mo(tfd)_3$.

5.5 Device modeling

The same software and model are applied in this section for device modeling. Figure 46 displays the fitting of an OFET with Au/$Mo(tfd)_3$ source and drain electrodes. Extracted μ and V_{TH} were 0.87 cm^2/Vs and -1.6 V. Fitted SS is 0.70 V/decade, and the corresponding defect density D_{it} calculated by equation (6) is 2×10^{12} cm^{-2}. Empirical parameters such as V_{aa}, γ, and λ are 10 V, 0, and 0.012 respectively. The current-voltage characteristics follow the model and no non-linearity of measured output characteristics

at low drain-to-source bias voltage as shown in Figure 39 (b) and Figure 40 (b). This indicates that the current injection barrier on source and drain contacts was eliminated by contact doping using $Mo(tfd)_3$.

(a) (b)

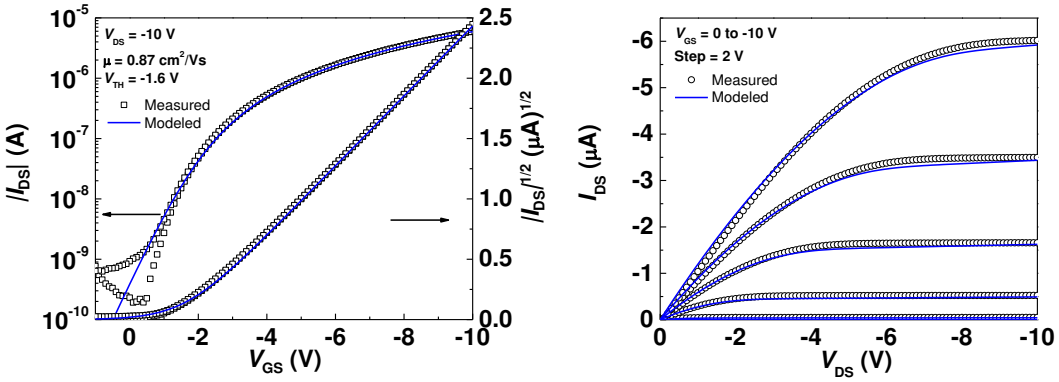


Figure 46. (a) Fitting of transfer characteristics on an OFET with Au/$Mo(tfd)_3$ source and drain electrodes. (b) Fitting of output characteristics on an OFET with Au/$Mo(tfd)_3$ source and drain electrodes.

5.6 Summary

Top-gate TIPS-pentacene:PTAA p-channel OFETs with Au/$Mo(tfd)_3$ source/drain electrodes display the lowest contact resistance among OFETs with bare Au contacts and PFBT-treated Au contacts. The normalized contact resistance of OFETs having Au/$Mo(tfd)_3$ source/drain electrodes varied from 42 to 34 kΩcm for V_{GS} in the range from -4 V to -8 V, respectively. In contrast, the normalized contact resistance of OFETs having PFBT-treated Au electrodes was found to range from 335 to 156 kΩcm for V_{GS} varying between -4 V to -8 V, respectively. Decreased contact resistance leads to improved linearity of the transfer and output characteristics, decreasing values of the threshold voltage, and the I_{on}/I_{off} of OFETs with Au/$Mo(tfd)_3$ and Au/PFBT OFETs are at the same level of 10^4. Reduction in contact resistance values are attributed to $Mo(tfd)_3$ induced p-

doping of the TIPS-pentacene:PTAA blend in the vicinity of the source and drain electrodes, rather than to differences in the work function of the modified Au electrodes. Device modeling on an OFET with Au/$Mo(tfd)_3$ shows good fitting also support this assumption from the theoretical aspect. Our group also studied on different contact treatments on source and drain electrodes and can be found from Choi *et. al.* [111] for comparisons among using $Mo(tfd)_3$, MoO_3, and PFBT.

CHAPTER 6

OFETS ON PAPER

6.1 Introduction

Paper is perhaps the most economical, ecologically-friendly and sustainable material onto which printed electronics can be built upon. OFETs can be fabricated at low-temperatures over large areas and with fabrication methods that are compatible with roll-to-roll processing techniques; widely used in the paper industry. However, fabricating printed electronics on paper is challenging because its fibrillar nature leads to porous films, with a large surface roughness [36], that are not appropriate for the fabrication of the ultrathin layers required for the realization of an OFET. To overcome this problem, two approaches have been proposed in the literature. In the first approach, ionic gate dielectrics (paper-based, ion gels, polymer electrolytes, etc.) have been used for the realization of ion modulated transistors, this approach has been demonstrated using both metal-oxide [112] as well as organic thin-film transistors [113, 114]. In the second approach, a buffer layer (either the gate dielectric or a separate layer coating the paper) is used to reduce its surface roughness [44, 46, 47, 115-122] and to insulate the device structure from chemical impurities on the surface of the substrate [119].

In the literature, most studies report on bottom-gate OFETs on paper [44, 46, 47, 115, 116, 118, 120-122] wherein the gate electrode and gate dielectric planarize the paper's surface on the channel region or, wherein a planarization layer, typically parylene by chemical vapor deposition, is deposited onto the paper's surface prior to the fabrication of the bottom-gate OFET structure. With the exception of recent work by Zschieschang and Klauk [120], which reported on the low voltage operation of bottom-

gate OFETs that use an AlO_x/self-assembled-monolayer gate dielectric, the operational voltage of bottom-gate OFETs on paper has been on the order of tens of volts due to the use of relatively thick gate dielectric layers which lead to small capacitance density values (< 16 nF/cm^2). Although bottom-gate OFETs can display low-voltage operation, high-mobility values and excellent short-term operational stability, the exposure of the semiconductor layer to the ambient will eventually lead to changes of the device performance, which have been exploited to develop sensors but are undesirable when developing electronic circuits. On the other hand, reports on top-gate OFETs on paper are rare. Recently, Mirari, *et. al.* [117] reported on C_8-BTBT-based top-gate OFETs fabricated on inkjet printing paper planarized with parylene. These OFETs displayed high mobility values up to 2.5 cm^2/Vs at operational voltages on the tens of volts range. Although the transfer characteristics of these devices present no hysteresis, no systematic study was conducted on their long-term operational stability.

Despite great progress in recent years, there is still a need to develop approaches that allow OFETs to operate at low voltages and with good stability on paper. Hence, we believe that the use of a top-gate OFET geometry is desirable because, as we have shown, this geometry inherently protects the organic semiconductor layer while at the same time, the gate dielectric can be engineered to enable top-gate OFETs to operate at low voltage values and to display exceptional operational and environmental stability even in aqueous environments [34, 35, 123, 124]; as well as when fabricated on plastic [66] or on CNC substrates [119].

In this chapter, the realization of solution-processed top-gate OFETs fabricated on specialty paper PowerCoat™ HD 230 from Arjowiggins Creative Papers is reported.

PowerCoat™ HD 230, here on referred to as HD 230 paper substrates, is a 200 µm-thick ultra-smooth paper (root-mean squared surface roughness < 20 nm) substrate designed for applications in advanced printed electronics such as high-definition patterning of microelectronics and electroplating. We demonstrate that the use of a buffer layer comprising of a 1:1 wt.% blend of polyvinyl alcohol (PVA) and polyvinylpyrrolidone (PVP) mixture coated leads to the demonstration of high performance top-gate OFETs. PVA and PVP are water-soluble, biodegradable, and low-cost materials that are highly miscible [125] and form polymer blends with very low crystallinity [126]. Top-gate OFETs fabricated on HD 230 paper display low threshold voltage values in the range of -2 to -3 V and high carrier mobility in the range of 0.1-1.0 cm^2/Vs. Furthermore, we also report on the high operational stability of these OFETs by demonstrating high reproducibility during 1000 scans of transfer characteristics and less than 6% source to drain current changes during on-state (at a drain and gate voltage value of -10 V) DC bias stress test for 1 h. This level of electrical performance is comparable to our previous reports on top-gate OFETs fabricated on conventional glass substrates. Finally, initial studies on the mechanical properties of these OFETs also demonstrate that stable electrical properties are retained during bending tests with a small strain of 0.82%.

6.2 Design of Experiments

The goal of this chapter is to demonstrate OFETs on CNC-based paper which is HD 230 from Arjonwiggins. To fabricate OFETs with comparable performance as they were on glass substrates, a buffer layer serving as planarization/barrier/nucleation is required in between the OFET structure and the CNC paper. A buffer layer composed of PVA (Sigma Aldrich) and PVP (Sigma Aldrich) mixture is applied because of its non-

crystallinity and ability for nucleation for the next layer. Furthermore, Al_2O_3 by ALD has been proven a good barrier layer for OFETs on CNC substrates in our previous publication, and in Chapter 4 we also demonstrated that Al_2O_3- and HfO_2-composed NLs provide better OFET environmental stability. To find a best combination for suitable buffer layers, a design of experiment is depicted as Table II including conditions: 1) OFETs directly fabricated on HD 230; 2) OFETs on HD 230 with a PVA:PVP buffer layer; 3) OFETs on glass with a PVA:PVP buffer layer (as a reference for condition 2); 4) OFETs on HD 230 with a buffer layer composed of PVA:PVP/Al_2O_3/NL; 5) OFETs on glass with a buffer layer of PVA:PVP/Al_2O_3/NL (as a reference for condition 4).

Type	Substrate	Buffer layer	OFET geometry
1	PowerCoat™ HD 230	None	Top-gate
2	PowerCoat™ HD 230	PVA:PVP	Top-gate
3	Glass (Corning Eagle 2000)	PVA:PVP	Top-gate
4	PowerCoat™ HD 230	PVA:PVP/Al_2O_3/NL	Top-gate
5	Glass (Corning Eagle 2000)	PVA:PVP/Al_2O_3/NL	Top-gate

Table II. Design of experiments of OFETs on HD 230.

6.3 Device fabrication

Top-gate bottom-contact OFETs were fabricated on Corning glass (Corning Eagle 2000) as reference samples and on HD 230 from Arjonwiggins. OFET structures with nominal thickness in type 1 to 5 are shown in Figure 47. Reference OFETs started from glass substrates cleaning by acetone, distilled water, and isopropanol in an ultrasonic cleaning bath for five min for each step. OFETs on HD 230 started from PDMS preparation as the adhesion layer between HD 230 and glass as holding substrates. PDMS was prepared from Gelest OE 41 base and cross-linker mixture at 1 to 1 weight ratio then spun-coated on 3.8 cm by 3.8 cm glass substrate at 2,000 rpm for 60 s (acceleration: 928

rpm/s) and curing at 80 °C for 1 h to cure PDMS; after PDMS curing, HD 230 substrates were attached to it and secured with Kapton tapes.

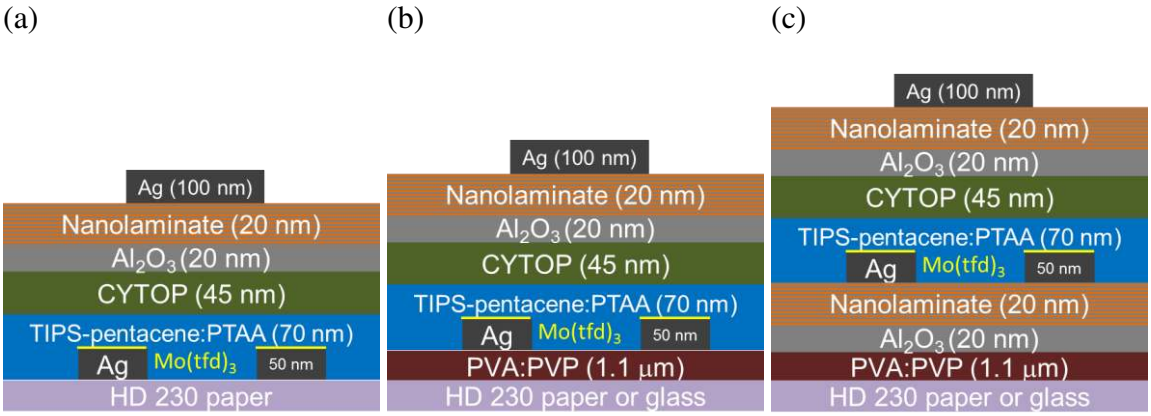


Figure 47. (a) The OFET structure of type 1. (b) The OFET structure of type 2 and 3. (c) The OFET structure of type 4 and 5.

For buffer/barrier layers, 1 to 1 PVA:PVP blend buffer layer prepared from PVA:PVP (7.5 wt.%, 150 mg + 150 mg in 4 mL distilled water) buffer layer coating at 1,000 rpm for 60 s (acceleration: 928 rpm/s) and annealing at 60 °C for five min; ALD-grown NL layers were deposited at 100 °C for 200 cycles of Al_2O_3 and NL (20 times of five cycles of Al_2O_3 and five cycles of HfO_2). Buffer layer coating sequence was prepared as a design of experiments. Later, substrates were deposited with 50 nm-thick Ag as source/drain electrodes through shadow masks in a SPECTROS followed by 1.5 nm of $Mo(tfd)_3$ deposition on source/drain electrodes with the same shadow mask in SPECTROS for contact resistance reduction. On top of source/drain electrodes was a spin-coated organic semiconductor layer: TIPS-pentacene (Sigma Aldrich) and PTAA (Sigma Aldrich) blend. TIPS-pentacene and PTAA blend solution was prepared as follow: TIPS-pentacene and PTAA were weighted by electronic scales (60 mg for each) to put into a bottle and dissolved in 1, 2, 3, 4-Tetrahydronaphthalene anhydrous, 99%, (Sigma Aldrich) (4 mL) for a concentration of 30 mg/mL and stirred overnight by a

magnetic stirrer. Organic layers were spin-coated (filtered with a 0.2 μm filter) at 500 rpm for 10 seconds (acceleration: 500 rpm/s) and 2,000 rpm (acceleration: 1,000 rpm/s) for 20 seconds. The organic film was then annealed at 100°C for 15 minutes. The organic active layer was followed by a CYTOP layer (ca. 45 nm) coating at 3,000 rpm (acceleration: 10,000 rpm/s) for 60 s and annealing at 100 °C for 10 min. To deposit a 45 nm of CYTOP, we needed to dilute the 9% CYTOP (CTL-809M) with CYTOP solvent (CT-SOLV180) by 1 to 3.5 volume ratio to have 2% CYTOP and then spin-coated as described above. After CYTOP coating, 200 cycles of Al_2O_3 and NL were deposited at 100 °C by a Savannah 100 ALD system from Cambridge Nanotech Inc. On top of the CYTOP/NL bilayer gate dielectric, 100 nm of Ag gate electrodes were deposited through a shadow mask by a thermal evaporator.

6.4 Device characterization

All measurements were conducted in a glove box with O_2 and H_2O < 0.1 ppm. Transfer characteristics and output characteristic measured at the pristine condition and statistics of device parameters are summarized in Table III. The channel width and length ratio (W/L) of OFETs is 2550 μm/180 μm.

Type	Buffer layer	Substrates	μ (cm^2/Vs)	V_{TH} (V)	I_{ON}/I_{OFF}	Yield
1	None	HD 230	$3.7 \pm 2.1 \times 10^{-4}$	-3.0 ± 1.9	2.2×10^{2}	8/10
2	PVA:PVP	HD 230	$1.7 \pm 1.1 \times 10^{-1}$	-1.4 ± 0.2	2.3×10^{5}	7/8
3	PVA:PVP	Glass	$1.6 \pm 0.6 \times 10^{-1}$	-4.1 ± 0.4	1.2×10^{5}	10/10
4	PVA:PVP/Al_2O_3/NL	HD 230	$5.8 \pm 3.8 \times 10^{-2}$	-0.8 ± 0.2	3.4×10^{4}	9/10
5	PVA:PVP/Al_2O_3/NL	Glass	$6.6 \pm 1.5 \times 10^{-1}$	-2.0 ± 0.3	3.7×10^{5}	7/10

Table III. Statistics of OFETs in each type.

6.4.1 Pristine condition in nitrogen

Representative OFETs in different conditions are shown in the following figures.

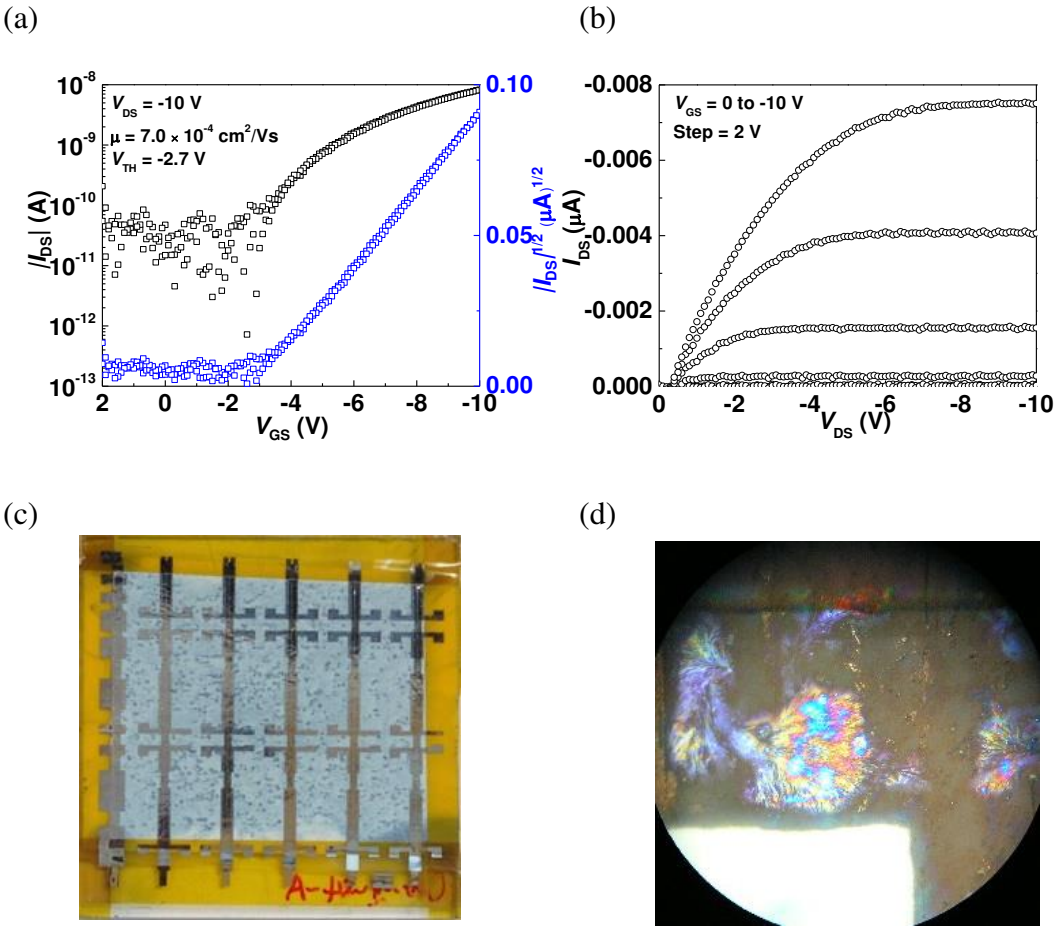
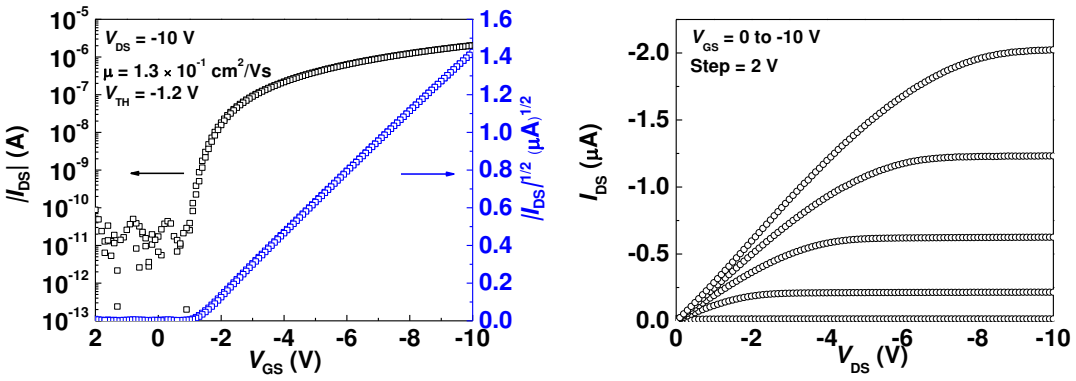


Figure 48. OFETs on bare HD 230 (a) Transfer characteristics (b) Output characteristics (c) A photograph of OFETs from type 1 (d) A 500× microscope image of an OFET from type 1.

Figure 48 displays characteristic of a representative OFET of type 1, OFETs on bare CNC paper. Figure 48 (a), transfer characteristics, shows drain current (left axis, black) and the square root of drain current (right axis, blue) as a function of gate voltage at a given drain voltage, and carrier mobility, threshold voltage, and on/off current ratio can be extracted from the relation between the square root of drain current and the drain voltage; Figure 48 (b), output characteristics, shows drain current as a function of drain voltage at given gate voltages from 0 to -10 V with a step of 2 V. The carrier mobility is as low as 10^{-4} cm^2/Vs level, and drain current is at nA range. Figure 48 (c) is a photo

image of organic semiconductor (OSC) film displaying scattered drops of OSC, and poor film quality contributes to poor OFET performance. Figure 48 (d) is a 500× microscope image in between orthogonal polarizers showing no crystalline film.

(a) (b)



(c) (d)

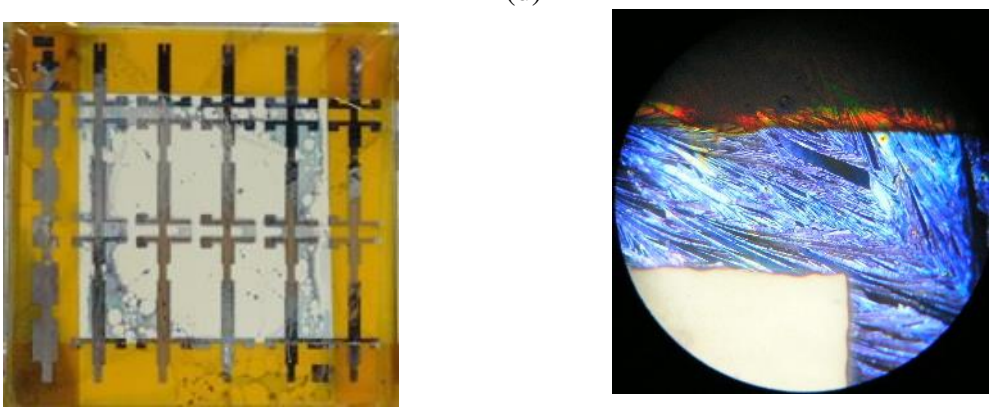


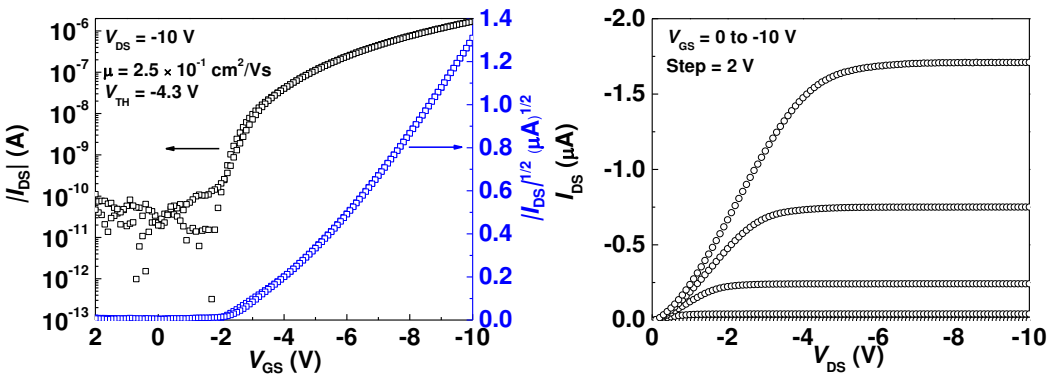
Figure 49. OFETs on PVA:PVP-coated HD 230. (a) Transfer characteristics. (b) Output characteristics. (c) A photograph of OFETs from type 2. (d) A 500× microscope image of an OFET from type 2.

Figure 49 displays characteristics of a representative OFET in type 2, OFETs on CNC paper with PVA:PVP buffer. The average carrier mobility is 0.17 cm^2/Vs, and average threshold voltage is -1.4 V. Figure 49 (a), transfer characteristics, provides extracted carrier mobility at 0.13 cm^2/Vs which is at the same range (0.1-1.0 cm^2/Vs) we reported for this OFET structure on glass; Figure 49 (b), output characteristics, shows

linear increased drain current at low drain voltage representing low energy barrier between the work function of source/drain contact and the IP of the organic semiconductor layer. Figure 49 (c) is a photo image displaying severe dewetting of OSC film on CNC paper with PVA:PVP buffer, and only source/drain area surrounded by OSC. However, Figure 49 (d), a 500× microscope image in between orthogonal polarizers, shows highly crystalized OSC film in channel area contributes to OFETs with best performance on CNC paper, and that is similar to performance of OFETs on glass substrates.

Meanwhile, a representative OFET in type 3, OFETs on glass with PVA:PVP buffer (reference to type 2) is shown in Figure 50. The average carrier mobility is 0.16 cm^2/Vs, and average threshold voltage is -4.1 V. Figure 50 (a), transfer characteristics, provides extracted carrier mobility at 0.25 cm^2/Vs; Figure 50 (b), output characteristics, shows non-linear increased drain current at low drain voltage representing barrier between the work function of source/drain contact and the IP of organic semiconductor layer. Figure 50 (c) is a photo image displaying severe dewetting of organic OSC film on glass with PVA:PVP buffer, and only source/drain area surrounded by OSC. This is similar to condition 2, and again Figure 50 (d), a 500× microscope image in between orthogonal polarizers, shows highly crystalized OSC film in channel area. However, OFETs in this condition show inferior performance to type 2. In conditions of OFETs with a PVA:PVP buffer on CNC paper and on glass (as reference), PVA:PVP provides a good buffer for OFET fabrication on CNC paper and this buffer layer provides superior OFET performance on CNC paper than that on glass although worse dewetting of OSC film was observed after PVA:PVP buffer applied.

(a) (b)



(c) (d)

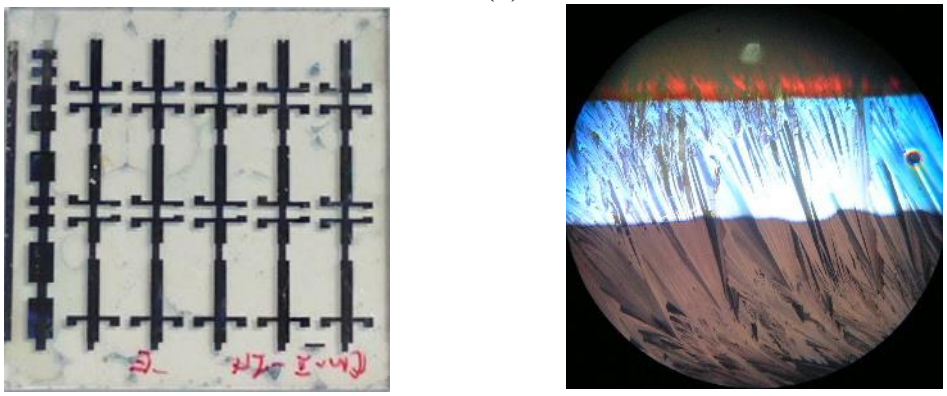
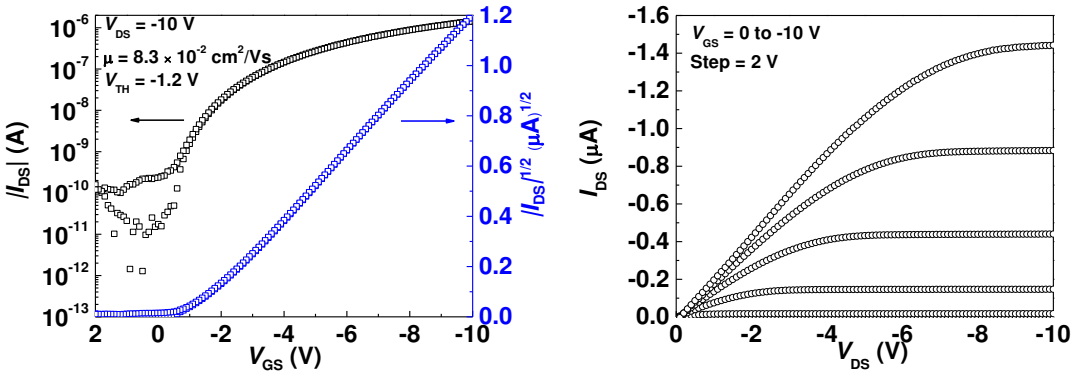


Figure 50. OFETs on PVA:PVP-coated glass. (a) Transfer characteristics. (b) Output characteristics. (c) A photograph of OFETs from type 3. (d) A 500× microscope image of an OFET from type 3.

The other buffer layer is composed of PVA:PVP/Al_2O_3/NL, and a representative OFET in type 4, OFETs on CNC paper with PVA:PVP/Al_2O_3/NL buffer, is shown in Figure 51. The average carrier mobility is 0.06 cm^2/Vs, and average threshold voltage is -0.8 V. Figure 51 (a), transfer characteristics, provides extracted carrier mobility at 0.08 cm^2/Vs which is lower than that in type 2, OFETs on CNC paper with PVA:PVP buffer; Figure 51 (b), output characteristics, also shows linear increased drain current at low drain voltage similar to type 2. Figure 51 (c) displays improved wetting of organic OSC film on CNC paper with PVA:PVP/Al_2O_3/NL buffer, but less crystalized OSC film is

observed under a 500× microscope image in between orthogonal polarizers in Figure 51 (d). Even with improved wetting of film, OFETs in this condition shows inferior performance to type 2 because of the less crystalized OSC film.

(a) (b)



(c) (d)

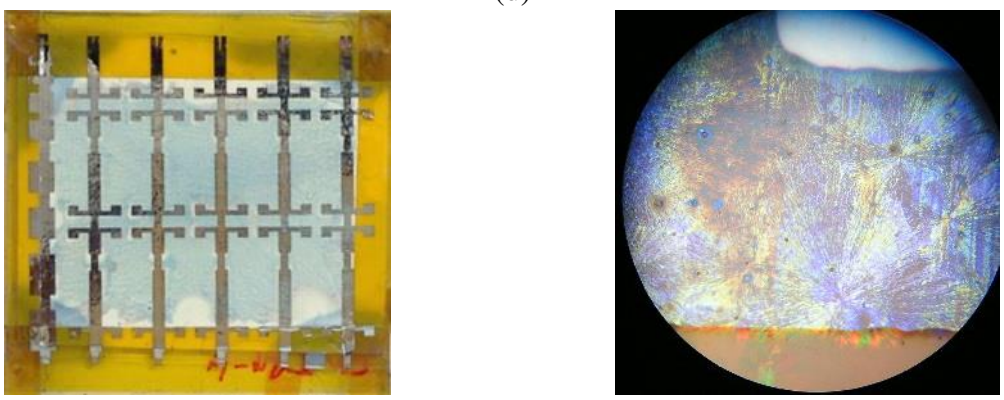
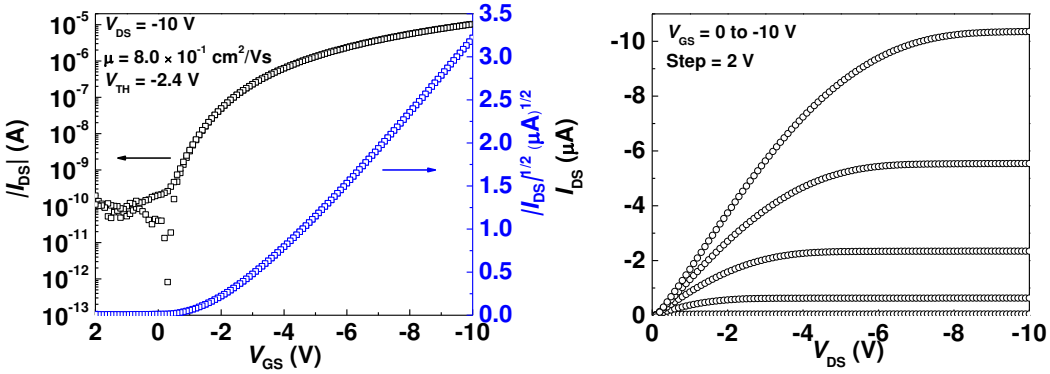


Figure 51. OFETs on PVA:PVP/NL-coated HD 230. (a) Transfer characteristics. (b) Output characteristics. (c) A photograph of OFETs from type 4. (d) A 500× microscope image of an OFET from type 4.

In type 5, a representative OFET on glass with PVA:PVP/Al_2O_3/NL buffer (reference to type 4), is shown in Figure 52. The average carrier mobility is 0.66 cm^2/Vs, and average threshold voltage is -2.0 V. Figure 52 (a), transfer characteristics, provides extracted carrier mobility at 0.80 cm^2/Vs; Figure 52 (b), output characteristics, shows linear increased drain current at low drain voltage similar to type 2. Figure 52 (c) also displays improved wetting of organic OSC film on glass with PVA:PVP/Al_2O_3/NL

buffer, and highly crystalized OSC film is also observed under a 500× microscope image in between orthogonal polarizers in Figure 52 (d). OFETs with a PVA:PVP/Al_2O_3/NL buffer on CNC paper, HD 230, and on glass (as reference) indicate that PVA:PVP/Al_2O_3/NL buffer improved wetting on both HD 230 and glass. However, PVA:PVP served as nucleation layer for Al_2O_3/NL only works on glass substrate instead of CNC paper. Highly crystalized and homogeneous wetted OSC film in this condition contribute to OFETs with highest carrier mobility among this design of experiments.

(a) (b)



(c) (d)

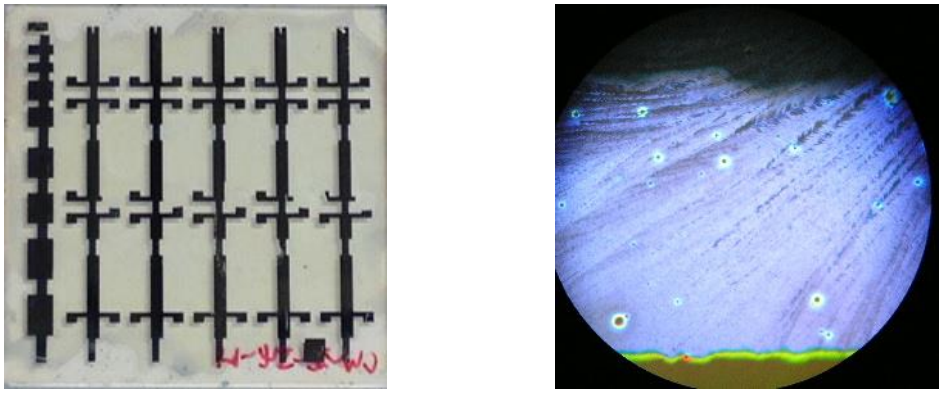
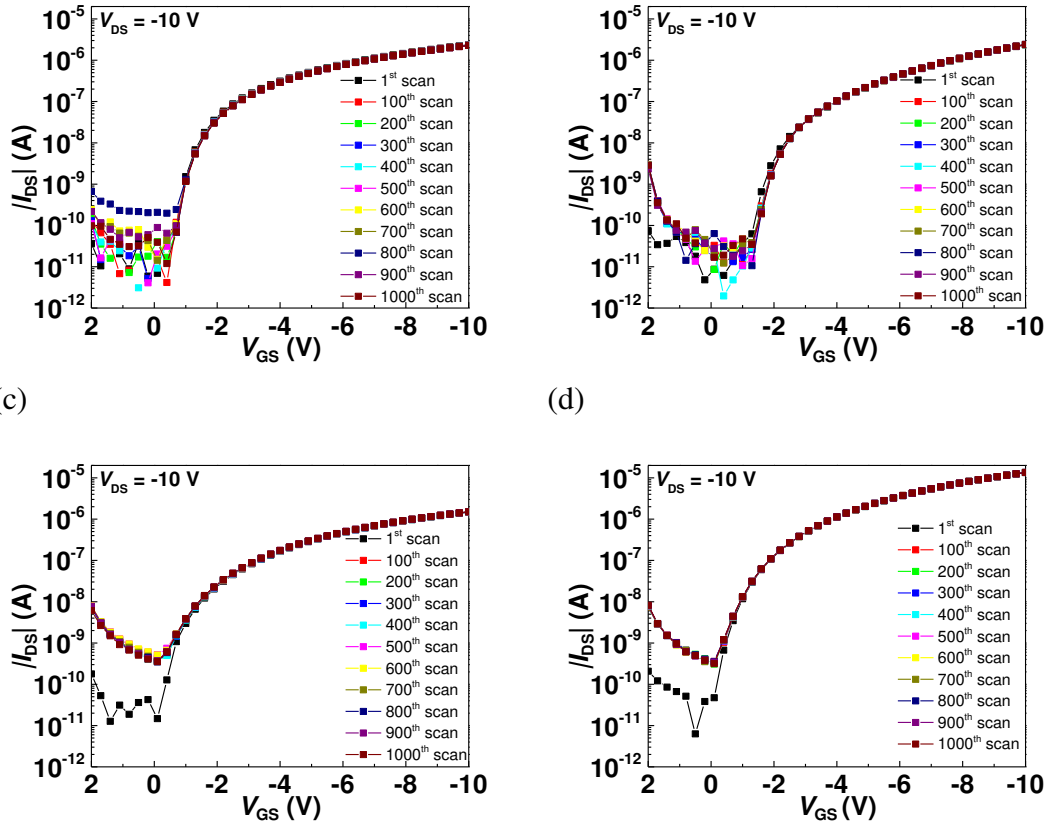


Figure 52. OFETs on PVA:PVP/NL-coated glass. (a) Transfer characteristics. (b) Output characteristics. (c) A photograph of OFETs from type 5. (d) A 500× microscope image of an OFET from type 5.

6.4.2 Operational stability in nitrogen

The operational stability was tested by 1,000 times of transfer characteristic scans and DC bias stress at V_{DS} = V_{GS} = -10 V on each representative OFET. Figure 53 displays 1,000 scans of transfer characteristic of OFETs from type 2 to 5, and type 1 is skipped because of its poor performance. OFETs on PVA:PVP buffer has less increased off-current shown in Figure 53 (a) on CNC paper and Figure 53 (b) on glass; OFETs on PVA:PVP/Al_2O_3/NL buffer has the same low off current at the beginning, and later they have stabilized off current with small increment shown in Figure 53 (c) on CNC paper and Figure 53 (d) on glass. Overall OFETs have stable operational stability when 1,000 scans are applied on each of them.

(a) (b)



(c) (d)

Figure 53. Comparison of 1,000 consecutive scans of the transfer characteristics of type 2-5 top-gate OFETs.

Another operational stability test shown in Figure 54 is the DC bias stress measurement. OFETs were biased at on-state at V_{DS} = V_{GS} = -10 V for 1 h, and on-current variation is less than 4%. From this design of experiments we can tell that OFETs were successfully demonstrated on CNC paper with optimized buffer layer on top of the CNC paper.

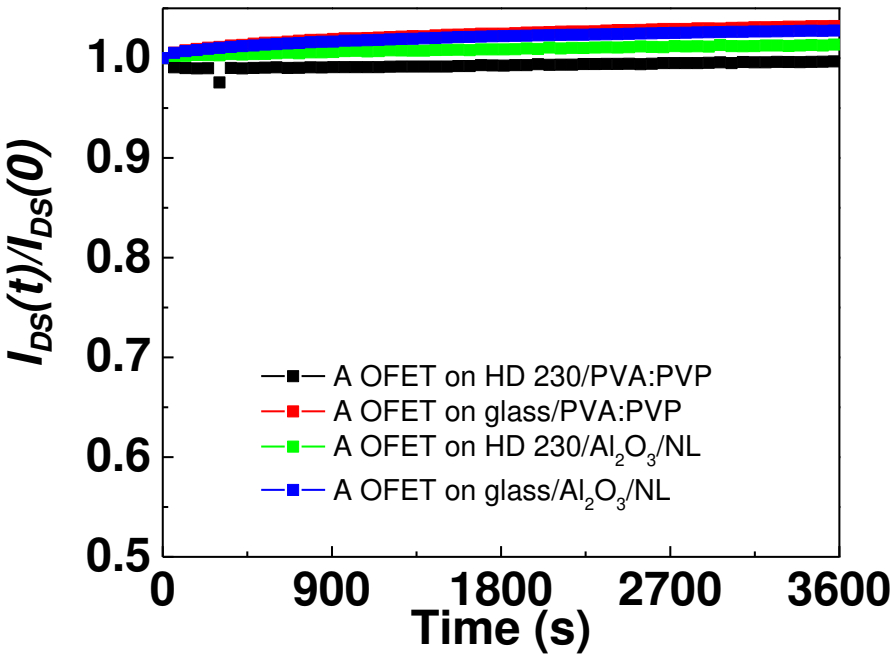


Figure 54. DC bias stress tests of type 2-5 top-gate OFETs.

6.4.3 Bending tests in nitrogen

The other operational stability test involved measuring OFETs under a bending condition of radius of curvature equaling to 13.5 mm. The substrate of HD 230 is 0.222 mm, there the strain is 0.82% calculated from dividing the substrate thickness by twice the radius of curvature. The bending direction is parallel to the channel of OFETs. The condition used in this bending test is the same as our previous study [66] to compare

similar OFET structures on different substrates. The set-up of this bending test is shown in Figure 55.

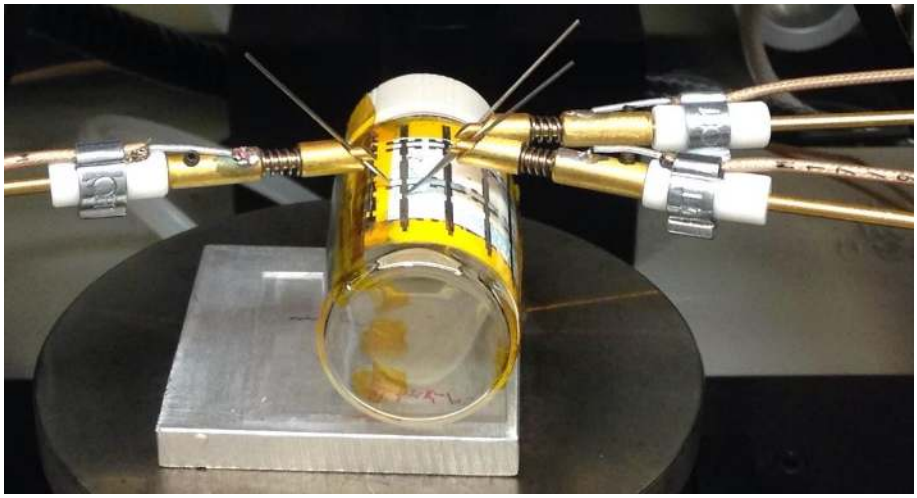


Figure 55. The set-up of bending tests for OFETs on paper.

OFETs on paper coated with PVA:PVP (type2) and PVA:PVP/Al_2O_3/NL (type 4) were both tested. Figure 56 displays transfer characteristics and output characteristics on a type-2 OFET in a bending test. In this bending test, slight degradation was found during the test and it was exciting because OFETs on flexible recyclable substrates were demonstrated. The extracted parameters such as carrier mobility, threshold voltage, and on/off current ratio were summarized in Table IV.

(a) (b)

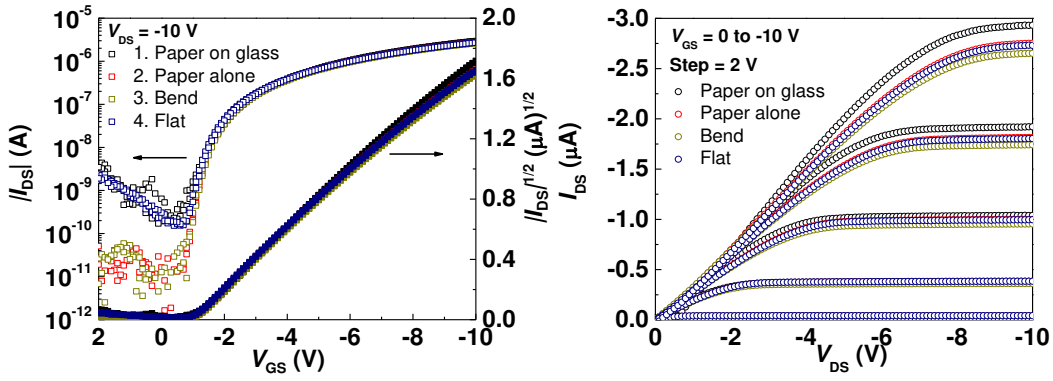


Figure 56. A type-2 OFET in a bending test. (a) Transfer characteristics. (b) Output characteristics.

Conditions	μ (cm^2/Vs)	V_{TH} (V)	I_{ON}/I_{OFF}
On paper attached on glass	2.2×10^{-1}	-1.1	4.1×10^{3}
On paper	2.1×10^{-1}	-1.0	2.3×10^{5}
Bending	2.0×10^{-1}	-1.0	2.2×10^{5}
After bending	2.0×10^{-1}	-0.9	1.1×10^{4}

Table IV. Parameters of a type-2 OFET in the bending test

In Table IV, a representative type-2 OFET had a slightly degraded carrier mobility from 0.22 to 0.20 cm^2/Vs, slightly changed threshold voltage from -1.1 to -0.9 V, and on/off current ratio varied in the range of 10^3 to 10^5. Statistical data of type-2 OFETs in the bending test is displayed in Table V. It provides information that type-2 OFETs with high yield and small variation during the bending test. The yield of OFETs is eight out of eight through the entire bending test. Average carrier mobility slightly degraded from 0.15 ± 0.09 to 0.12 ± 0.08 cm^2/Vs, and average threshold voltage slightly changed from -1.2 ± 0.2 to -0.9 ± 0.2 V. On/off current ratio stayed at the range of 10^4.

Conditions	μ (cm^2/Vs)	V_{TH} (V)	I_{ON}/I_{OFF}	Yield
On paper attached on glass	$1.5 \pm 0.9 \times 10^{-1}$	-1.2 ± 0.2	3.3×10^{4}	8/8
On paper	$1.4 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.1	5.7×10^{4}	8/8
Bending	$1.2 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.2	4.7×10^{4}	8/8
After bending	$1.2 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.2	1.2×10^{4}	8/8

Table V. Statistical data of type-2 OFETs in the bending test

In contrast, type-4 OFETs cannot sustain through the bending test. Only a type-4 OFET shows recoverable transfer characteristics and output characteristics after a bending test in Figure 57. Even recoverable performance was observed, severe degradation happened while the type-4 OFET was bending. None of the rest of type-4 OFETs worked functionally during and after the bending test. This bending test confirmed that PVA:PVP is the better buffer layer compared to PVA:PVP/Al_2O_3/NL.

(a) (b)

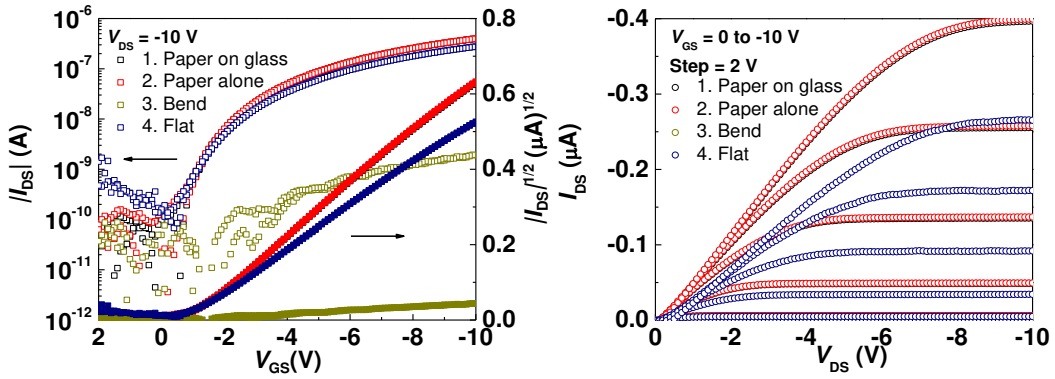


Figure 57. A type-4 OFET in a bending test. (a) Transfer characteristics. (b) Output characteristics.

6.5 Device modeling

The same software and model are applied in this section for device modeling. Figure 58 displays the fitting of a type-2 OFET, the best combination in this design of experiment. Extracted μ and V_{TH} were 0.39 cm^2/Vs and -1.6 V. Fitted SS is 0.20 V/decade, and the corresponding defect density D_{it} calculated by equation (6) is 4×10^{11} cm^{-2}. Empirical parameters such as V_{aa}, γ, and λ are 115 V, 0.02, and 0.005 respectively.

(a) (b)

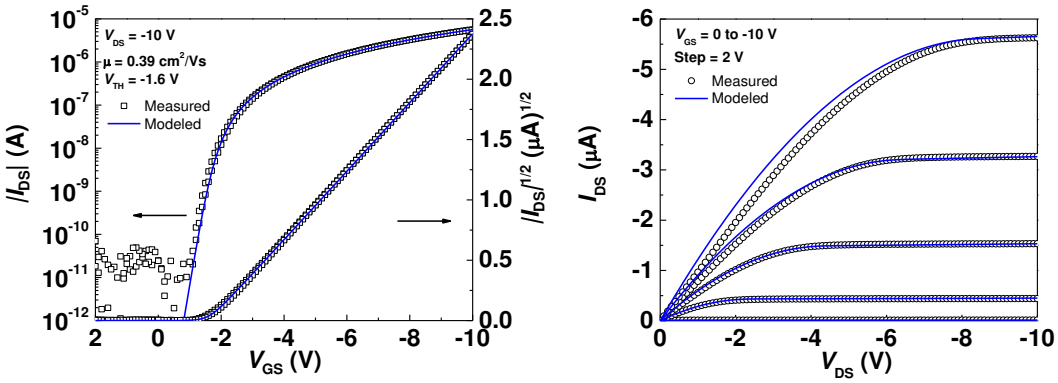


Figure 58. (a) Fitting of transfer characteristics on a type-2 OFET. (b) Fitting of output characteristics on a type-2 OFET.

The current-voltage characteristics follow the model and only a slightly difference between the measured data and model at the transition from linear regime to saturation regime at high gate-to-source bias voltage as shown in Figure 58 (b).

6.6 Summary

In this chapter, top-gate OFETs using TIPS-pentacene:PTAA blend as an organic semiconducting layer have been demonstrated on CNC-based paper PowerCoat^{TM} HD 230. Different buffer layers deposited on HD 230 were applied in top-gate OFETs including PVA:PVP blend and PVA:PVP/Al_2O_3/NL. OFETs on HD 230 showed average carrier mobility of $1.7 \pm 1.1 \times 10^{-1}$ cm^2/Vs, $5.8 \pm 3.8 \times 10^{-2}$ cm^2/Vs, and $3.7 \pm 2.1 \times 10^{-4}$ cm^2/Vs with PVA:PVP, PVA:PVP/Al_2O_3/NL, and no buffer layer that assured buffer layers improved device performance. Threshold voltage decrement (from -3.0 ± 1.9 V to -1.4 ± 0.2 V and -0.8 ± 0.2 V) and on/off current ratio increment (from 10^2 to 10^4 or 10^5) on OFETs were also observed when buffer layers were applied. Stable operational stability was demonstrated by conducting 1,000 scans of transfer characteristics and a 1 h DC bias stress of OFETs with buffer layer on HD 230. All conditions displayed stable performance for these two operational stability tests. Furthermore, only OFETs with PVA:PVP work functionally during and after a bending test. Between these two buffer layers, PVA:PVP provides better performance for OFETs, and larger crystallinity observed on the channel area even though the semiconductor film showed dewetting on HD 230.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This dissertation reported solution-processed high-performance top-gate OFETs with highly operational and environmental stability on novel renewable substrates. Chapter 3 described top-gate OFETs with a bilayer CYTOP/Al_2O_3 gate dielectric on environmentally friendly renewable CNC:glycerol substrates. OFETs fabricated on bare water soluble CNC:glycerol substrates served as a control group, and OFETs on CNC:glycerol with an ALD-grown Al_2O_3 buffer/barrier layer served as an experimental group. We found that with a buffer/barrier layer of ALD-grown Al_2O_3 on top of bare CNC:glycerol substrates, it prolonged the process of CNC:glycerol dissolving in water and further realized solution-processed organic electronics fabrication meanwhile previous results of OPVs [38, 39] and OLEDs [40] fabricated on CNC:glycerol substrates used dry process. This work is also one of the scare reports of high-performance solution-processed OFETs on cellulose material substrates [44]. Operational stability was demonstrated by conducting 1,000 scans of transfer characteristics that very few reports addressed [44], and we are the only group demonstrating normally-off OFETs on cellulose substrates with such operational stability.

OFETs fabricated on CNC:glycerol with an Al_2O_3 buffer layer displayed comparable average carrier mobility at 0.11 cm^2/Vs and average threshold voltage at -2.1 V to that of OFETs on glass [34, 35] and plastic [66] substrates. Meanwhile, the control group had average carrier mobility at 0.06 cm^2/Vs and average threshold voltage at -1.0 V. In various aspects of performance comparison, OFETs fabricated on CNC:glycerol

with an Al_2O_3 buffer layer, the experimental group, displayed superior performance in conditions such as storing in nitrogen for one month, stressing OFETs on on-state for 1 h, measuring higher on/off current ratio in 1,000 scans of transfer characteristics in both nitrogen and air, and especially storing OFETs in air to test their environmental stability. The assumption of the origin of instability in the control group are by-products produced during the CNC:glycerol synthesis introducing sodium cations and sulfur anions, and the assumption was confirmed by XPS measurements on bare CNC:glycerol and CNC:glycerol coated with ALD-grown Al_2O_3 showing byproducts only detected on bare CNC:glycerol substrates. It assures that a barrier/buffer layer is necessary for OFETs on novel substrates.

Chapter 4 described developing a nanolaminate structure comprised of Al_2O_3 and HfO_2 to replace Al_2O_3 in the gate dielectric bilayer in top-gate OFETs to improve their environmental stability while maintaining comparable operational stability. ALD-grown Al_2O_3 was known to be corroded in hot water [77], and nanolaminate structure was discovered superior barrier properties than a single layer of ALD-grown metal oxide layer [77-79]. We discovered that by integrating the nanolaminate structure in our bilayer gate dielectric layer in OFETs, the electrical properties were preserved, and environmental properties were superior in extreme conditions such as in water at 95 °C. Compared to Someya *et al.* [32, 33] using either a stable organic semiconductor or a μm-thick encapsulation layer for OFETs sustain at temperature above 100 °C, we can use a thin layer with thickness less than 100 nm to preserve OFETs' characteristics for tens of minutes at temperature close to 100 °C broadening the applications of our OFETs. OFETs with modified gate dielectric were first measured in pristine conditions to confirm

comparable electrical properties with average carrier mobility at 0.9 cm^2/Vs and average threshold voltage at -1.9 V. After that, stable operational stability was demonstrated in air by measuring DC stress on on-state for 1 h with less than 3% variation of on-current; stable environmental stability was demonstrated by storing OFETs in various environments such as air, vacuum annealing at 100 °C, 80% relative humidity, water at room temperature, and water at 50 °C with stable average carrier mobility changed only from 0.9 cm^2/Vs to 0.8 cm^2/Vs and reproducible average threshold voltage after storing in different environments followed by vacuum annealing. All of these tests displayed comparable device performance of OFETs with modified CYTOP/NL gate dielectric to that of OFETs with the original CYTOP/Al_2O_3 gate dielectric. Harsher environmental stability was tested in water at 95 °C displaying a huge difference between OFETs with CYTOP/Al_2O_3 and CYTOP/NL gate dielectric. OFETs with modified CYTOP/NL gate dielectric can sustain in water at 95 °C for 1 h without average carrier mobility change. In contrast, OFETs with original CYTOP/Al_2O_3 gate dielectric only worked in the first three minutes while immersed in water at 95 °C. Further barrier property investigations of these two dielectrics were demonstrated by encapsulating Ca and immersing in water at 95 °C to monitor the oxidation of Ca during the test. From the photographs of Ca encapsulated by these two dielectrics in hot water immersion tests, similar durability of CYTOP/Al_2O_3 and CYTOP/NL was observed.

Chapter 5 described reduction of contact resistance on our top-gate OFETs platform by depositing 1.5 nm of $Mo(tfd)_3$ on source and drain electrodes. OFETs were fabricated in three conditions: 1) no contact treatment, 2) conventional PFBT contact treatment, 3) $Mo(tfd)_3$ on top of contacts. Increased on-current and decreased threshold

voltage were observed on OFETs with $Mo(tfd)_3$ treatment compared to PFBT treatment; OFETs without contact treatment displayed poor results with lowest on-current and highest threshold voltage. Reduced contact resistance on OFETs with $Mo(tfd)_3$ treatment can be observed on more linear output characteristics close to origin. Extracted contact resistance on OFETs with $Mo(tfd)_3$ treatment is 34 kΩcm, approximately one fifth of that on OFETs with PFBT treatment, 156 kΩcm, at on-state with gate voltage at -8 V with the same range of on/off current ratio. This study provides a dry process for OFETs on novel substrates that avoiding damages of novel substrates during a long wet process of contact treatment. Further comparison between $Mo(tfd)_3$ and MoO_3 done by our lab can be referred to reference 95.

Chapter 6 described top-gate OFETs on cellulose-based paper substrates with modified gate dielectric discussed in Chapter 4 and reduced contact resistance discussed in Chapter 5. We discovered that by using a buffer layer of PVA:PVP, OFETs have comparable performance as that of them fabricated on glass substrates. In literatures, many bottom-gate OFETs on paper-based substrates have been reported on many applications including memories [47] and display drivers [118], but they usually operated at voltages higher than 10 V. Top-gate OFETs were reported scarcely, Mirari *et. al.* [117] reported top-gate OFETs using a C_8-BTBT-based organic semiconductor layer on inkjet printing paper planarized with parylene. These OFETs had high mobility values up to 2.5 cm^2/Vs, they were operated at large operational voltage with a normally-on characteristic. Meanwhile we demonstrated OFETs with low-voltage operation and normally-off characteristics. A systematically study of operational stability, in Chapter 6, was also usually lack in most of the OFETs fabricated on paper. OFETs on bare paper were the

control group, and two kinds of buffer layers prepared on top of this paper: PVA:PVP and PVA:PVP/NL. The PVA:PVP is here because of its non-crystallinity and ability to serve as a nucleation layer for the organic semiconductor layer; the NL is here because of its proven superior environmental barrier properties described in Chapter 3. On paper substrates, the best crystallinity of TIPS-pentacene:PTAA blend organic semiconductor layer was found on OFETs fabricated on paper with PVA:PVP coating, thought it had a dewetting issue; on glass substrates as references, the dewetting issue was also found on OFETs on PVA:PVP-coated glass, and the best crystallinity was found on OFETs on PVA:PVP/NL-coated glass. Carrier mobility was positively correlated to the crystallinity. Therefore, OFETs on PVA:PVP-coated paper can achieve highest average carrier mobility, 0.17 cm^2/Vs, among OFETs on paper with different buffer layers; OFETs on PVA:PVP/NL coated glass have higher average carrier mobility, 0.66 cm^2/Vs, compared to that of OFETs on PVA:PVP coated glass, 0.17 cm^2/Vs. Even OFETs on different buffer layers have similar operational stability by demonstrating stable transfer characteristics for 1,000 cycles and less than 6% change of on-state DC bias stress for 1 h, only OFETs with PVA:PVP work functionally during and after a bending test with a stain of 0.82%. Among these two buffer layers, PVA:PVP is a better buffer layer because of better OFET performance and larger crystallinity observed on channel area even though the semiconductor film showed dewetting on HD 230.

7.2 Recommendations for future work

The recommended future works based on this dissertation can be divided into several parts: interface property, crystallinity, gate dielectric, and mechanical test.

7.2.1 Interface property and crystallinity

In Chapter 3 and Chapter 6, OFETs were fabricated on CNC:glycerol substrates and CNC-based paper respectively. Both cases yielded comparable average carrier mobility values of 0.1 to 0.2 cm^2/Vs and constant resistance near the origin in output characteristics. However, there was no contact treatment of OFETs on CNC:glycerol, and a contact treatment of a layer of $Mo(tfd)_3$ was deposited on OFETs on CNC-based paper. The interface property played an important role for OFETs on different substrates affecting the arrangement of organic semiconductor molecules. Therefore, OFETs without any contact treatment on CNC:glycerol had comparable carrier mobility to that of OFETs with $Mo(tfd)_3$ contact treatment on CNC-based paper. Furthermore, OFETs on CNC-based paper had different crystallinity resulting in different carrier mobility when different buffer layers were applied on CNC-based substrates. The wettability of organic semiconductor film on different substrates will be a good starting point to explore physical and chemical interaction in interface. After that, X-ray diffraction can provide crystallinity of organic semiconductor films on different buffer layers on various substrates. Then, carrier mobility and contact resistance can be correlated to the crystallinity and even wettability.

7.2.2 Gate dielectric

In Chapter 4, a CYTOP/NL gate dielectric was applied to have superior environmental stability on OFETs. From various reports, NL has been shown to have a

denser metal oxide dielectric layer [127] and lower VWTR [128] in many applications. Developing a method to determine the pinhole density will provide a more direct evidence for denser dielectric and lower VWTR. A fully planned study of trying different single layers of dielectric serving as gate dielectric will also be valuable because it can provide the permeability of these dielectrics and insight into the NL structure. Another important aspect is to optimize the thickness of the gate dielectric. Having a thinner gate dielectric, lower threshold voltage can be achieved because of higher capacitance density, and less material can be put into this layer preparation.

7.2.3 Mechanical tests

Mechanical tests such as the bending test is always attractive to organic electronics for the potential use of flexible electronics. Several reports demonstrated the flexibility of OFETs on CNF [44], specialty paper [47, 115], etc. On our platform, we have demonstrated the potential of our OFETs on flexible substrates [66]. In Chapter 6, OFETs were fabricated on CNC-based paper substrates with comparable electrical properties and operational stability. Only OFETs with a PVA:PVP buffer layer on paper worked functionally during and after the bending test. An extended study can be done by choosing a thinner thickness of the CNC-based paper to test if OFETs with PVA:PVP/NL work when smaller strain is applied. A thinner paper will provide less strain while the bending test is conducted because the strain equals to substrate thickness divided by twice the radius of curvature. Since paper substrate may create cracks during bending, less strain will prevent potential damages by cracks on the substrates during the bending test.

7.3 Publications

7.3.1 Journal publications

1. C. -Y. Wang, C. Fuentes-Hernandez, W. -F. Chou, B. Kippelen, *"Operational stable low-voltage operation top-gate organic field-effect transistors on cellulose-based paper substrates,"* under review by Org. Electron., 2016

2. C. -Y. Wang, C. Fuentes-Hernandez, M. Yun, A. Singh, A. Dindar, S. Choi, S. Graham, B. Kippelen, *"Organic field-effect transistors with a bilayer gate dielectric comprising an oxide nanolaminate grown by atomic layer deposition,"* ACS Appl. Mater. Interfaces, 2016

3. C. -Y. Wang, C. Fuentes-Hernandez, J. -C. Liu, A. Dindar, S. Choi, J. P. Youngblood, R. J. Moon, B. Kippelen, *"Stable low-voltage operation top-gate organic field-effect transistors on cellulose nanocrystal substrates,"* ACS Appl. Mater. Interfaces, v 7, no 8, 2015

4. H. Kim, A. Singh, C. -Y. Wang, C. Fuentes-Hernandez, B. Kippelen, S. Graham, *"Experimental investigation of defect-assisted and intrinsic water vapor permeation through ultrabarrier films,"* Rev. Sci. Instrum., v 87, no 3, 2016

5. B. Fu, C. -Y. Wang, B. D. Rose, Y. Jiang, M. Chang, P. -H. Chu, Z. Yuan, C. Fuentes-Hernandez, B. Kippelen, JL. Bredas, D. M. Collard, E. Reichmanis, "*Molecular engineering of nonhalogenated solution-processable bithiazole-based electron-transport polymeric semiconductors*," Chem. Mater., v 27, no 8, 2015

6. A. Bulusu, A. Singh, C. -Y. Wang, A. Dindar, C. Fuentes-Hernandez, H. Kim, D. Cullen, B. Kippelen, S. Graham, *"Engineering the mechanical properties of ultrabarrier*

films grown by atomic layer deposition for the encapsulation of printed electronics," J. Appl. Phys., v 118, no 085501, 2015

7. S. Choi, C. Fuentes-Hernandez, M. Yun, A. Dindar, T. M. Khan, C. -Y. Wang, B. Kippelen, "*Organic field-effect transistor circuits using atomic layer deposited gate dielectrics patterned by reverse stamping*," Org. Electron. v 15, no 12, 2014

8. R. R. Dasari, A. Dindar, C. K. Lo, C. -Y. Wang, C. Quinton, S. Singh, S. Barlow, C. Fuentes-Hernandez, J. R. Reynolds, B. Kippelen, S. R. Marder, "*Tetracyano isoindigo small molecules and their use in n-channel organic field-effect transistors*," Phys. Chem. Chen. Phys. v 16, no 36, 2014

9. Y. A. Getmanenko, S. Singh, B. Sandhu, C. -Y. Wang, T. Timofeeva, B. Kippelen, S. R. Marder, "*Pyrrole[3,2-d:4,5-d']bisthiazole-bridged bis(naphthalene diimide)s as electron-transport materials*," J. Mater. Chem. C, v 2, no 1, 2014

7.3.2 Conference publications

1. C. -Y. Wang, C. Fuentes-Hernandez, M. Yun, A. Singh, A. Dindar, S. Choi, S. Graham, B. Kippelen, "*Highly stable organic field-effect transistors with bilayer gate dielectric comprised of a perfluorinated polymer and a metal-oxide nanolaminate,"* 58th Electronic Materials Conference, Newark, Delaware, 2016

2. C. -Y. Wang, C. Fuentes-Hernandez, J. -C. Liu, A. Dindar, S. Choi, J. P. Youngblood, R. J. Moon, B. Kippelen, *"Stable top-gate organic field-effect transistors on cellulose nanocrystal substrates,"* TAPPI International Conference on Nanotechnology for Renewable Materials, Atlanta, Georgia, 2015

3. S. Choi, C. Fuentes-Hernandez, C. -Y. Wang, A. Wei, W. Voit, Y. Zhang, S. Barlow, S. R. Marder, and B. Kippelen, *"Top-Gate Organic Field-Effect Transistors Fabricated on Shape-Memory Polymer Substrates,"* SPIE , San Diego, California, 2015

4. S. Choi, C. Fuentes-Hernandez, M. Yun, A. Dindar, T. M. Khan, C. -Y. Wang, B. Kippelen, *"Organic field-effect transistor with electrode interconnections using reverse stamping,"* SPIE, San Diego, California, 2014

REFERENCES

1. Ahn, B.Y., et al., *Omnidirectional Printing of Flexible, Stretchable, and Spanning Silver Microelectrodes.* Science, 2009. **323**(5921): p. 1590.

2. Chen, C.-W., et al., *Development of high-efficiency large-area screen-printed solar cells on direct kerfless epitaxially grown monocrystalline Si wafer and structure.* Progress in Photovoltaics: Research and Applications, 2016. **24**(8): p. 1133-1141.

3. https://infinitypv.com/infinitypro/opv, 2016. **Accessed**.

4. http://www.idtechex.com/research/reports/printed-organic-and-flexible-electronics-forecasts-players-and-opportunities-2016-2026-000457.asp, 2016. **Accessed**.

5. Brédas, J.L., et al., *Organic semiconductors: A theoretical characterization of the basic parameters governing charge transport.* Proceedings of the National Academy of Sciences, 2002. **99**(9): p. 5804-5809.

6. Edgar, L.J., *Method and apparatus for controlling electric currents*. 1930, Edgar, Lilienfeld Julius: United States.

7. Atalla, M.M., E. Tannenbaum, and E.J. Scheibner, *Stabilization of Silicon Surfaces by Thermally Grown Oxides*.* Bell System Technical Journal, 1959. **38**(3): p. 749-783.

8. Chiang, C.K., et al., *Electrical Conductivity in Doped Polyacetylene.* Physical Review Letters, 1977. **39**(17): p. 1098-1101.

9. Ebisawa, F., T. Kurokawa, and S. Nara, *Electrical properties of polyacetylene/polysiloxane interface.* Journal of Applied Physics, 1983. **54**(6): p. 3255-3259.

10. Tsumura, A., H. Koezuka, and T. Ando, *Macromolecular Electronic Device - Field-Effect Transistor with a Polythiophene Thin-Film.* Applied Physics Letters, 1986. **49**(18): p. 1210-1212.

11. Horowitz, G., et al., *A field-effect transistor based on conjugated alpha-sexithienyl.* Solid State Communications, 1989. **72**(4): p. 381-384.

12. Menard, E., et al., *High-Performance n- and p-Type Single-Crystal Organic Transistors with Free-Space Gate Dielectrics.* Advanced materials, 2004. **16**(23-24): p. 2097-2101.

13. Hasegawa, T. and J. Takeya, *Organic field-effect transistors using single crystals.* Science and Technology of Advanced Materials, 2009. **10**(2): p. 024314.

14. Minemawari, H., et al., *Inkjet printing of single-crystal films.* Nature, 2011. **475**(7356): p. 364-7.

15. Takahashi, Y., et al., *High Mobility Organic Field-Effect Transistor Based on Hexamethylenetetrathiafulvalene with Organic Metal Electrodes.* Chemistry of Materials, 2007. **19**(26): p. 6382-6384.

16. Chesterfield, R.J., et al., *Organic Thin Film Transistors Based on N-Alkyl Perylene Diimides: Charge Transport Kinetics as a Function of Gate Voltage and Temperature.* The Journal of Physical Chemistry B, 2004. **108**(50): p. 19281-19292.

17. Tatemichi, S., et al., *High mobility n-type thin-film transistors based on N,N'-ditridecyl perylene diimide with thermal treatments.* Applied Physics Letters, 2006. **89**(11): p. 112108.

18. Singh, S., et al., *Reduction of contact resistance by selective contact doping in fullerene n-channel organic field-effect transistors.* Applied Physics Letters, 2013. **102**(15): p. 153303.

19. Yan, H., et al., *A high-mobility electron-transporting polymer for printed transistors.* Nature, 2009. **457**(7230): p. 679-86.

20. Newman, C.R., et al., *Introduction to Organic Thin Film Transistors and Design of n-Channel Organic Semiconductors.* Chemistry of Materials, 2004. **16**(23): p. 4436-4451.

21. Tiwari, S.P., et al., *Study of electrical performance and stability of solution-processed n-channel organic field-effect transistors.* Journal of Applied Physics, 2009. **106**(5): p. 054504.

22. McDowell, M., et al., *Improved organic thin-film transistor performance using novel self-assembled monolayers.* Applied Physics Letters, 2006. **88**(7): p. 073505.

23. Kim, C.H., Y. Bonnassieux, and G. Horowitz, *Compact DC Modeling of Organic Field-Effect Transistors: Review and Perspectives.* IEEE Transactions on Electron Devices, 2014. **61**(2): p. 278-287.

24. Marinov, O., et al., *Organic Thin-Film Transistors: Part I—Compact DC Modeling.* IEEE Transactions on Electron Devices, 2009. **56**(12): p. 2952-2961.

25. Deen, M.J., et al., *Organic Thin-Film Transistors: Part II—Parameter Extraction.* IEEE Transactions on Electron Devices, 2009. **56**(12): p. 2962-2968.

26. Estrada, M., et al., *Accurate modeling and parameter extraction method for organic TFTs.* Solid-State Electronics, 2005. **49**(6): p. 1009-1016.

27. Chang Hyun, K., et al., *A Compact Model for Organic Field-Effect Transistors With Improved Output Asymptotic Behaviors.* IEEE Transactions on Electron Devices, 2013. **60**(3): p. 1136-1141.

28. Li, L., et al., *A compact model for polycrystalline pentacene thin-film transistor.* Journal of Applied Physics, 2010. **107**(2): p. 024519.

29. Shur, M. and M. Hack, *Physics of amorphous silicon based alloy field-effect transistors.* Journal of Applied Physics, 1984. **55**(10): p. 3831-3842.

30. Vissenberg, M.C.J.M. and M. Matters, *Theory of the field-effect mobility in amorphous organic transistors.* Physical Review B, 1998. **57**(20): p. 12964-12967.

31. Gaikwad, A.M., et al., *Identifying orthogonal solvents for solution processed organic transistors.* Organic Electronics, 2016. **30**: p. 18-29.

32. Kuribara, K., et al., *Organic transistors with high thermal stability for medical applications.* Nature communications, 2012. **3**: p. 723.

33. Yokota, T., et al., *Flexible low-voltage organic transistors with high thermal stability at 250 degrees C.* Advanced materials, 2013. **25**(27): p. 3639-44.

34. Hwang do, K., et al., *Top-gate organic field-effect transistors with high environmental and operational stability.* Advanced materials, 2011. **23**(10): p. 1293-8.

35. Hwang do, K., et al., *Systematic reliability study of top-gate p- and n-channel organic field-effect transistors.* ACS Appl Mater Interfaces, 2014. **6**(5): p. 3378-86.

36. Tobjork, D. and R. Osterbacka, *Paper Electronics.* Adv Mater, 2011. **23**(17): p. 1935-1961.

37. Moon, R.J., et al., *Cellulose nanomaterials review: structure, properties and nanocomposites.* Chemical Society Reviews, 2011. **40**(7): p. 3941-3994.

38. Zhou, Y., et al., *Recyclable organic solar cells on cellulose nanocrystal substrates.* Scientific reports, 2013. **3**: p. 1536.

39. Zhou, Y., et al., *Efficient recyclable organic solar cells on cellulose nanocrystal substrates with a conducting polymer top electrode deposited by film-transfer lamination.* Organic Electronics, 2014. **15**(3): p. 661-666.

40. Najafabadi, E., et al., *Efficient organic light-emitting diodes fabricated on cellulose nanocrystal substrates.* Applied Physics Letters, 2014. **105**(6): p. 063305.

41. Hong, X., *Introduction to Semiconductor Manufacturing Technology, Second Edition.* 2012.

42. http://www.jeol.co.jp/en/science/eb.html, 2016. **Accessed**.

43. http://www.cambridgenanotechald.com/atomic-layer-deposition/index.shtml, 2016. **Accessed**.

44. Fujisaki, Y., et al., *Transparent Nanopaper-Based Flexible Organic Thin-Film Transistor Array.* Advanced Functional Materials, 2014. **24**(12): p. 1657-1663.

45. Huang, J., et al., *Highly Transparent and Flexible Nanopaper Transistors.* Acs Nano, 2013. **7**(3): p. 2106-2113.

46. Zschieschang, U., et al., *Organic Electronics on Banknotes.* Advanced Materials, 2011. **23**(5): p. 654-658.

47. Peng, B. and P.K.L. Chan, *Flexible organic transistors on standard printing paper and memory properties induced by floated gate electrode.* Organic Electronics, 2014. **15**(1): p. 203-210.

48. Zocco, A.T., et al., *Pentacene organic thin-film transistors on flexible paper and glass substrates.* Nanotechnology, 2014. **25**(9): p. 094005.

49. Kim, T.S., et al., *Solution-processible polymer solar cells fabricated on a papery substrate.* Physica Status Solidi Rapid Res. Lett., 2012. **6**(1): p. 13-15.

50. Hübler, A., et al., *Printed paper photovoltaic cells.* Adv. Energy Mater., 2011. **1**(6): p. 1018-1022.

51. Wang, F., et al., *Papery solar cells based on dielectric/metal hybrid transparent cathode.* Solar Energy Materials and Solar Cells, 2010. **94**(7): p. 1270-1274.

52. Purandare, S., E.F. Gomez, and A.J. Steckl, *High brightness phosphorescent organic light emitting diodes on transparent and flexible cellulose films.* Nanotechnology, 2014. **25**(9): p. 094012.

53. Zhu, H., et al., *Biodegradable transparent substrates for flexible organic-light-emitting diodes.* Energy & Environmental Science, 2013. **6**(7): p. 2105-2111.

54. Ummartyotin, S., et al., *Development of transparent bacterial cellulose nanocomposite film as substrate for flexible organic light emitting diode (OLED) display.* Industrial Crops and Products, 2012. **35**(1): p. 92-97.

55. Yoon, D.-Y., T.-Y. Kim, and D.-G. Moon, *Flexible top emission organic light-emitting devices using sputter-deposited Ni films on copy paper substrates.* Current Applied Physics, 2010. **10**(4, Supplement): p. e135-e138.

56. Bollström, R., et al., *A multilayer coated fiber-based substrate suitable for printed functionality.* Organic Electronics, 2009. **10**(5): p. 1020-1023.

57. Andersson, P., et al., *Active Matrix Displays Based on All-Organic Electrochemical Smart Pixels Printed on Paper.* Adv Mater, 2002. **14**(20): p. 1460-1464.

58. Pereira, L., et al., *The influence of fibril composition and dimension on the performance of paper gated oxide transistors.* Nanotechnology, 2014. **25**(9): p. 094007.

59. Gaspar, D., et al., *Nanocrystalline cellulose applied simultaneously as the gate dielectric and the substrate in flexible field effect transistors.* Nanotechnology, 2014. **25**(9): p. 094008.

60. Petritz, A., et al., *Cellulose as biodegradable high-k dielectric layer in organic complementary inverters.* Applied Physics Letters, 2013. **103**(15): p. 153303.

61. Valentini, L., et al., *Cellulose nanocrystals thin films as gate dielectric for flexible organic field-effect transistors.* Materials Letters, 2014. **126**(0): p. 55-58.

62. Thiemann, S., et al., *Cellulose-Based Ionogels for Paper Electronics.* Advanced Functional Materials, 2014. **24**(5): p. 625-634.

63. Kawahara, J., et al., *Reconfigurable sticker label electronics manufactured from nanofibrillated cellulose-based self-adhesive organic electronic materials.* Organic Electronics, 2013. **14**(11): p. 3061-3069.

64. Choi, S., et al., *Organic field-effect transistor circuits using atomic layer deposited gate dielectrics patterned by reverse stamping.* Organic Electronics, 2014. **15**(12): p. 3780-3786.

65. Possanner, S.K., et al., *Threshold Voltage Shifts in Organic Thin-Film Transistors Due to Self-Assembled Monolayers at the Dielectric Surface.* Advanced Functional Materials, 2009. **19**(6): p. 958-967.

66. Hwang, D.K., et al., *Flexible and stable solution-processed organic field-effect transistors.* Organic Electronics, 2011. **12**(7): p. 1108-1113.

67. Peng, B., et al., *High performance organic transistor active-matrix driver developed on paper substrate.* Scientific Reports, 2014. **4**: p. 6430.

68. Fukuda, K., et al., *Fully Solution-Processed Flexible Organic Thin Film Transistor Arrays with High Mobility and Exceptional Uniformity.* Scientific Reports, 2014. **4**: p. 3947.

69. Fukuda, K., et al., *Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films.* Nature communications, 2014. **5**.

70. Lee, S., et al., *A transparent bending-insensitive pressure sensor.* Nat Nano, 2016. **advance online publication**.

71. Nawrocki, R.A., et al., *300-nm Imperceptible, Ultraflexible, and Biocompatible e-Skin Fit with Tactile Sensors and Organic Transistors.* Advanced Electronic Materials, 2016. **2**(4): p. n/a-n/a.

72. Sirringhaus, H., *25th anniversary article: organic field-effect transistors: the path beyond amorphous silicon.* Advanced materials, 2014. **26**(9): p. 1319-35.

73. Knopfmacher, O., et al., *Highly stable organic polymer field-effect transistor sensor for selective detection in the marine environment.* Nature communications, 2014. **5**.

74. Hwang, D.K., et al., *Systematic Reliability Study of Top-Gate p-and n-channel Organic Field-Effect Transistors.* ACS applied materials & interfaces, 2014.

75. Hwang do, K., et al., *Stable solution-processed molecular n-channel organic field-effect transistors.* Advanced materials, 2012. **24**(32): p. 4445-50.

76. Yun, M., et al., *Stable Organic Field-effect Transistors for Continuous and Non-destructive Sensing of Chemical and Biologically Relevant Molecules in Aqueous Environment.* ACS applied materials & interfaces, 2014. **6**(3): p. 1616-1622.

77. Kim, L.H., et al., *Al_2O_3/TiO_2 Nanolaminate Thin Film Encapsulation for Organic Thin Film Transistors via Plasma-Enhanced Atomic Layer Deposition.* ACS Applied Materials & Interfaces, 2014. **6**(9): p. 6731-6738.

78. Meyer, J., et al., *Reliable thin film encapsulation for organic light emitting diodes grown by low-temperature atomic layer deposition.* Applied Physics Letters, 2009. **94**(23): p. 233305.

79. Seo, S.-W., et al., *Optimization of Al_2O_3/ZrO_2 nanolaminate structure for thin-film encapsulation of OLEDs.* Organic Electronics, 2012. **13**(11): p. 2436-2441.

80. Abdulagatov, A.I., et al., *Al_2O_3 and TiO_2 Atomic Layer Deposition on Copper for Water Corrosion Resistance.* ACS Applied Materials & Interfaces, 2011. **3**(12): p. 4593-4601.

81. Meyer, J., et al., *The origin of low water vapor transmission rates through Al_2O_3/ZrO_2 nanolaminate gas-diffusion barriers grown by atomic layer deposition.* Applied Physics Letters, 2010. **96**(24): p. 243308.

82. Baek, Y., et al., *Al_2O_3/TiO_2 nanolaminate gate dielectric films with enhanced electrical performances for organic field-effect transistors.* Organic Electronics, 2016. **28**: p. 139-146.

83. Shim, J.W., et al., *Inverted Tandem Polymer Solar Cells with Polyethylenimine-Modified MoO_x/Al_2O_3:ZnO Nanolaminate as the Charge Recombination Layers.* Advanced Energy Materials, 2014. **4**(10): p. n/a-n/a.

84. Bulusu, A., et al., *Engineering the mechanical properties of ultrabarrier films grown by atomic layer deposition for the encapsulation of printed electronics.* Journal of Applied Physics, 2015. **118**(8): p. 085501.

85. Oh, J.H., P. Wei, and Z. Bao, *Molecular n-type doping for air-stable electron transport in vacuum-processed n-channel organic transistors.* Applied Physics Letters, 2010. **97**(24): p. 243305.

86. Guo, S., et al., *n-Doping of Organic Electronic Materials Using Air-Stable Organometallics: A Mechanistic Study of Reduction by Dimeric Sandwich Compounds.* Chemistry – A European Journal, 2012. **18**(46): p. 14760-14772.

87. Fujimori, F., et al., *Current transport in short channel top-contact pentacene field-effect transistors investigated with the selective molecular doping technique.* Applied Physics Letters, 2007. **90**(19): p. 193507.

88. Minari, T., et al., *Highly enhanced charge injection in thienoacene-based organic field-effect transistors with chemically doped contact.* Applied Physics Letters, 2012. **100**(9): p. 093303.

89. Darmawan, P., et al., *Optimal Structure for High-Performance and Low-Contact-Resistance Organic Field-Effect Transistors Using Contact-Doped Coplanar and Pseudo-Staggered Device Architectures.* Advanced Functional Materials, 2012. **22**(21): p. 4577-4583.

90. Abe, Y., et al., *Control of threshold voltage in pentacene thin-film transistors using carrier doping at the charge-transfer interface with organic acceptors.* Applied Physics Letters, 2005. **87**(15): p. 153506.

91. Minari, T., et al., *Charge injection process in organic field-effect transistors.* Applied Physics Letters, 2007. **91**(5): p. 053508.

92. Vanoni, C., S. Tsujino, and T.A. Jung, *Reduction of the contact resistance by doping in pentacene few monolayers thin film transistors and self-assembled nanocrystals.* Applied Physics Letters, 2007. **90**(19): p. 193119.

93. Vanoni, C., T.A. Jung, and S. Tsujino, *Temperature dependent charge-injection at the metal-organic semiconductor interface and density of states in pristine and doped pentacene.* Applied Physics Letters, 2009. **94**(25): p. 253306.

94. Yamagishi, Y., et al., *Organic field-effect transistors with molecularly doped polymer gate buffer layer.* Synthetic Metals, 2012. **162**(21–22): p. 1887-1893.

95. Nicht, S., et al., *Functionalized p-dopants as self-assembled monolayers for enhanced charge carrier injection in organic electronic devices.* Organic Electronics, 2014. **15**(3): p. 654-660.

96. Menke, T., et al., *Highly efficient p-dopants in amorphous hosts.* Organic Electronics, 2014. **15**(2): p. 365-371.

97. Kröger, M., et al., *P-type doping of organic wide band gap materials by transition metal oxides: A case-study on Molybdenum trioxide.* Organic Electronics, 2009. **10**(5): p. 932-938.

98. Gwinner, M.C., et al., *Doping of Organic Semiconductors Using Molybdenum Trioxide: a Quantitative Time-Dependent Electrical and Spectroscopic Study.* Advanced Functional Materials, 2011. **21**(8): p. 1432-1441.

99. Lee, T.H., et al., *p-Channel Field-Effect Transistors Based on C60 Doped with Molybdenum Trioxide.* ACS Applied Materials & Interfaces, 2013. **5**(7): p. 2337-2341.

100. Qi, Y., et al., *Use of a High Electron-Affinity Molybdenum Dithiolene Complex to p-Dope Hole-Transport Layers.* Journal of the American Chemical Society, 2009. **131**(35): p. 12530-12531.

101. Qi, Y., et al., *A Molybdenum Dithiolene Complex as p-Dopant for Hole-Transport Materials: A Multitechnique Experimental and Theoretical Investigation.* Chemistry of Materials, 2010. **22**(2): p. 524-531.

102. Tiwari, S.P., et al., *Pentacene organic field-effect transistors with doped electrode-semiconductor contacts.* Organic Electronics, 2010. **11**(5): p. 860-863.

103. Yan, H., et al., *A high-mobility electron-transporting polymer for printed transistors.* Nature, 2009. **457**(7230): p. 679-686.

104. Cheng, X., et al., *Air Stable Cross-Linked Cytop Ultrathin Gate Dielectric for High Yield Low-Voltage Top-Gate Organic Field-Effect Transistors.* Chemistry of Materials, 2010. **22**(4): p. 1559-1566.

105. Yun, M., et al., *Stable Organic Field-Effect Transistors for Continuous and Nondestructive Sensing of Chemical and Biologically Relevant Molecules in Aqueous Environment.* ACS Applied Materials & Interfaces, 2014. **6**(3): p. 1616-1622.

106. Zhou, Y., et al., *A Universal Method to Produce Low–Work Function Electrodes for Organic Electronics.* Science, 2012. **336**(6079): p. 327-332.

107. Klauk, H., et al., *Contact resistance in organic thin film transistors.* Solid-State Electronics, 2003. **47**(2): p. 297-301.

108. Meijer, E.J., et al., *Scaling behavior and parasitic series resistance in disordered organic field-effect transistors.* Applied Physics Letters, 2003. **82**(25): p. 4576-4578.

109. Davis, R.J., et al., *Determination of energy level alignment at interfaces of hybrid and organic solar cells under ambient environment.* Journal of Materials Chemistry, 2011. **21**(6): p. 1721-1729.

110. Logan, S., et al., *Compatibility of amorphous triarylamine copolymers with solution-processed hole injecting metal oxide bottom contacts.* Journal of Materials Chemistry C, 2015. **3**(17): p. 4530-4536.

111. Choi, S., et al., *A Study on Reducing Contact Resistance in Solution-Processed Organic Field-Effect Transistors.* ACS applied materials & interfaces, 2016.

112. Martins, R., et al., *Complementary Metal Oxide Semiconductor Technology With and On Paper.* Adv. Mater., 2011. **23**(39): p. 4491-4496.

113. Pettersson, F., et al., *Environmentally Friendly Transistors and Circuits on Paper.* ChemPhysChem, 2015. **16**(6): p. 1286-1294.

114. Pettersson, F., D. Adekanye, and R. Österbacka, *Stability of environmentally friendly paper electronic devices.* physica status solidi (a), 2015. **212**(12): p. 2696-2701.

115. Grau, G., et al., *Printed Transistors on Paper: Towards Smart Consumer Product Packaging.* Advanced Functional Materials, 2014. **24**(32): p. 5067-5074.

116. Li, Y., et al., *Solution-processed organic crystals for field-effect transistor arrays with smooth semiconductor/dielectric interface on paper substrates.* Organic Electronics, 2012. **13**(5): p. 815-819.

117. Minari, T., et al., *Room-Temperature Printing of Organic Thin-Film Transistors with π-Junction Gold Nanoparticles.* Advanced Functional Materials, 2014. **24**(31): p. 4886-4892.

118. Peng, B., et al., *High performance organic transistor active-matrix driver developed on paper substrate.* Scientific reports, 2014. **4**: p. 6430.

119. Wang, C.Y., et al., *Stable low-voltage operation top-gate organic field-effect transistors on cellulose nanocrystal substrates.* ACS applied materials & interfaces, 2015. **7**(8): p. 4804-8.

120. Zschieschang, U. and H. Klauk, *Low-voltage organic transistors with steep subthreshold slope fabricated on commercially available paper.* Organic Electronics, 2015. **25**: p. 340-344.

121. Eder, F., et al., *Organic electronics on paper.* Applied Physics Letters, 2004. **84**(14): p. 2673-2675.

122. Kim, Y.H., et al., *Organic thin-film devices on paper substrates.* Journal of the Society for Information Display, 2005. **13**(10): p. 829-833.

123. Yun, M., et al., *Stable organic field-effect transistors for continuous and nondestructive sensing of chemical and biologically relevant molecules in aqueous environment.* ACS applied materials & interfaces, 2014. **6**(3): p. 1616-22.

124. Wang, C.-Y.F.-H., Canek; Yun, Minseong; Singh, Ankit; Dindar, Amir; Choi, Sangmoo; Graham, Samuel; Kippelen, Bernard, *Organic field-effect transistors with a bilayer gate dielectric comprising an oxide nanolaminate grown by atomic layer deposition.* (submitted).

125. Ping, Z., Q.T. Nguyen, and J. Néel, *Investigation of poly(vinyl alcohol)/poly(N-vinyl-2-pyrrolidone) blends, 3. Permeation properties of polymer blend membranes.* Macromolecular Chemistry and Physics, 1994. **195**(6): p. 2107-2116.

126. Jones, S.A., et al., *Biocompatible polymer blends: Effects of physical processing on the molecular interaction of poly(vinyl alcohol) and poly(vinyl pyrrolidone).* Journal of Applied Polymer Science, 2005. **98**(5): p. 2290-2299.

127. Azadmanjiri, J., et al., *A review on hybrid nanolaminate materials synthesized by deposition techniques for energy storage applications.* Journal of Materials Chemistry A, 2014. **2**(11): p. 3695-3708.

128. Kim, H., et al., *Experimental investigation of defect-assisted and intrinsic water vapor permeation through ultrabarrier films.* Review of Scientific Instruments, 2016. **87**(3): p. 033902.