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Origin of the low-frequency noise in n-channel FinFETs

C.G. Theodorou [a,c,*], N. Fasarakis [a], T. Hoffman [b], T. Chiarella [b], G. Ghibaudo [c], C.A. Dimitriadis [a]

[a] Aristotle University of Thessaloniki, Department of Physics, 54124 Thessaloniki, Greece
[b] IMEC, Kapeldreef 75, 3001 Heverlee, Belgium
[c] IMEP-LAHC Laboratory, MINATEC, Louis Néel, 38054 Grenoble Cedex 9, France

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ABSTRACT

The origin of the low-frequency noise is investigated in n-channel fin-shaped field-effect transistors (FinFETs) in terms of the channel length and fin width. In long-channel and wide fin devices, the spectra are dominated by 1/*f* noise due to carrier number fluctuation, correlated with mobility fluctuations. In long-channel and narrow fin devices, the spectra are composed of both 1/*f* and excess generation–recombination (*g*–*r*) noise components. Analysis of the *g*–*r* noise parameters lead to the conclusion that the *g*–*r* noise originates from traps in the sidewall gate oxides and in a depletion region near the sidewall interfaces. In short-channel devices, the spectra show 1/*f* behavior in the weak inversion described by carrier number fluctuations and *g*–*r* noise component in the low drain current region, possibly originating from the source and drain contacts process.

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1. Introduction

Tri-gate (TG) fin-shaped field-effect transistors (FinFETs) are promising device structures for sub-100-nm scaling of MOSFETs due to their immunity to short-channel effects (SCEs) [1–3]. However, as the FinFETs scale down, the low-frequency (LF) noise becomes more pronounced due to its inverse dependence with the gate area, and it could lead to serious limitations of the analog and digital circuits functionality [4,5]. In addition, the LF noise is a non-destructive and sensitive diagnostic tool to characterize the traps present at the gate oxide/silicon interface and in the depletion layer of silicon [7–14]. Therefore, it is important to clarify the origin of the LF noise in nanoscale TG FinFETs, in order to optimize their noise level.

In most cases of n-channel TG FinFETs, the origin of the LF noise has been investigated in long-channel devices [6–13], and recently, the investigation was extended to gate lengths down to 60 nm [12,13]. In several cases, it was found that the noise spectra contain two noise sources: 1/*f* noise ascribed to carrier number fluctuations (CNFs) due to carrier exchange between the gate dielectric traps near the interface and the channel and generation–recombination (*g*–*r*) noise components due to charge traps in the gate oxide or in the silicon depletion region. Analysis of the *g*–*r* noise components at different temperatures enabled the extraction of the trap characteristic parameters (energy level, capture cross-section) [12,13]. In the weak inversion region of n-channel FinFETs, in some cases, the mobility fluctuation was found to be the dominant 1/*f* noise generation mechanism [14]. Recently, the LF noise in the linear region from weak to strong inversion has been investigated in *p*-channel FinFETs, with channel length ranging from 70 nm to 1 μm [15]. It has been shown that in *p*-channel FinFETs, the LF noise is composed of both 1/*f* noise governed by CNF and *g*–*r* noise originating from traps in the gate oxide [15].

In this work, we investigate systematically the impact of the fin width on the LF noise of n-channel TG FinFETs with long-channel length (L = 1 μm) and short-channel length (L = 25 nm). It is shown that the LF noise spectra are composed both of 1/*f* noise and *g*–*r* noise components. The origin of the 1/*f* and *g*–*r* noise components is clarified in the long-channel and short-channel devices in terms of the fin width.

2. Experimental

The n-channel FinFETs were fabricated at IMEC (Leuven, Belgium) on silicon on insulator (SOI) wafers with 145 nm buried oxide thickness. The device parameters are channel doping concentration 10^{15} cm^{-3}, TiN/HfO_2 gate insulator stack with equivalent gate oxide thickness t_{ox} = 1.7 nm, constant fin height H_{fin} = 65 nm, fin width W_{fin} varying from 5 nm to 1 μm, and channel length L = 25 nm and 1 μm. The investigated devices have five fins, and the effective device width is $5 \times (2H_{fin} + W_{fin})$. Details for the device fabrication processes are presented elsewhere [16].

* Corresponding author at: IMEP-LAHC Laboratory, MINATEC, Louis Néel, 38054 Grenoble Cedex 9, France. Tel.: +33 616116148.
E-mail address: cgtheodo@auth.gr (C.G. Theodorou).

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Low-frequency noise measurements were performed at room temperature in the linear regime (drain voltage V_d = 30 mV), with the gate bias varying from weak to strong inversion, using a fully automatic LFN measuring system by synergy concept [17]. During measurements, the substrate contact was grounded.

3. Results and discussion

Drain current noise spectra of n-channel FinFETs with constant channel length L = 1 μm and fin widths W_{fin} = 1000, 65, 15, and 5 nm were measured in the frequency range of 5–10^4 Hz at different drain currents. In general, the noise spectra contain 1/*f* and *g–r* noise components, with the noise spectral density S_I following the equation:

$$S_I = \frac{K_f}{f} + \sum_{i=0}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{oi}}\right)^2}, \quad (1)$$

where K_f is a coefficient characterizing the intensity of the 1/*f* noise and the second term represents a sum of *g–r* components with A_i the plateau value and f_{oi} the characteristic frequency of the *g–r* noise components associated with the time constant of the traps $\tau_i = 1/2\pi f_{oi}$. The later is characterized by a plateau value at low frequencies and a fall-off according to $1/f^2$ at higher frequencies. It is noticed that the white noise observed at high frequencies is two orders of magnitude lower than the measured power spectral density and has been neglected in Eq. (1). The 1/*f* and *g–r* noise components can be revealed more clearly by representing the product $S_I \times f$ versus frequency *f* in Fig. 1. For the wide fin device (W_{fin} = 1000 nm), it is seen that $S_I \times f$ increases with *f*, *that is,* the noise follows a $1/f^{\gamma}$ (with $\gamma < 1$) behavior indicating that the top gate oxide trap density decreases with distance from the Si–SiO_2 interface [9]. In the TG device (W_{fin} = 65 nm), one can notice a slight distortion of the 1/*f* noise due to the presence of weak *g–r* noise component, whereas in the narrow fin devices (W_{fin} = 15 and 5 nm), the presence of the *g–r* noise is more evident.

The normalized drain current noise spectral density S_I/I_d^2 at frequency *f* = 10 Hz, extracted from the noise spectra of the FinFETs of Fig. 1, is presented in Fig. 2. The normalized flicker noise components at frequency 10 Hz, extracted from analysis of the noise spectra, are also presented in Fig. 2. In most cases, the data tend to saturate to a plateau in weak inversion and exhibit a decreasing trend with increasing the drain current I_d in strong inversion. In the case of the wide fin FinFET with W_{fin} = 1000 nm, a good correlation between normalized drain current noise and transconductance $(g_m/I_d)^2$ is shown. These results satisfy the model of carrier number fluctuations and additional correlated mobility fluctuations, *that is,* the so-called correlated mobility fluctuations (CMF) [18,19]. In this noise model, the interaction between traps in the gate oxide near the interface and channel carriers is the main source of noise. In several cases, peaks and humps occur in the plots of S_I/I_d^2 versus I_d, which can be ascribed to excess *g–r* contributions in the spectra. In Fig. 2b, weak peaks are observed indicating the dominance of the 1/*f* noise over the *g–r* noise components. However, in the narrow fin devices of Fig. 2c and d, the occurrence of strong peaks and humps is a clear evidence of the *g–r* noise components dominance over the 1/*f* noise. Specifically, in the case of the very narrow fin device (W_{fin} = 5 nm), the *g–r* noise dominates over the whole drain current range.

The *g–r* component of the noise spectra can originate from a trap located in the gate dielectric, at the interface between gate dielectric/silicon or in the depletion region [20,21]. To identify the origin of the *g–r* noise observed in Fig. 2c and d, the normalized plateau amplitude A_i/I_d^2 and the trap time constant τ of the obtained *g–r* components are presented in Fig. 3a and b, respectively. These results show clearly the presence of two trap levels in FinFETs with W_{fin} = 15 and 5 nm. The values of τ and A_i/I_d^2 depend on the gate voltage and some of the curves $\tau(V_g)$ and $A_i/I_d^2\,(V_g)$ pass through a maximum in the region near the threshold. Such behavior is typical for *g–r* noise due to thin layers of single energy trap levels in the depletion region near the Si/SiO_2 interface [20,21]. It is noted that similar behavior of $\tau(V_g)$ is also typical for *g–r* noise

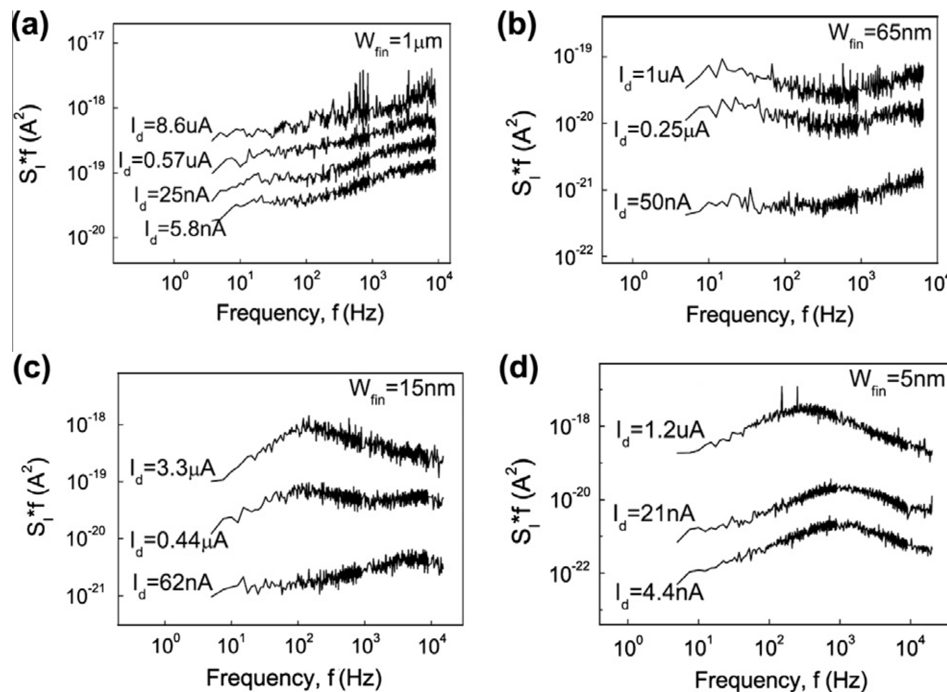

Fig. 1. Frequency dependence of the drain current noise spectral density multiplied by frequency, measured at drain voltage V_d = 30 mV at different drain currents, in n-channel FinFETs with channel length L = 1 μm and fin widths W_{fin} = 1 μm (a), 65 nm (b), 15 nm (c), and 5 nm (d).

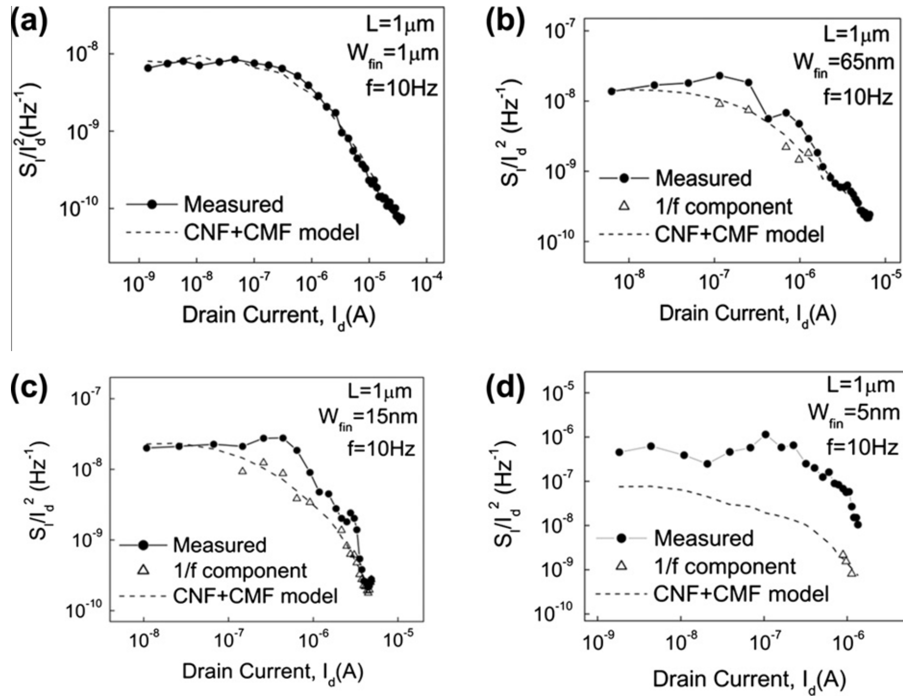

Fig. 2. Normalized measured drain current power spectral density S_I/I_d^2 (circles) and flicker noise components (triangles) versus drain current I_d, extracted from the experimental data of Fig. 1. The dotted lines correspond to the CNF + CMF model, derived using the $(g_m/I_d)^2$ parameter, along with the noise parameters values: $S_{vfb} = 4.5 \times 10^{-12}\ V^2/Hz$ and $a_{sc}\cdot\mu_{eff} = 1.25 \times 10^6\ cm^2/C$ (a), $S_{vfb} = 1 \times 10^{-11}\ V^2/Hz$ and $a_{sc}\cdot\mu_{eff} = 1{,}5 \times 10^6\ cm^2/C$ (b), $S_{vfb} = 2 \times 10^{-11}\ V^2/Hz$ and $a_{sc}\cdot\mu_{eff} = 1 \times 10^6\ cm^2/C$ (c), $S_{vfb} = 7 \times 10^{-11}\ V^2/Hz$ and $a_{sc}\cdot\mu_{eff} = 9 \times 10^5\ cm^2/C$ (d), where S_{vfb} is the flat-band voltage spectral density, α_{sc} is the Coulomb scattering coefficient and μ_{eff} is the effective carrier mobility.

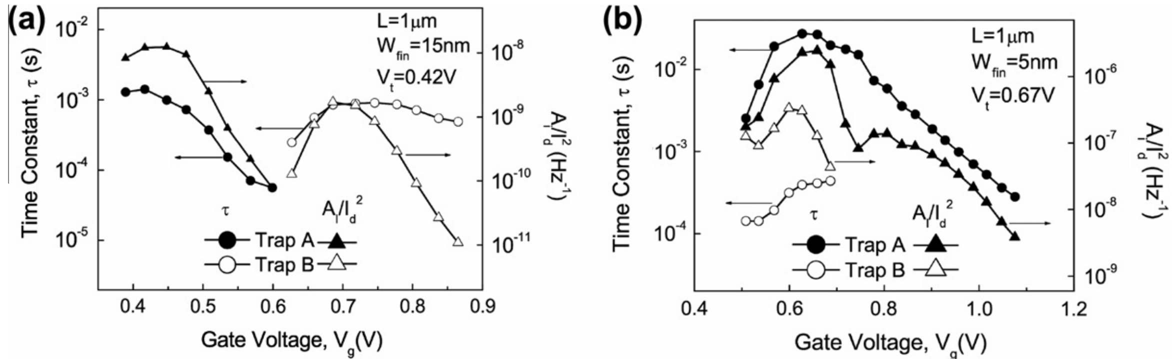

Fig. 3. Dependence of the normalized plateau and time constant on gate voltage for the *g–r* noise components in n-channel FinFETs with channel length $L = 1\ \mu m$ and fin widths $W_{fin} = 15$ nm (a) and 5 nm (b).

due to interface traps in the sub-threshold mode of operation [20]. The dominance of the *g–r* noise with decreasing the fin width clearly indicates that the layers of traps are located near the sidewall gates, originating either from process steps used to define the sidewall fins by reactive ion etching, or due to the different sidewall crystalline orientation from the one of the top gate, thus leading to different energy states in the bandgap. In Fig. 3a and b, it is also seen that a *g–r* noise appears at strong inversion, in which both the time constant τ and the normalized plateau amplitude are gate voltage dependent exhibiting a peak at $V_g > V_t$. This type of *g–r* noise, most likely corresponds to a trap in the sidewall gate dielectric, with a well-defined activation energy and/or position in the oxide. This finding implies that these traps are created by processing steps specific for the gate oxide.

In Fig. 4a, the normalized drain current noise spectral density S_I/I_d^2 at frequency $f = 20$ Hz, extracted from the noise spectra of a short-channel FinFET with channel length $L = 25$ nm and fin width $W_{fin} = 20$ nm is presented, showing a dominance of the *g–r* noise component in the sub-threshold and weak inversion regions. Fig. 4b shows that the *g–r* time constant τ is independent on the gate voltage, which suggests that the *g–r* noise originates from defects in the silicon layer [20,21]. Similar behavior for the normalized drain current noise spectral density S_I/I_d^2 and the time constant τ were observed also for the short-channel FinFET with $W_{fin} = 5$ nm (not presented).

The overall results clearly show the impact of the fin width and length on the traps observed in the silicon film. In short-channel FinFETs, the prevailing traps may originate from process steps used for realization of the source and drain contacts. In long-channel FinFETs, the traps may be related to the process steps used for defining the sidewalls of the fin and the gate oxide growth. The characteristic trap parameters of the *g–r* noise (energy level, capture cross-section) can be determined from noise measurements at different temperatures [12,13]. Moreover, in order to further

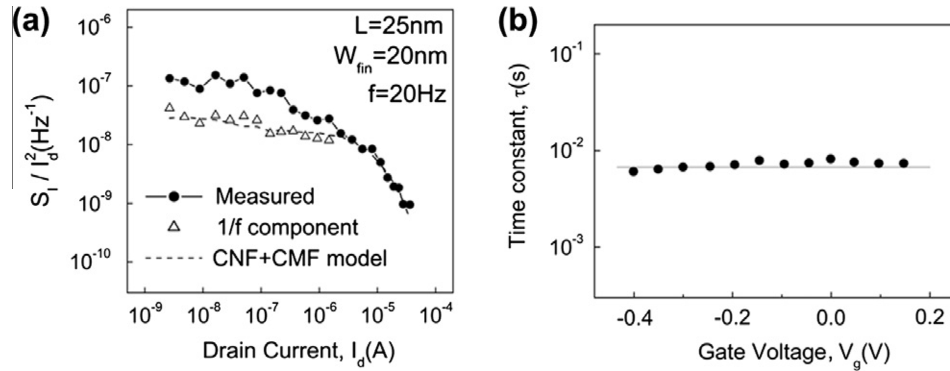

Fig. 4. (a) Normalized measured drain current power spectral density S_I/I_d^2 (circles) and flicker noise components (triangles) versus drain current I_d, in n-channel FinFET with channel length L = 25 nm and fin width W_{fin} = 20 nm. The dotted line corresponds to the CNF + CMF model, derived using the $(g_m/I_d)^2$ parameter, along with the noise parameter values $S_{vfb} = 1 \times 10^{-10}$ V^2/Hz and $a_{sc} \cdot \mu_{eff} = 2.5 \times 10^5$ cm^2/C, where S_{vfb} is the flat-band voltage spectral density, α_{sc} is the Coulomb scattering coefficient and μ_{eff} is the effective carrier mobility. (b) Dependence of the time constant τ on gate voltage for the g–r noise component.

clarify the origin of the 1/f noise in small area devices (<1 μm^2), low-frequency noise measurements in the time domain are required to detect possible random telegraph signals (RTS) which are generally caused by electron exchange between oxide trap and the channel [22,23].

4. Conclusion

The impact of the fin width on the low-frequency noise has been investigated in long-channel (L = 1 μm) and short-channel (L = 25 nm) n-channel FinFETs. In the long-channel devices with wide fins, the noise shows 1/f behavior which is compatible with carrier number fluctuations and additional correlated mobility fluctuations. In long-channel devices with narrow fins, the spectra are composed of both 1/f and excess g–r noise on top of the 1/f noise. From analysis of the gate voltage dependence of the g–r parameters, it has been concluded that the g–r noise originates from traps in the sidewall gate oxides and in a depletion region near the sidewall interfaces. In the short-channel devices, the noise spectra show 1/f type behavior in the strong inversion region, whereas g–r noise appears in the sub-threshold and weak inversion region originating from traps due to process steps for the source and drain contacts formation.

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