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Origin of the relatively low transport mobility of graphene grown through chemical vapor deposition

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The reasons for the relatively low transport mobility of graphene grown through chemical vapor deposition (CVD-G), which include point defect, surface contamination, and line defect, were analyzed in the current study. A series of control experiments demonstrated that the determinant factor for the low transport mobility of CVD-G did not arise from point defects or surface contaminations, but stemmed from line defects induced by grain boundaries. Electron microscopies characterized the presence of grain boundaries and indicated the polycrystalline nature of the CVD-G. Field-effect transistors based on CVD-G without the grain boundary obtained a transport mobility comparative to that of Kish graphene, which directly indicated the detrimental effect of grain boundaries. The effect of grain boundary on transport mobility was qualitatively explained using a potential barrier model. Furthermore, the conduction mechanism of CVD-G was also investigated using the temperature dependence measurements. This study can help understand the intrinsic transport features of CVD-G.

Graphene, a distinct two-dimensional (2D) building block, has attracted much attention due to its excellent transport properties that make it a promising material for next-generation nanoelectronics[1–4]. The strong interest in graphene has motivated various kinds of preparation methods, such as mechanical exfoliation from bulk graphite[1], graphitization of silicon carbide substrate[5,6], and chemical vapor deposition (CVD) on transition metals[7–9]. Among these methods, CVD method grown on polycrystalline copper foils exhibits its superiority from the relatively simple and low-cost growth, large size, predominant monolayer graphene growth, and ease of transfer to other substrates[10]. However, the charge carrier mobility of graphene grown through CVD (CVD-G) is typically orders of magnitude lower[9] than the theoretical values[11] or data reported for exfoliated graphene[12,13]. Clarifying the source of inferior carrier transport performance is highly desired for the realistic and industrial applications of CVD-G. Theoretical calculations in which graphene presents electronic excitations as two dimensional Dirac fermions predict the reasons may be led by impurities, edges and grain boundaries[14–19]. Combined with the experimental process from CVD-G growth to device fabrication, the main possible reasons for the inferior performance are suggested as point defect, surface contamination, and line defects. Although lateral experimental work[36] also found the detrimental effect from above individual factor, the report systematically discussing the effect of above three factors is still absent especially unclear for the determined role among them. Considering further that the CVD-G growth does not grow slowly atom-by-atom from one nucleus, but rather through relaxation of a metal-carbon system with many nuclei[20], the presence of defects in the as-grown CVD-G samples should be expected. Generally, point defect was introduced from damage effect, such as reconstruction to form nonhexagonal rings, particle irradiation to miss the lattice atom, carbon, or foreign adatom, and so on[21–24]; surface contamination was induced inevitably from the substrate transfer and device fabrication process[12,13,25]; meanwhile, line defect was mainly introduced by the grain boundary through the polycrystalline graphene materials[26–28]. Structural defects and surface contamination may act as internal or external scattering centers for electron waves, and greatly degrade transport properties[25–28]. Comparing to the vast amount of the available theoretical analysis, the experimental analysis to the transport of CVD-G has just begun, and especially for the lack of reproducible experimental results[20].

To clarify the roles of the above three factors on CVD-G, various comparative experiments have been designed and carried out. Single crystalline graphene samples exfoliated from Kish graphite (Kish-G) was utilized as reference for the effect of point defect. Various contents of point defect were introduced into Kish-G samples

through oxygen plasma bombardment. Thermal annealing treatment was adopted to remove surface contamination and to investigate its effect. Scanning electron microscopy (SEM), Transmission electron microscopy (TEM), and electrical transport measurements (room temperature and variable temperature dependence) were utilized to determine the presence and roles of grain boundaries. Results from the present investigation will be helpful to understand the origin of the transport properties of CVD-G.

Results

The structural and electrical properties of CVD-G samples have been investigated as shown in Fig. 1. Raman spectroscopy, a powerful tool to identify the presence of defects and graphene layers, was utilized to analyze the characteristics of Raman peaks. Three dimensional (3D) Raman maps of D, G, and 2D peaks from one typical CVD-G ribbon sample were extracted and plotted, as shown in Figs. 1a to 1c, respectively. The D peak, located at approximately 1350 cm^{-1}, is caused by the breathing mode of sp^2 atoms and activated by the existence of some defects such as edges, functional groups, or structural disorders[30]. The contrast of the D peak intensity in Fig. 1a clearly shows the defect spatial distribution. A pronounced D band signal was found on the edge of the sample which was introduced through patterning, while the continuous ridge, except for the edge, was resulted from the grain boundary. Thus, Raman mapping of the D peak intensity can provide a convenient way to identify the locations of the grain boundary. The maps of G and 2D are relatively uniform with high counts (approximately tens of thousands) except for few vertexes. The corresponding Raman spectra (Fig. 1d) were also extracted from six typical spots far from the edge. The intensity of the 2D peak is twice more than the intensity of the G peak. Furthermore, the shape of the 2D peak can be perfectly fitted by one Lorenz peak. Both of the above two Raman features assure the monolayer nature of the CVD-G samples[30]. The ratio of the intensity of the D peak to the intensity of the G peak (I_D/I_G) is conveniently utilized as the footprint for the estimation of the amount of defect in graphene. The corresponding I_D/I_G ratio as shown in Fig. 1d contains a small ratio varying from 0.02 to 0.15. The field effect mobility for CVD-G samples has been obtained from the back-gate FETs, which are mainly located at 800 $cm^2/(Vs)$ to 1700 $cm^2/(Vs)$, occupying 11 of the 16 measured devices. The mean mobility is approximately 1100 $cm^2/(Vs)$. The small I_D/I_G ratio and intermediate mobility demonstrated that our CVD-G was similar to previous results[8–10] on CVD-G and could be utilized in control experiments, although its mobility was lower than that of the Kish-G (approximately 5000 $cm^2/(Vs)$), as shown below.

The presence of the defect has been captured in Raman map (Fig. 1a) which made it reasonable to correlate the defect to the lower transport mobility. Kish-G samples without the Raman defect signal were chosen as references to understand the effect of point defect. Figure 2a shows the optical image of a typical sample, Sample A of Kish-G (denoted as Kish-G@A). The point defect from particle irradiation has been introduced into Kish-G through oxygen plasma bombardment, and the content was controlled by increasing the exposure time. As shown in Fig. 2b, the I_D/I_G ratio increases as the exposure time extended from 6 s to 30 s. The increase of the I_D/I_G ratio indicates an evolution process from intact graphene lattice to a more disordered carbon phase. Figure 2c shows the corresponding electrical property evolution for plasma damage. The FET performance reveals a decrease in mobility and conductivity, as well as a positive shift in charge neutral point (CNP) voltage, indicating that *p*-dopants are attached to the defect sites[31]. Additional three devices (Sample Kish-G@B, C, and D) also displayed similar evolution trend through damage effect. The evolution curves of I_D/I_G ratio *versus* field effect mobility have been plotted based on Raman and electrical

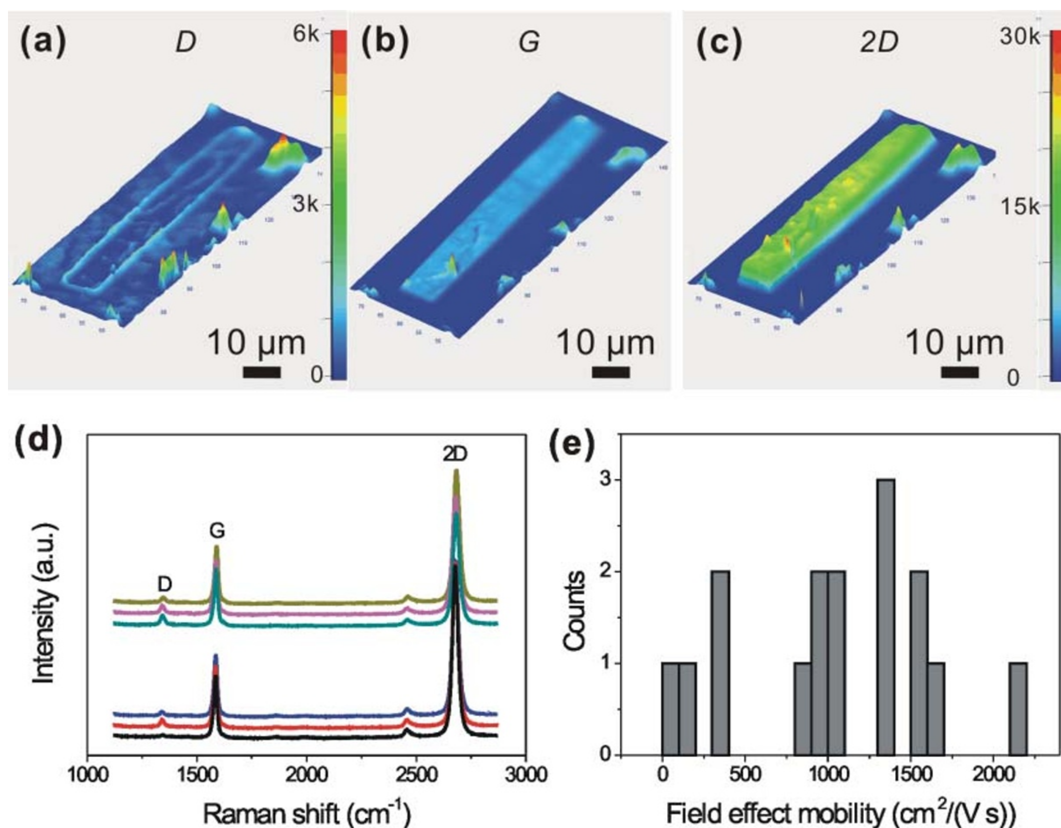

Figure 1 | Basic investigation of the CVD-G samples: (a–c) Intensity maps of the D, G, and 2D bands, respectively. Figure 1b and c share the same count scale. (d) Raman spectra of the same sample as Fig. 1a to c were collected from six typical spots far from the edge. (e) Statistic field effect mobility distribution for CVD-G devices.

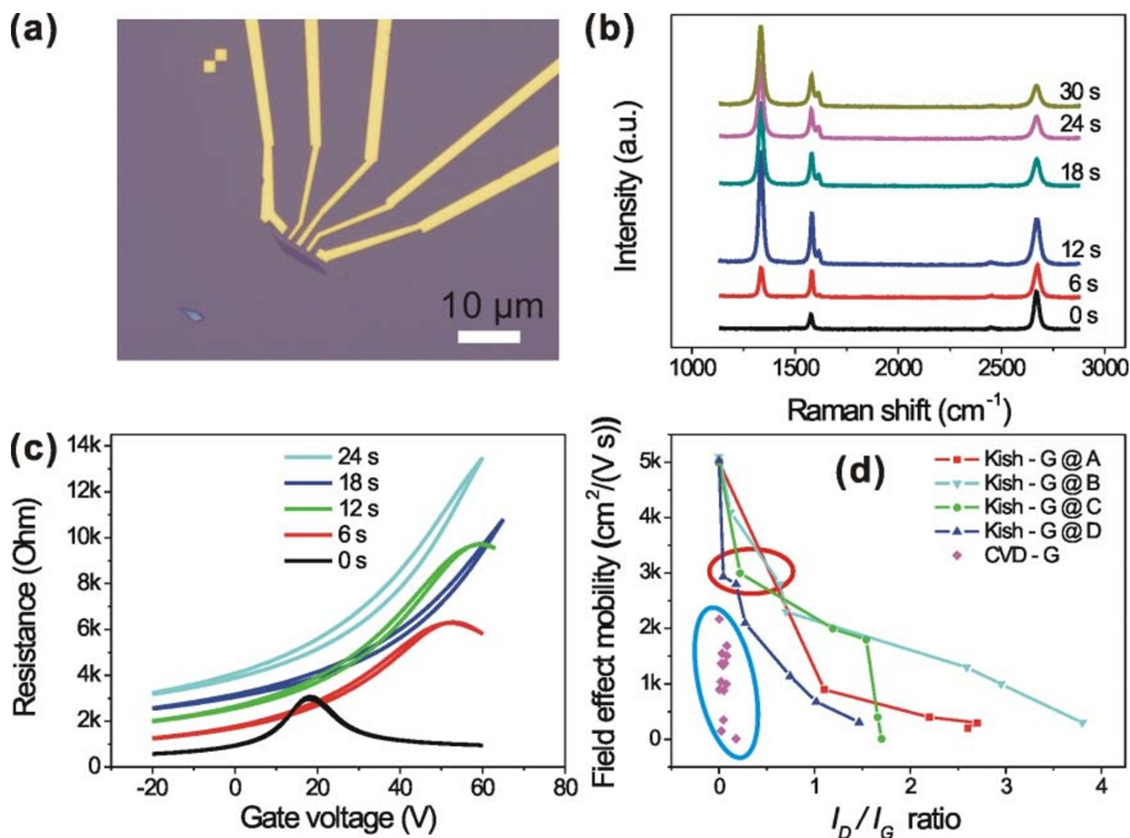

Figure 2 | Damaged Kish-G samples as the references for CVD-G. (a) Optical image for one typical Kish-G sample (Kish-G@A) with 1.6 μm channel length and 1.5 μm width; (b, c) Raman spectra and transfer character evolution as Kish-G@A is exposed to oxygen plasma with different duration time. (d) Mobility μ versus I_D/I_G ratio for CVD-G and Kish-G samples, respectively.

measurements (Fig. 2c). Although point defect has decreased the transport mobility of Kish-G samples (encircled by red oval) in a certain degree, Kish-G mobility is still higher (approximately twice) than that of CVD-G (encircled by blue oval) with similar point defect content. The interior transport mobility of CVD-G compared with that of Kish-G with similar I_D/I_G ratio suggested that point defect was not the main source of the low field effect mobility of CVD-G.

Graphene grown through CVD is generally integrated into devices via substrate transfer and electron beam lithography. The hydrophobic graphene surface was inevitably exposed to resist leading to the surface contamination which cannot be removed using standard solvents, such as acetone or remover[12,13,25]. Contamination may act as external scattering centers and degrade transport properties[32]. Thus, methods of cleaning the surface should be considered. Thermal annealing has been proven to be an efficient method to eliminate residue and restore the clean surface of graphene[33,34]. For that purpose, the CVD-G devices were thermally annealed under nitrogen gas protection. Figure 3 shows the transfer characteristic change of Device 1 via annealing treatment and the inset shows its corresponding optical image. After annealing, CNP decreased from 21 V to 6 V, which indicated that surface contamination was highly reduced[35]. Transport mobility was slightly reduced from 1370 $cm^2/(Vs)$ to 1090 $cm^2/(Vs)$. To eliminate exception from one device data, additional five devices have also been measured, and the corresponding key parameter change is listed in Table 1. Similar to the changing trend of Device 1, all the CNP voltages negatively shifted to 0 V and the mobility of most devices was kept with no considerable change. The exceptional one seriously decreased from one thousand to few

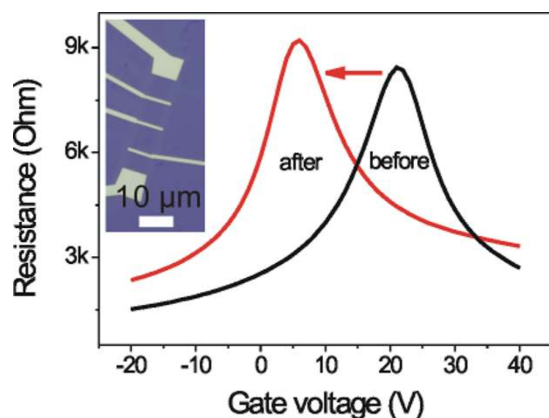

Figure 3 | Thermal annealing treatment to one CVD-G device (Device 1) and its corresponding optical image (inset). The bottom center section is the working channel with 10 μm length and 5 μm width. The CNP decreased from 21 V to 6 V and the transport mobility was slightly degraded.

Table 1 | Summary of the mobility and CNP change of CVD-G devices from the annealing treatment

	Field effect mobility ($cm^2/(V\ s)$)		Charge Neutral point (V)	
Device No.	Before	After	Before	After
1	1370	1090	20	6
2	1510	840	22.5	6.2
3	1040	40	26	11
4	1690	1640	24	13
5	1370	1250	27	4.8
6	900	2400	18	−0.5

tens may be damaged by coupling to the corrugated SiO_2 surface[13]. The relatively clean CVD-G surface and little change in mobility assured that surface contamination was also not the main factor for low mobility.

Aside from point defects and surface contamination, another possible source, namely, line defect, which mainly results from the grain boundaries or stacking faults is also very common in large area graphene sheet especially in CVD-G. To clarify the presence and roles of grain boundary, CVD-G samples were characterized using TEM, SEM, and FET measurements. Prior to the testing of SEM and TEM, more than 10 spots in a wide range distribution of CVD-G samples were tested by Raman to confirm the monolayer nature of our CVD-G[30]. Figure 4a shows the bright field TEM image of CVD-G. Two typical areas denoted by b and c (highlighted by pink dashed circles) were further tested using selected area electron diffraction (SAED), as shown in Figs. 4b and 4c, respectively. Figure 4b only contained one set of six-fold symmetric diffraction spots encircled by one white hexagon, indicating that the corresponding area was a single crystal grain with a diameter as large as 3 μm, whereas Fig. 4c was indexed as two sets of patterns (encircled by one red hexagon), which demonstrated that the viewing field was composed of two coalesced grains. The polycrystalline character of the CVD-G samples was further confirmed by stunting the growth of the CVD-G. An SEM image was obtained during the initial growth stage, as shown in Fig. 4d. Graphene simultaneously grew from the random nuclei (dark area with higher contrast compared with the white area from the uncovered metal surface) and finally merged with each other to form the large area polycrystalline sheet. The above growth process was consistent with the recent report[36]. The random distribution of the grain boundary causes difficulty in quantifying its effect on transport mobility. However, Raman mapping technique can help fabricate the device without the grain boundary. Prior to the device fabrication, the corresponding graphene ribbon was characterized by Raman mapping to confirm the absence of the grain boundary similar like Fig. 1a. Figure 4e was obtained from the short channel (approximately 2 μm in length) FET device without containing the grain boundary. The mobility of this kind of devices reached ~2700 $cm^2/(Vs)$, which was comparative to the data from the Kish-G samples (~3000 $cm^2/(Vs)$) with similar defect content. The enhanced performance of CVD-G samples without grain boundary from the control experiments directly draw the conclusion that the determinant effect was from the grain boundaries.

Although the precise mechanism of the transport mobility degradation led by grain boundary still remains elusive, what is known is that line defect promotes surface reactions with adsorbates from the ambient or with deposited dielectrics[37]. Substituting the network of hexagons with heptagons and pentagons in grain boundary has been observed experimentally, and quantum-transport calculations based on first principles have predicted that periodicity-breaking disorder can adversely affect transport properties[38,39]. The introduction of line defect can give rise to higher surface chemical activity that would further disrupt the sp^2-bonding nature of graphene and thus, affect its fundamental properties. Therefore, the development of the growth method of large single crystal graphene is highly imperative

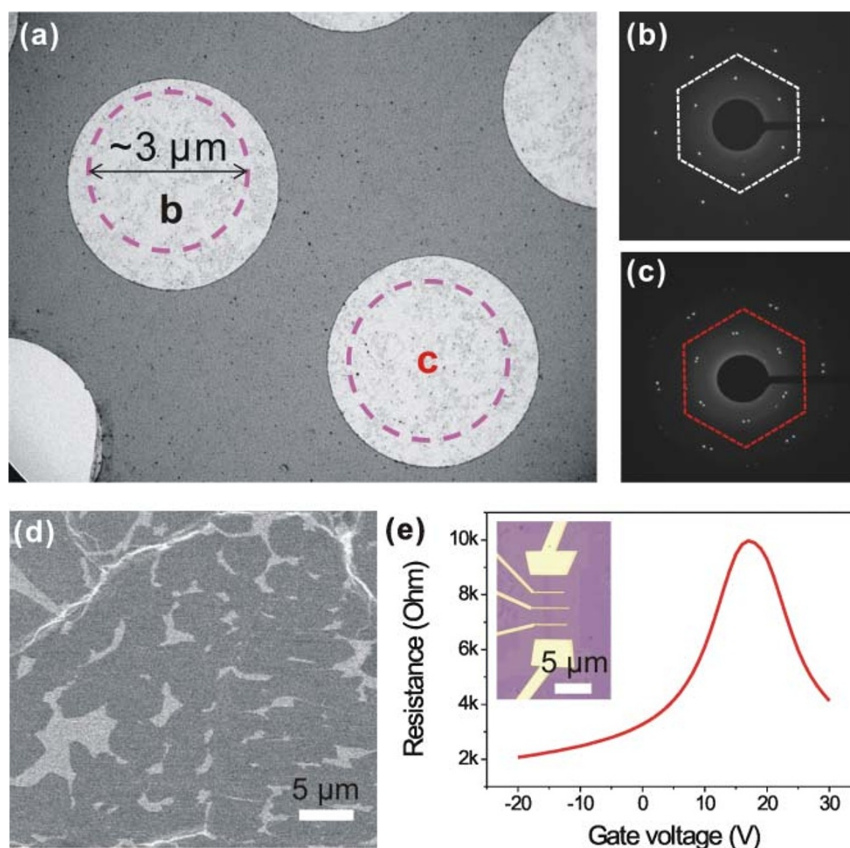

Figure 4 | (a) Bright field TEM image of CVD-G, the pink dashed circle selected area denoted by b and c were further tested by SAED, corresponding to Fig. 4b and 4c, respectively. (b) The SAED pattern is composed of only one set of six-fold symmetric diffraction spots, highlighted by one white dashed hexagon, which indicates the single crystalline grain. (c) Two sets spots (circled by a red dashed hexagon), indicating that the viewing field is composed of two merged grains with small tilted angle. (d) SEM image of the paused growth sample. The higher contrast from the dark grains was divided by uncovered white metal surface. (e) Transfer characters for the short channel device (~2 μm channel length and 1 μm width). The absence of grain boundary demonstrates the comparative transport mobility to Kish-G with similar defect content. Inset shows the corresponding optical image. The bottom center section is the working channel.

to minimize the presence of line defect arising from boundaries between misoriented grains. The interior mobility performance mainly resulting from the grain boundaries was qualitatively explained using a potential barrier model[40]. The CVD-G is assumed to be composed of high and low resistivity areas. The high resistivity region works as the potential barrier, which is typically related to the grain boundaries, and separates the low resistivity area from each other. Assuming that the length, resistivity, and mobility for the low resistivity region (intra-grain) are l_1, ρ_1, and μ_1, respectively, and the corresponding parameters for the higher resistivity region (inter-grain) are l_2, ρ_2, and μ_2, respectively, then the resistivity and the mobility for the whole CVD-G can be expressed as $\rho=\rho_1+\rho_2\beta$ and $\mu=\left(\frac{\alpha}{\alpha+\beta}\right)(\mu_1+2\beta\mu_2)$, where $\alpha={}^{\rho_1}/_{\rho_2}$ and $\beta={}^{l_2}/_{l_1}$[41]. For typical conditions where, $\alpha\ll1$ and $\beta<1$, the expression for the mobility can be simplified as $\mu\approx{}^{\alpha\mu_1}/_{(\alpha+\beta)}$. The introduction of the grain boundary, namely, β increasing, the mobility of CVD-G obviously decreases according to the above expression. This conclusion is also consistent with the current CVD-G related experimental results.

The charge transport mechanism of the polycrystalline CVD-G samples was investigated through temperature dependence conduction. Inset of Fig. 5 shows that resistance slightly increased after the sample cooling down and approximately 18% change had been obtained by varying the temperature from 300 K to 50 K. The plots for the minimum differential conductance versus temperature have been obtained (main panel of Fig. 5) through extrapolation. The small deviation between the cooling down and warming up processes shows the small hysteresis during temperature change. For the relationship between the natural logarithm of conductance *versus* 1000/T, it displays two distinct temperature dependent features. One is the temperature independent region at low temperature; the other is the linear temperature dependence in the high temperature region. In the low temperature part, the conduction of CVD-G is not like the insulator in which the conductance decreases as the temperature decreases. The most likely explanation for the observed temperature independent conduction at low temperature is tunneling[42]. Tunneling through grain boundary barriers requires no thermal excitations and can occur even at zero temperature, it exhibits a temperature independent conductance process. This kind of temperature independent conduction is analogous to the relatively large conductance in the zero-temperature limit often observed in high-conducting polymers and single-walled carbon nanotube networks[43,44]. While in high temperature part, the conduction deviates

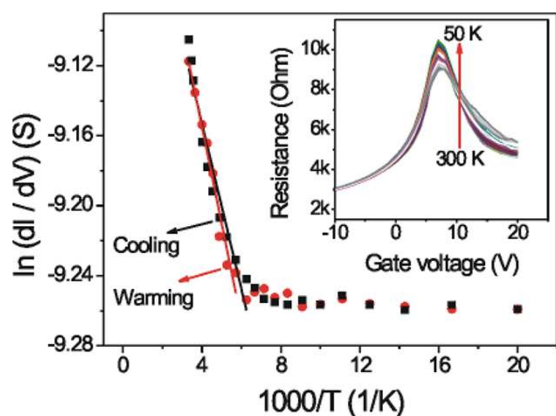

Figure 5 | Temperature dependence of CVD-G conduction. Inset shows the transfer curves which vary as temperature changed. Plots from $\ln(dI/dV)$ *versus* 1000/T show two distinct temperature dependent features, one keeps at a plateau in low temperature part and the other linearly changes at high temperature.

from the constant plateau and shows linear temperature dependence. It can be well fitted by a Arrhenius relation $dI/dV\propto\exp(-E_a/2k_BT)$[42], where E_a is the activation energy and k_B is the Boltzmann constant. The estimated activation energy from the Arrhenius equation is approximately 10 meV which describes the tunneling barrier height that the carriers overcome. Considering the adverse effect to the carrier transport induced by the grain boundary, the utilization of CVD-G in high performance electrical devices should decrease the content of grain boundary or even be absence of it.

Discussion

In summary, the reasons for the relatively low transport mobility of CVD-G were investigated through a series of control experiments. The possible reasons were studied gradually to find its determinant factor. The higher transport mobility (approximately 3000 cm^2/(Vs)) for damaged Kish-G compared with CVD-G (approximately 1100 cm^2/(Vs)) with similar content of defect demonstrated that point defect was not the main source of low mobility. Although thermal annealing treatment could greatly reduce the CVD-G surface contamination, mobility was slightly degraded, which also indicated that surface contamination was not the key factor affecting mobility. Both of TEM and SEM characterizations demonstrated the polycrystalline nature of CVD-G growing from random multi-nuclei. The transport mobility of the short channel devices absent of the grain boundary can reach 2700 cm^2/(Vs). This data was comparative to that of the Kish-G, in such defect degree. Combining SEM and TEM characterizations with the superior performance of the devices without grain boundary shows that grain boundary was the determinant factor for the inferior performance of CVD-G. A potential barrier model has been suggested to qualitatively explain the detrimental effect of grain boundary. Further temperature dependence conduction demonstrated that the charge transport mechanism was attributed to tunneling in the low temperature part and thermal activation in high temperature region. The unfolded origin of relatively lower transport mobility of CVD-G can help remove the block and promote the development of CVD-G.

Methods

The CVD-G samples grown on Cu foil/film utilized in the current study were prepared using the well-developed CVD technique and subsequently transferred to *p*-type heavily doped silicon substrate covered with 285 nm SiO_2 in Reference[9] and[29]. The experimental process can be described briefly as follows. Cu film sputtered on SiO_2/Si substrates was placed in a cold wall type high-vacuum chamber using CH_4 diluted by Ar and H_2 as carbon source. After Ar/H_2 annealing for 20 min, graphene growth was performed at 1000°C under a pressure of approximately 1 kPa for 60 min. For the paused growth samples, the growth time was decreased to 20 min, whereas the other parameters were kept constant. Thermal annealing treatment of CVD-G was conducted using a rapid thermal annealing furnace at 300°C for 30 min under nitrogen gas.

The reference Kish-G samples were prepared via mechanical exfoliation of Kish graphite on SiO_2/Si substrate. Damage effect was introduced to Kish-G by applying low power (20 W) oxygen plasma with variable duration time to obtain the different contents of point defect. The corresponding Raman spectra and electrical measurements were performed in a short time interval (within 10 min) after the occurrence of the damage.

For device fabrication, the obtained graphene samples located on the SiO_2/Si substrate were first patterned into regular geometry using oxygen plasma. Four terminal electrodes were then deposited on graphene using electron beam lithography followed by Ti/Au (5 nm/50 nm) evaporation and a lift-off process. Finally, back-gate field-effect transistors (FETs) were fabricated using a standard procedure. All Raman measurements were carried out under ambient atmosphere and temperature, whereas electrical measurements were performed under a four-terminal geometry in a sample-in-vacuum (approximately 5×10^{-7} mbar) cryostat with a temperature range of 50 K to 300 K.

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Author contributions statement

S.H.S and K.T. planned the experiments. S.S., K.H., A.Y., N.Y. fabricated the CVD-G and characterized it by SEM and TEM. H.S.S., S.L.L. and H.M. performed the oxygen plasma damaging, thermal annealing experiments and processing of the data. All authors contributed to the discussion of the results. S.H.S and K.T. wrote the paper.

Additional information

Competing financial interests: The authors declare no competing financial interests.

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