Overtemperature Protection Circuit for GaN Devices Using a *di/dt* Sensor

Mohammad H. Hedayati, Jianjing Wang, Harry C. P. Dymond, Dawei Liu, and Bernard H. Stark

***Abstract*—Power semiconductor devices have maximum junction temperature limits, but it is not straightforward to sense or infer temperature inside sealed devices in running converters. One method is to observe electrical behavior that is known to be temperature dependent. For example, in some gallium nitride (GaN) power semiconductor devices, the maximum slope of the device current at turn-ON has been shown to reduce as the junction temperature increases. This article demonstrates the first noncontact overtemperature protection circuit for GaN power devices that exploits this effect and overcomes the complication that this inverse proportionality is affected by load current. A variant of a previously reported magnetic field "Infinity Sensor," named after its figure-of-eight topology and high bandwidth (>200 MHz), measures *di/dt*. Using the sensor signal as the only input, a detection circuit finds peak *di/dt*, and a high-speed integrator derives instantaneous load current. The reference voltage for the decision-making part of the circuit is automatically adjusted as a function of load current, in order to counteract the dependence of *di/dt* on load current. Experimental results on a 400 V, 2 kW buck converter show the protection circuit successfully activating within ±5 °C of a preprogrammed junction temperature setting, independently of load current, for settings of 100, 120, and 140 °C.**

***Index Terms*—Gallium Nitride (GaN), indirect temperature sensing, overtemperature protection, temperature-sensitive electrical parameters (TSEPs), turn-ON *di/dt,* wideband gap.**

I. Introduction

PROTECTION circuits are typically necessary to make a power converter robust, increase functionality, and achieve sufficient reliability [1]–[3]. In particular, the control scheme of the converter should be capable of protecting the switches against overtemperature. A general practice in the industry is to place temperature sensing chips on the board, as close as possible to the switching devices, or, in systems using modules, the modules will often include a thermistor attached to the substrate. The temperature reading signals are fed back to the controller and calibrated for a critical temperature point. This method only works for gradual temperature rises and could have significant error in the case of sharp temperature rises.

The move from silicon IGBTs to Gallium Nitride (GaN) field effect transistor (FETs) has a significant impact on temperature sensing. Whilst the faster switching provides lower per-transient switching loss [4], the thermal characteristics are actually more challenging: smaller device packages and dies have lower thermal mass and increased thermal resistance. Lower thermal mass means the die will heat up faster for a given transient loss, limiting transient loss capability. Higher thermal resistance makes it harder to transfer heat to a cooling system, limiting total loss capability. As a result, GaN circuits are more thermally vulnerable than their silicon counterparts. In addition, sensing in these circuits is generally harder, as the order of magnitude higher switching rates significantly increases noise mechanisms such as near-field-coupled common-mode interference, and there is less space for sensors, as the faster switching requires more compact circuit layouts. And finally, response times need to be faster, and measurement bandwidths need to be higher.

For these reasons, temperature sensing in GaN circuits is more challenging than for silicon. Direct [4], [5] and indirect [6] sensing techniques have been reported for GaN temperature measurement. Direct measurement uses a physical sensor to measure the temperature. For example, in [4], an integrated GaN-on-SiC heterojunction diode is shown to monitor junction temperature of a GaN power device. Texas Instruments offer 600 V GaN devices with integrated driver, overcurrent protection, and overtemperature protection [7]. It is reported that overtemperature shutdown prevents thermal runaway of the chip. However, the response time of the protection is not stated. Also, IGBT modules sometimes contain a thermistor in the package. Accurate junction temperature estimation can be achieved, if the thermal impedances in the path from the junction to the thermistor are known, bearing in mind that some of these parameters may change as modules age. Indirect temperature indicators could eliminate the need to understand the thermal path, relying instead on knowledge of how device behavior changes with temperature, which, again, may change as devices age. Usually referred to as temperature-sensitive electrical parameters (TSEPs), these temperature indicators include gate threshold voltage [8], quasi-threshold voltage [9], internal gate resistance [8], ON-state resistance [8], bias temperature instability [10], drain current gradient [11], [12], and gate current leakage [13]. This literature generally quantifies the linearity

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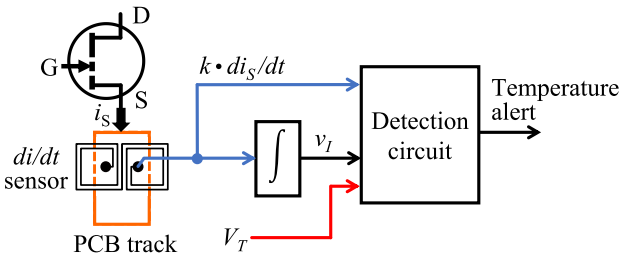

Fig. 1. Temperature alert concept using a *di/dt* sensor.

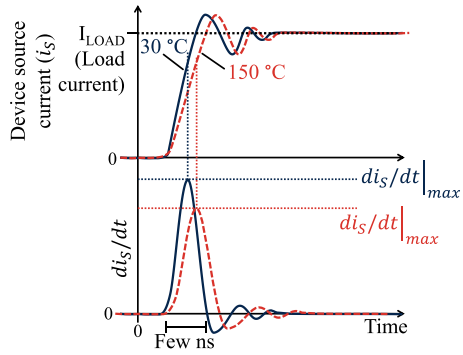

Fig. 2. Concept waveforms, at the instant of device turn-ON, of the source current and its time derivative, for a hard-switched GaN device at different temperatures.

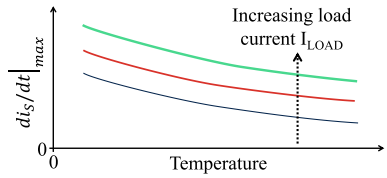

Fig. 3. Illustration of GaN device $di_S/dt|_{\max}$ against temperature at different load currents.

and sensitivity of these indicators, and studies their limitations due to device-to-device variability and parameter drift, with side-by-side comparisons provided in [8], [14], and [15].The almost-linear dependence of *di/dt* on the GaN device junction temperature is shown in [12].

This article presents the first "noncontact," online junction-temperature alert circuit for hard-switched GaN power devices, exploiting this temperature-dependence of device current gradient di_S/dt at turn-ON. The concept is illustrated in Fig. 1. A *di/dt* sensor provides a voltage signal $k \cdot di_S/dt$, where *k* is a constant of proportionality inherent to the sensor, i.e., a signal that, within bandwidth limits, is proportional to the GaN device source current gradient di_s/dt. This signal is integrated and scaled to provide a voltage signal v_I that represents instantaneous device source current i_s, from which load current I_{LOAD} can be estimated. These two voltage signals and a reference voltage V_T, representing a user-selected temperature threshold T_{SET}, are fed into an analogue detection circuit, which generates an alert signal if the GaN device junction temperature is higher than T_{SET}.

Section II analyzes the variation of *di/dt* with temperature, and the device turn-ON event, to show that in hard-switched scenarios peak *di/dt* is a function of I_{LOAD}; hence, the need for knowing both di_s/dt and I_{LOAD} to determine device temperature.

The junction-temperature alert concept that compensates for load current changes and that uses only a single *di/dt* input signal is explained in more depth in Section III.

Section IV details the design of the required high-speed integration and comparison circuits, using commercially available low-cost analogue components and a modified version of the current sensor reported in [12]. The sensor has insertion inductance of only 0.2 nH, allowing it to be placed into the power loop of a GaN FET bridge-leg without significantly affecting switching speed.

Section V explains the hardware implementation of the sensing and protection circuits, and a 2 kW, 400 V GaN half-bridge power converter with active device temperature control for test purposes. Before use, the protection circuit must be calibrated using experimental data from double-pulse tests; this procedure is detailed in Section VI.

The results presented in Section VII show the converter operating at up to 2 kW, over a range of load currents and switching frequencies. The protection circuit is shown to trigger at the correct junction temperature and to respond sufficiently quickly for use in GaN converters.

II. Temperature Sensing in GaN FETs Using *di/dt*

A. Temperature Dependence of Peak Current Gradient $di_S/dt|_{\max}$

The upper graph in Fig. 2 illustrates the temperature dependence of a hard-switched GaN device's current transient at turn-ON. The higher temperature is seen to reduce the gradient di_s/dt. It is presented in [16] that: "One notable feature of this GaN HFET is that its transconductance drops significantly as the junction temperature increases." The lower transconductance, at higher temperature, results in lower switching speed and consequently lower *di/dt*. The lower transconductance is caused by a reduction of device electron mobility with increasing temperature [17].

In practice, a temperature rise of 100 °C reduces the current gradient by around 25% [18]. The lower waveforms in Fig. 2 are the time-derivatives of the current waveforms. Here, it is apparent that a higher device temperature also results in a lower peak of the current gradient ($di_S/dt|_{\max}$). The inverse proportionality between peak gradient and temperature is illustrated in Fig. 3.

B. Why Peak di/dt Is Selected Among all the TSEPs

As discussed in Section I, there are several TSEPs that could potentially be used to infer the junction temperature of GaN devices. Online measurement of any of these TSEPs, including *di/dt*, is challenging in terms of computation, isolation, and signal sensitivity. Furthermore, many TSEPs, such as V_{TH} or R_{dson}, cannot be directly measured and must themselves be somehow inferred.

TABLE I
TYPICAL SIGNAL MAGNITUDES AND SENSITIVITIES OF VARIOUS TSEPs

TSEP	Signal derived from	Signal magnitude	Signal sensitivity
Turn-on rise time [18]	High-bandwidth measurement of i_D	3.7 – 4.9 ns	12 ps/°C
R_{dson} on-state resistance [18]	Measurement of i_D and v_{DS} and computed by v_{DS}/i_D	50 – 128 mΩ	0.62 mΩ/°C
R_{gint} gate internal resistance [8]	Measurement of i_G and v_{GS} and computed by v_{GS}/i_G	2 Ω	2.9 mΩ/°C
Gate threshold voltage [8]	Time-synchronised measurement of v_{GS} and i_D	1.4 V	2.9 mV/°C below 60°C; −3.9 mV/°C above 60 °C
Peak of turn-on *di/dt*	Directly measured by modified version of Infinity Sensor	1 – 1.5 V	5 mV/°C

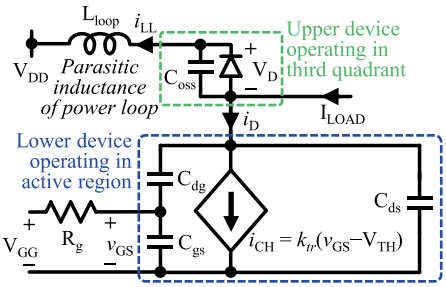

Fig. 4. Circuit model used to represent a GaN bridge leg during the turn-ON transient of the lower device. Load current is flowing into the switch node.

Measuring the source current and taking the derivative would be challenging as derivative circuit outputs are very noisy and not recommended in practice. However, for the sensor used in this work (a modified version of the Infinity Sensor [12]), *di/dt* is directly measured and its output is galvanically isolated. A further benefit is a high signal-to-noise ratio: the peak output of the sensor is between 1 and 1.5 V and has sensitivity of about 5 mV/°C (i.e., 500 mV per 100 °C). This can be easier to robustly detect as compared to the aforementioned 25% change in gradient, and compares favorably with many other TSEPs, as summarized in Table I.

C. $di_S/dt|_{\max}$ Dependence on Load Current

The peak *di/dt* not only depends on temperature, but it also increases with load current, as illustrated in Fig. 3. This is a property of hard-switched bridge legs that use power devices whose transconductance increases with current. Consider the simplified circuit of Fig. 4, which models a bridge leg at the end of a deadtime period, where current is commutating from the "OFF" upper device to the lower device. The upper GaN device's third-quadrant operation and output capacitance are modeled by a diode and capacitor $C_{\rm oss}$, respectively, whilst the lower device is modeled as a voltage-controlled current source and the parasitic capacitances $C_{\rm gs}$, $C_{\rm dg}$, and $C_{\rm ds}$.

Once the gate-to-source voltage ($v_{\rm GS}$) reaches the threshold voltage ($V_{\rm TH}$), the channel begins to conduct and the load current $I_{\rm LOAD}$ starts to divert from the upper device to the lower

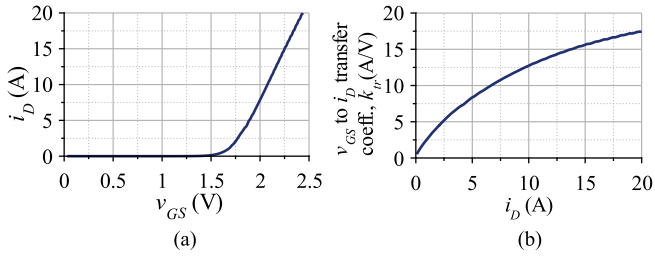

Fig. 5. (a) i_D versus $v_{\rm GS}$ characteristic, at 25 °C, of the GaN device used in this article: the GS66508T from GaN Systems. (b) Transistor's $i_D - v_{\rm GS}$ transfer coefficient k_{tr} as a function of current, calculated from $i_D = k_{tr}(v_{\rm GS} - V_{\rm TH})$.

device. The changing current results in a voltage drop across the parasitic loop inductance $v_{\rm Lloop}$. Throughout the current switching transition, a portion of $I_{\rm LOAD}$ flows through the upper device, and the lower device's drain terminal is thereby pulled up to $V_{\rm DD} - v_{\rm Lloop} - V_D$, through the diodelike behavior of the upper device operating in the third quadrant. The lower device is, therefore, operating in the active region, and its channel current $i_{\rm CH}$ is given by the following equation:

$$i_{\rm CH} = k_{tr}\ (v_{\rm GS} - V_{\rm TH}) \tag{1}$$

where k_{tr} is a large-signal parameter related to the small-signal transconductance of the device. Fig. 5(a) shows the $i_{\rm D}$ versus $v_{\rm GS}$ characteristic for the device used in this work. This dc characterization, where $i_{\rm CH}$ is equal to $i_{\rm D}$, is extracted from the manufacturer's "level 3" Spice model [19], [20] and verified to closely match the datasheet curve. From this, $V_{\rm TH}$ is determined—taken to be the value of $v_{\rm GS}$ for a drain current of 10 mA; in this case, 1.29 V—and k_{tr} is calculated as a function of $i_{\rm D}$, as shown in Fig. 5(b). As the device drain current increases, k_{tr} also increases. From (1), this implies that, for a fixed gate-drive strength, switching larger currents will result in a larger *di/dt*.

Whilst this is the dominant mechanism that influences the relationship between $I_{\rm LOAD}$ and peak *di/dt*, the trajectory of i_D is determined by several factors including parasitic inductances and capacitances, and the level of damping in the circuit [21]. These additional influences on peak *di/dt* have been investigated with the more detailed LTspice model shown in Fig. 6. Here, Q_1 is GaN System's "level-3" Spice model, and a zero-volts voltage source Id is used to measure its drain current.

Cdamp and Rdamp are introduced as a simplified way to model the effects of high-frequency damping that occurs in physical circuits due to skin effect and other loss mechanisms. C2 models the parasitic capacitance of the circuit layout at the switch node, whilst Lout includes parasitic elements as noted in the figure caption. For realistic value ranges for R_g, $L_{\rm loop}$, and damping, as described in Table II, peak *di/dt* is always a function of $I_{\rm LOAD}$, but the shape of this function changes. The presented analysis is valid for hard-switched converter topologies that use power devices whose transconductance increases with current, and whose switching cells can be modeled as bridge-legs with similar ranges of parasitic circuit values.

To model the target system in this article, R_g is set to 10 Ω, $L_{\rm loop}$ to 2.5 nH, and Rdamp to 10 Ω, giving peak *di/dt* versus

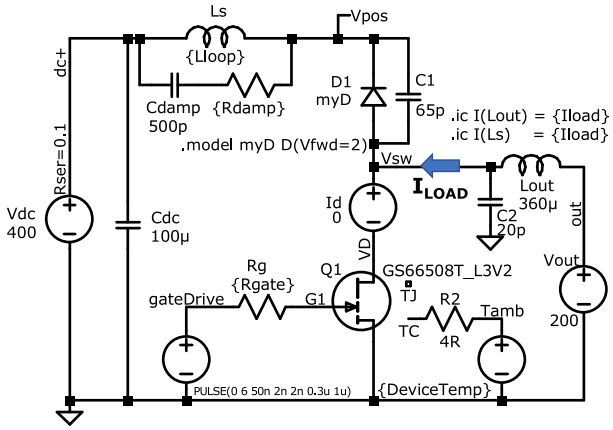

Fig. 6. More detailed LTspice circuit model. Lout has parasitic capacitance of 20 pF, series resistance of 10 mΩ, and parallel resistance of 12 kΩ.

TABLE II
CIRCUIT ELEMENT VALUE RANGES

Circuit Element	Value Range
R_g	2 Ω to 22 Ω
L_{loop}	1 nH to 4 nH
Rdamp	2 Ω (heavy damping) to ∞ Ω (no damping)

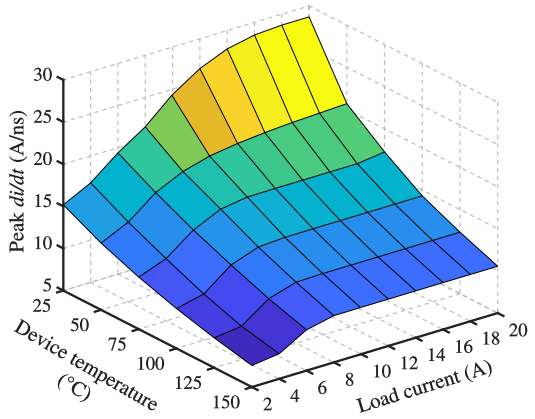

Fig. 7. Peak di/dt as a function of device temperature and load current, for the circuit of Fig. 6, with $R_g = 10\ \Omega$, $L_{\text{loop}} = 2.5$ nH, and $R_{\text{damp}} = 10\ \Omega$.

device temperature and I_{Load}, as shown in Fig. 7. It is evident that the protection circuit must account for the variation of peak *di/dt* with load current. This is accomplished with a simple analogue circuit presented in Section IV-B.

It is worth noting that all of the factors that influence the shape of the *di/dt* versus current and temperature relationship would be fixed for any given design. Once a power stage has been designed, including layout and gate-drive regime, the resulting peak *di/dt* versus I_{LOAD} relationship can be factored into the design of the protection circuit. Due to the large number of parasitic components involved, analytical expressions that relate device parameters and circuit parasitics to the exact *di/dt* versus temperature and current relationship are not intuitive or tractable. Furthermore, extracting all the parasitics from a

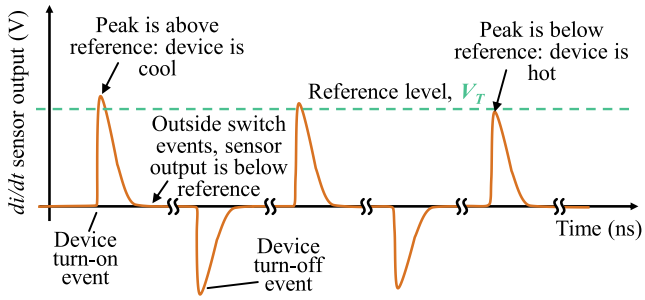

Fig. 8 Idealized output from *di/dt* sensor as GaN device heats up. For clarity, a constant temperature reference level is shown; however, this needs to be adjusted as the load current changes.

system to input into the protection circuit design would be excessively time consuming. The proposed method is, therefore, to build flexibility into the protection circuit, to allow its response to be tuned according to measured circuit behavior. Currently, calibration is performed manually. An important area of future research is to identify ways in which the calibration procedure could be simplified, automated, or possibly obviated.

D. Influence of GaN Device Parameter Instabilities

Some GaN devices exhibit instabilities, such as gate threshold voltage (V_{TH}) shift and current collapse [22], [23]. It may be possible that such instabilities could affect the *di/dt* versus temperature relationship and impact the accuracy of the temperature-protection circuit.

Normally these instabilities manifest when the device conditions change. For example, the gate drive voltage changes, or the power converter is energized and deenergized. However, we have confirmed that once the power converter is started and stabilized, the device parameters also stabilize, i.e., after a short period of operation, the device V_{TH} will shift to a stable value, this value being repeatable from one circuit energization to another. Therefore, in the case of these devices, circuit operation stabilizes to a repeatable state, enabling the temperature protection circuit to operate in a repeatable manner.

III. SYSTEM ARCHITECTURE

The central function of the system is to compare the positive peaks of the *di/dt* sensor's output ($k \cdot di_S/dt|_{\max}$) to a voltage reference V_T, the value of which is derived from the user-selected temperature threshold T_{REF}. The k challenges in this article are as follows.

1) Higher temperatures correspond to lower peaks, but the sensor output is zero outside of switching events, as illustrated in Fig. 8. As such, it is not sufficient to simply continuously compare the sensor's output to a reference level.
2) Current transients have a duration of units to tens of nanoseconds, so the peaks in the *di/dt* sensor output are very narrow.
3) The reference level V_T has to be adjusted as the converter load current changes.

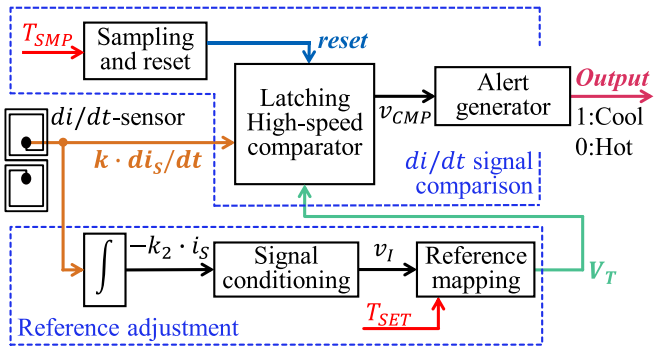

Fig. 9. Temperature alert architecture using a single *di/dt* sensor.

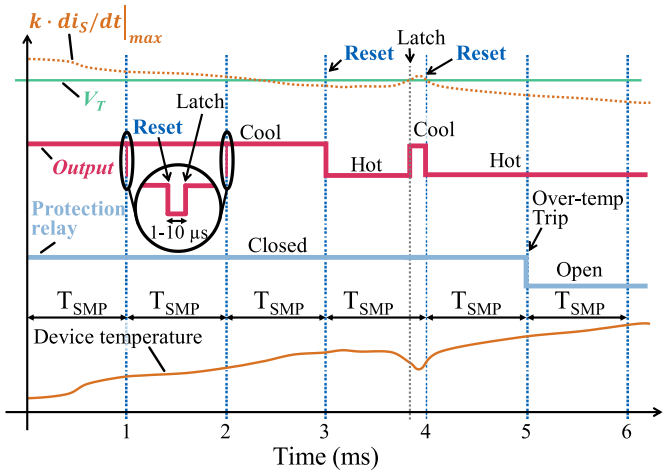

Fig. 10. Operating principle of the proposed temperature alert system for the case of a GaN device gradually heating up. For clarity, the figure shows a constant temperature reference level; however, this is adjusted as the load current changes.

The solution adopted here is shown in Fig. 9. There are three subsystems: sensor, temperature reference adjustment, and *di/dt* signal comparison.

The reference adjustment block generates the voltage reference V_T , the value of which depends on the user-selected temperature limit T_{SET} (set via a potentiometer) and that is corrected up or down depending on device ON-state current I_{LOAD}. This current is determined by integrating and conditioning the $k \cdot di_S/\mathrm{dt}$ signal. The reference adjustment circuit is calibrated using experimental data.

The operating principle of the *di/dt* comparison circuit is illustrated in Fig. 10. The circuit compares the peak of the $k \cdot di_S/dt$ signal against the corrected reference V_T. The output is an alert indicating either 1 (cool) or 0 (hot), corresponding to whether the device junction temperature is cooler or hotter than the set temperature T_{SET}. The latching high-speed comparator is regularly reset by the *reset* signal with period T_{SMP} as set by the user and is followed by a slow-response alert generator block. When reset, the high-speed comparator output becomes low. Subsequently, a *di/dt* event whose peak is above the threshold (device is "cool") causes the comparator output to latch to high, whilst for a *di/dt* event below the threshold (device is "hot"), the output will stay logic low. Under normal operation with "cool" devices, the comparator output is therefore normally high, with brief low-going pulses occurring on each *reset* pulse. Because the *reset* signal is not synchronized to the power converter switching events, the maximum duration of this low-going pulse is equal to the converter switching period. The response time of the protection relay following the alert generator circuit is chosen such that the output signal must stay logic low for at least 1 ms in order to generate the trip signal.

Hot–cool transitions can occur instantly, whereas cool–hot transitions can occur only after sampling/reset points. This helps to avoid false alerts.

IV. Circuit-Level Design

A. *di/dt Sensor*

Current sensors that are designed for measuring transient currents in silicon and silicon carbide (SiC) devices [24], [25] are generally not suitable for observing the switching transients in GaN devices, due to their relatively high insertion inductance. For instance, the high-bandwidth 2 GHz coaxial shunt from T&M research [26] has an insertion inductance of 2 nH. This is of the same order as the switching loop inductance of a GaN bridge leg and is, therefore, large enough to significantly affect switching performance, for example, by slowing down transients or causing excessive ringing. The cost and/or physical size of such devices would also be prohibitive for many applications. Lower-inductance shunts have been reported (e.g., 0.3 nH in [27]); however, these still use appreciable PCB area, generate heat, and are not floating. Also, in order to obtain the derivative of the current, an active differentiator would be required with the drawback that these are highly sensitive to high-frequency noise.

Therefore, a magnetic field sensor, which responds to di_{s} */dt* directly, and can measure *di/dt* up to around 10 A/ns, is used in this article. It is a planar Rogowski coil based on the Infinity Sensor concept of Wang *et al.* [12], where two windings on either side of the current-carrying conductor are connected to cancel out any influence from distant currents [28]. The key advantage of the Infinity Sensor over a Rogowski coil is significantly lower insertion impedance of only 0.2 nH and 4.2 mΩ. This is due to its planar topology that can be implemented at millimeter scale (e.g., 3 × 10 × 1 mm) in PCB technology, and without breaking the underlying power PCB layers that contain the power loop's current return path. The drawbacks over shunt resistors are the sensitivity to *dv/dt*, and the absence of an absolute transfer function, as the gain is dependent on the positioning and trace geometry. In order to avoid common-mode voltage coupling capacitively into the sensor, it can be placed at the low-side source, or high-side drain in a bridge leg. The sensor used here has two concentric in-plane turns per side, as shown in Fig. 11, double the windings of the sensor in [12], which roughly quadruples the gain from 110 to 450 mV/(A/ns). The coils track width is 6 mil (0.15 mm); this can be even smaller depending on the PCB manufacturing capabilities. Two electrically isolated solder pads on the bottom of the sensor are used to attach it to the power converter PCB.

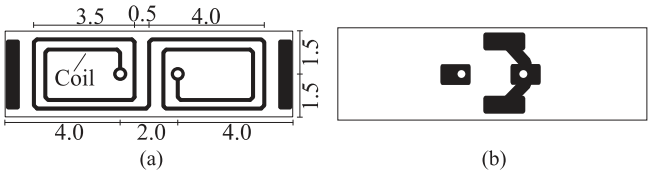

Fig. 11. 2-D renders of the infinity sensor variant design used in this work. (a) Bottom view (sense coils with vias to top side; dimensions in mm). (b) Top view (vias from bottom side with solder pads for U.FL connector).

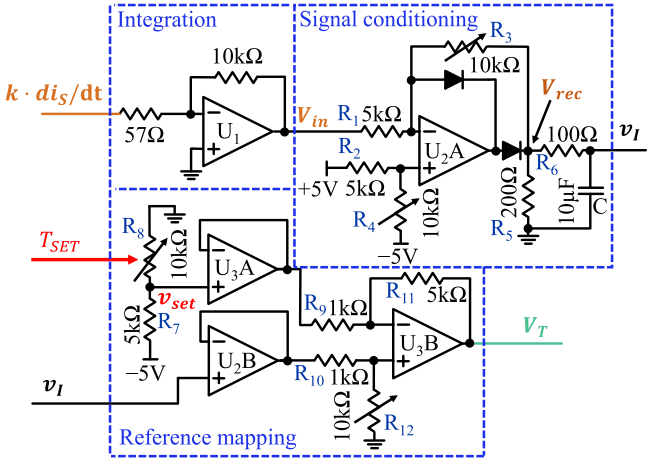

Fig. 12. Electrical circuit diagram for the reference adjustment block of Fig. 9.

When the sensor is positioned above the 6-mm-wide current-carrying trace on the power converter PCB, the total vertical distance between the coils and the current-carrying trace is 200 μm, consisting of two solder masks with thickness of 50 μm each, and additional 100 μm Kapton tape added for safety.

B. Reference Adjustment Circuit

The circuit for the reference adjustment is shown in Fig. 12. The measured *di/dt* pulses have a duration of only around 7 ns. The bandwidth of this signal is of the order of 150 MHz, and it must be integrated to create a load-current signal whose amplitude is large enough (>mV) for further processing in a noisy environment. An ideal integrator with sufficient gain at 150 MHz would imply an impractically large low-frequency gain where any noise or offset would saturate the output. A lossy integrator (low-pass filter) response is, therefore, used to limit low-frequency gain. Traditionally, a low-pass response is implemented using an op-amp with a capacitor in the feedback path. However, using such an approach here, with the very wide bandwidth requirement of a closed-loop unity-gain crossover point close to 300 MHz, would require a unity-gain stable voltage-feedback op-amp with at least 3 GHz gain-bandwidth product in order to maintain a loop gain of at least ten. An alternative approach is used here, where the open-loop integration response of U1 (AD8045; a single dominant-pole compensated op-amp with unity open-loop gain at 400 MHz [29]) is exploited—no feedback capacitor is necessary because the closed-loop response will naturally asymptote to the open-loop

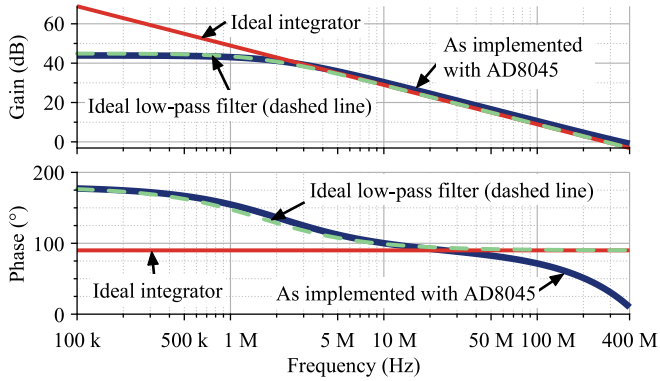

Fig. 13. Simulated frequency response of the integration circuit (U1), as shown in Fig. 12, and the equivalent ideal integrator responses.

response [30], [31], to give the desired response, as illustrated in Fig. 13.

The output of the integration circuit (U_1) passes through a precision rectifier (U_2A) whose gain and dc offset are adjusted using potentiometers R_4 and R_3. The input–output relation of this circuit is given in (2) and (3). An *RC* low-pass filter is provided to filter out high-frequency ac components. The output signal of this stage v_I is a voltage that is proportional to the device ON-state current. The output of the low-pass filter is given in (4).

$$v_+ = 10\frac{R_4}{R_2 + R_4} - 5 \tag{2}$$

$$V_{\text{rec}} = \begin{cases} 0 & \text{if } v_+\left(\frac{R_1}{R_3}+1\right) < V_{\text{in}} \\ v_+\left(\frac{R_3}{R_1}+1\right) - V_{\text{in}}\frac{R_3}{R_1} & \text{if } v_+\left(\frac{R_1}{R_3}+1\right) \geq V_{\text{in}} \end{cases} \tag{3}$$

$$v_I = \frac{1}{1 + j\,(\omega RC)}\,V_{\text{rec}}. \tag{4}$$

In the reference-mapping circuit of Fig. 12, a dc offset determined by the T_{SET} temperature-threshold setting potentiometer R_8 is added to the v_I signal by differential amplifier U_3B. The gain of this amplifier is adjusted using a potentiometer R_{12}. The output of this stage is the reference level V_T that is passed on to the signal-comparison circuit. The process used to adjust the potentiometers to give the desired circuit response is detailed in Section VI. The input–output relation of the reference mapping circuit is given in the following equations:

$$v_{\text{set}} = -5\frac{R_8}{R_7 + R_8} \tag{5}$$

$$V_T = v_I \times \frac{R_{12}}{R_{10} + R_{12}}\frac{R_9 + R_{11}}{R_9} - v_{\text{set}} \times \frac{R_{11}}{R_9}. \tag{6}$$

The signal conditioning and reference-mapping circuit used here has been optimized for the fixed operating conditions of the demonstration power converter. As such, responses to changes in load current are slow. For applications with more dynamic operation, a circuit with a faster response time would be needed, for example, replacing the signal-conditioning block with a fast

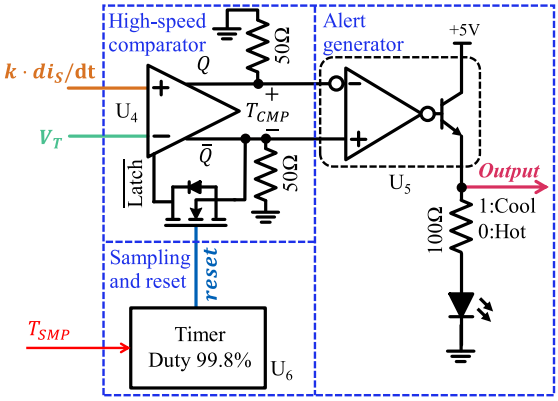

Fig. 14. Electrical circuit diagram of the signal comparison parts of Fig. 9.

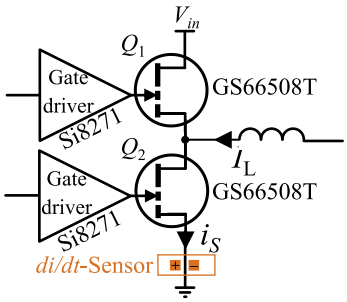

Fig. 15. Power circuit used to demonstrate junction temperature sensing via *di/dt*.

peak-detect circuit with a decay rate optimized for the specific operating conditions.

C. di/dt Signal Comparison Circuit

The *di/dt* signal comparison circuit is shown in Fig. 14. It consists of a high-speed comparator, alert generator, and sampling and reset circuits.

A high-speed comparator ADCMP553 compares the $k \cdot di_S/\mathrm{dt}$ signal against V_T. The outputs of the comparator are differential signals v_{CMP} , using the Q and $\bar{Q}$ pins. The $\overline{\mathrm{Latch}}$ pin is connected to the $\bar{Q}$ pin using a MOSFET, in order to latch the comparator when the $k \cdot di_S/dt$ signal exceeds V_T. To release the latch, the sample and reset signal $reset$ is pulled down. The reset period T_{SMP} is set with a potentiometer in a timer circuit, which in turn generates the $reset$ signal, which is a square pulse train with a 99.8% duty.

The alert generator block is an output buffer that limits the loading of the high-speed comparator. A falling edge at the output indicates an overtemperature alert, to be used in any subsequent protection circuit. The buffer comprises a low-speed comparator LM311 driving a solid-state protection relay TLP227G.

V. Hardware Implementation and Experimental Method

Fig. 15 shows a schematic of the GaN FET bridge-leg used to demonstrate temperature sensing. A 3 × 10 mm Infinity Sensor measures *di/dt* in the source of the lower device, which has

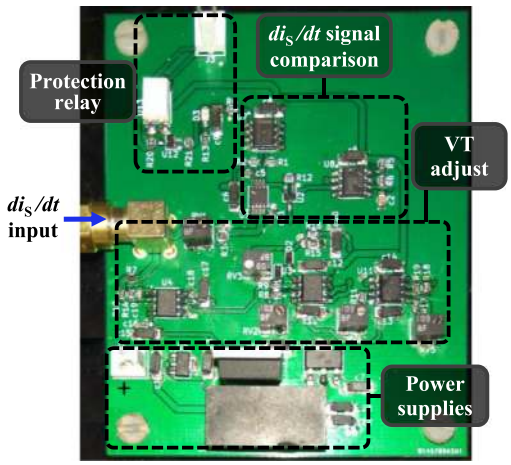

Fig. 16. Fabricated overtemperature alert system with protection relay.

required the source trace to be extended by 3 mm, resulting in an increased loop inductance of around 0.2 nH (the return current runs underneath this trace, on the next layer down in the PCB stack). The sensor output signal is connected to the sensing circuitry, shown in Fig. 16, via a U.FL connector and a 50 Ω coaxial cable.

In this configuration, Q_2 is the active device and operates in the hard-switched mode at turn ON, whilst Q_1 is the synchronous device and operates in the zero voltage switching (ZVS) mode at turn ON. This method cannot be used for devices with ZVS operation, as ZVS does not generate the required device-dependent *di/dt*. If Q_1 were the active device, the sensor could be moved to the drain side of Q_1. In converters where, depending on circuit conditions, either device could be the active one, such as bidirectional dc-dc converters or inverters, two sensors could be used—one in the drain of the high-side and the other in the source of the low-side. A selection circuit could then determine the appropriate sensor output to route to the temperature detection circuit.

The overtemperature protection board accommodates the reference adjustment (see Fig. 12) and signal comparison (see Fig. 14) circuits. It also includes a protection relay that is connected to the interlock of the power converter's input power supply. In the case of an overtemperature event, the relay shuts down the power supply.

The topside of the power board is shown in Fig. 17. A 12 V, 40 W ceramic heater cartridge, whose temperature is regulated with an Inkbird ITC-100RL controller, is used to bring the circuit into the thermal steady state. This heater is thermally attached to the GaN device that is mounted on the underside of the power board. A TESTO 875-1I thermal camera is used to measure the temperature of a via placed on the source pad of the bottom device. This area of the topside of the PCB (facing the thermal camera) is the closest in temperature to the device junction temperature—on the other side of the board, the devices are obscured by the heat plate, or in later experiments, the power devices' heatsink.

The GaN bridge leg on the underside of the PCB is shown in Fig. 18. This 2 kW, 400 to 200 V dc–dc converter uses GaN

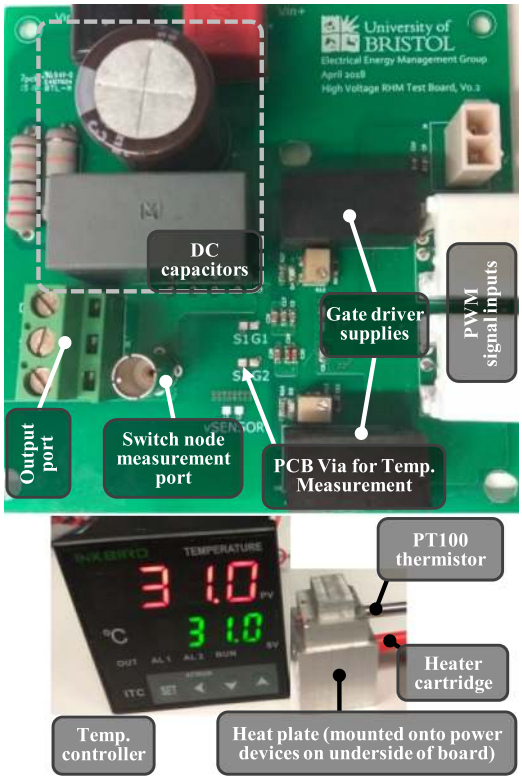

Fig. 17. Top side of the power board, showing temperature measurement via and temperature-controller setup. The power devices are mounted on the bottom side of the board (see Fig. 18).

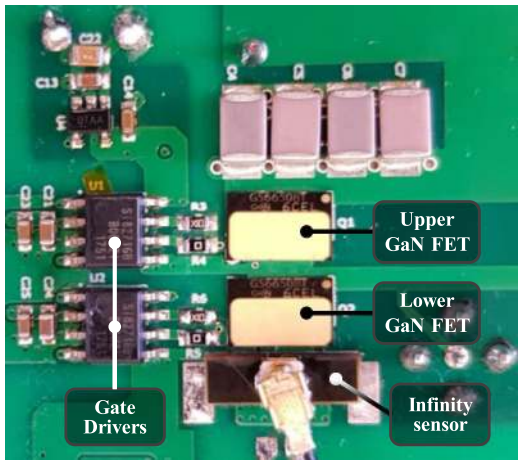

Fig. 18. Underside of the power board. A 2 kW GaN bridge leg, with Infinity sensor in the source of the lower device.

Systems GS66508T top-side-cooled devices (650 V, 50 mΩ). An EA-EL 9500-60B electronic dc load is used to vary the load up to 2.0 kW. Note that the load is referenced to the converter's positive rail, so current flows into the switch node.

VI. Protection Circuit Calibration

Before the protection circuit can be used in an operational converter, the temperature sensing must be calibrated with the

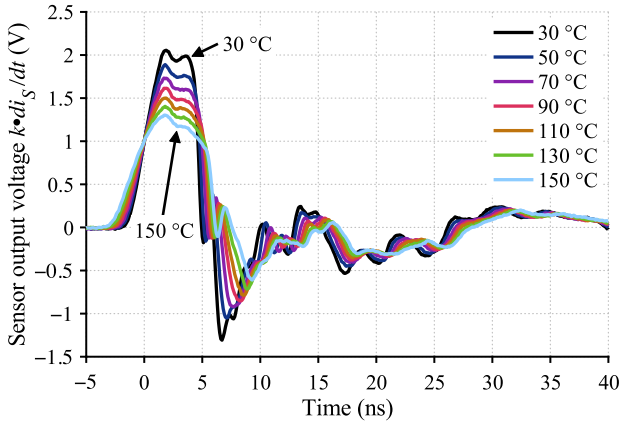

Fig. 19. Measured sensor output voltage ($k \cdot di_S/dt$), for load current of 10A and device temperatures from 30 to 150 °C.

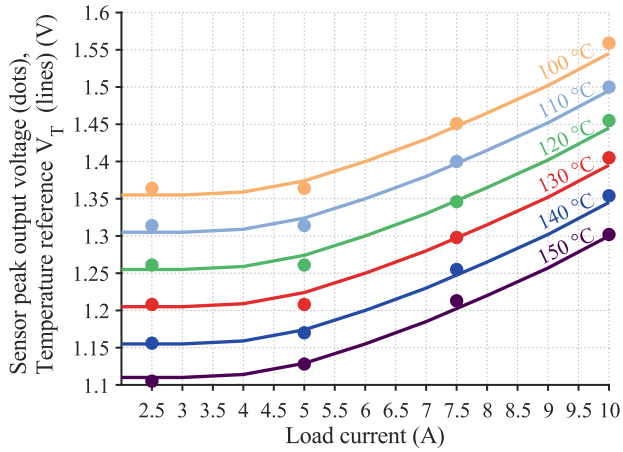

Fig. 20. Measured sensor peak output voltage (dots), and the measured temperature reference V_T (solid lines), after calibration of the reference adjustment circuit.

Infinity Sensor *in situ*, using experimental data from double-pulse tests at different temperatures and current levels.

The bridge leg is stabilized at a specific temperature, using a heat plate, so that the junction temperature is close to the case temperature. Then a double pulse test is carried out to obtain a switching cycle at 10 A of load current. The $k \cdot di_S/dt$ signal is captured using a 2 GHz, 10 GS/s, Rohde & Schwarz RTO1024. This process is repeated to obtain the sensor output waveforms of Fig. 19, for temperatures from 30 to 150 °C. As the temperature increases, the peak of $k \cdot di_S/dt$ is seen to reduce, resulting in an average sensitivity of −6.41 mV/°C.

This test is carried out at load currents 2.5, 5, 7.5, and 10 A, and at temperatures from 100 to 150 °C in steps of 10 °C, in order to obtain the measured peak gradients $k \cdot di_S/dt|_{\max}$ in Fig. 20. This provides the required data for calibration. The self-heating of the device during the double-pulse test increases the device temperature. This self-heating is simulated using the parameters provided in [18] for a double-pulse test at 10 A. It is found that the junction temperature increases by only 0.7 °C, and hence, if the heat plate is set to 100 °C, the junction temperature at the

end of the 10 A test is around 100.7 °C. As a result, self-heating is neglected here.

The reference adjustment circuit must be calibrated, to increase V_T by the required amount as load current increases. The gains and offsets are tuned, using the potentiometers shown in Fig. 12, such that the generated reference V_T (solid lines in Fig. 20) lies as close as possible to the measured values of peak *di/dt* (dots). It is apparent that there remain deviations; these correspond to errors of at most ±5 °C.

The calibration procedure is as follows. First, the device temperature is stabilized at 120 °C. Then the converter is operated at 10 A, the $v_{\rm rec}$ signal is measured, and R_4 is adjusted such that when Q_2 is OFF, $v_{\rm rec}$ is zero. Next, the power converter is operated at 2.5 A; at this low current the circuit must deliver the nominal V_T. R_8 is adjusted to deliver the required value. Finally, the converter is operated at 5, 7.5, and 10 A; at each load current, R_3 and R_{12} are adjusted to get the V_T values, as shown in Fig. 20.

VII. Experimental Results

The aim of the following experiments is to examine the effectiveness of the implemented overtemperature protection concept, on a converter in continuous operation, across a range of load currents and switching frequencies.

A. Trip Case Temperature Versus Operating Point

In a first set of experiments, the power converter is stepping down from 400 to 200 V DC. The heat plate is replaced by a passive heatsink. The protection circuit is set to trip at a junction temperature of 100 °C. The ambient temperature is 22 °C. A suite of experiments is carried out to cover load currents from 4 to 10 A, and switching frequencies[1] from 80 to 200 kHz. The results are shown in Fig. 21.

The operating points (pairs of load current and switching frequency) where the circuit trips have a grey pillar indicating the last measured temperature of the sensing via. The highest and lowest trip temperatures are highlighted with red and blue squares. The green squares without a pillar indicate the operating points where the junction temperature reaches a steady state below the threshold temperature of 100 °C.

The via is placed on the PCB close to the GaN device. However, there exists a thermal resistance between the via and the GaN device, and the PCB has thermal mass (capacitance). This creates a low-pass filter that causes the via temperature to always lag the junction temperature of the switching device.

It is observed that the lowest trip temperatures correspond to the operating points with the highest power losses (high switching frequency and high current). Here, the via temperature is around 77 °C. By contrast, the higher trip temperatures relate to operating points with lower power loss. The reason behind this is that with increasing power loss, the temperature of the sensing via increasingly lags behind that of the junction, and in fact, it is anticipated that the junction will have reached similar temperatures in all cases.

[1]It is important to distinguish between the switching frequency of the converter and the speed of its individual switching transitions. The transitions of the test circuit are inline with the state-of-the-art hard-switched GaN converters, with *dv/dt* peaking at over 100 V/ns, and *di/dt* peaking at over 10 A/ns. The high-speed components in the protection circuit are necessary to handle the high *di/dt* of these transitions and the resulting very brief output pulses from the sensor, as depicted in Fig. 19.

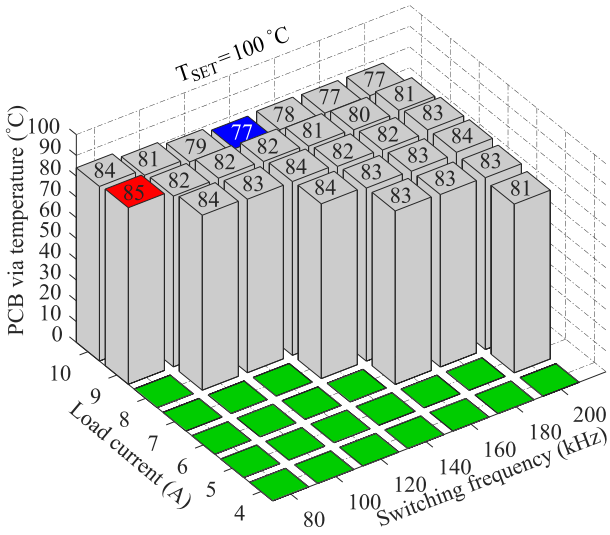

Fig. 21. Measured trip temperatures (on PCB via) against load current and switching frequency. Junction threshold temperature set to 100 °C. No heatsink fan is used.

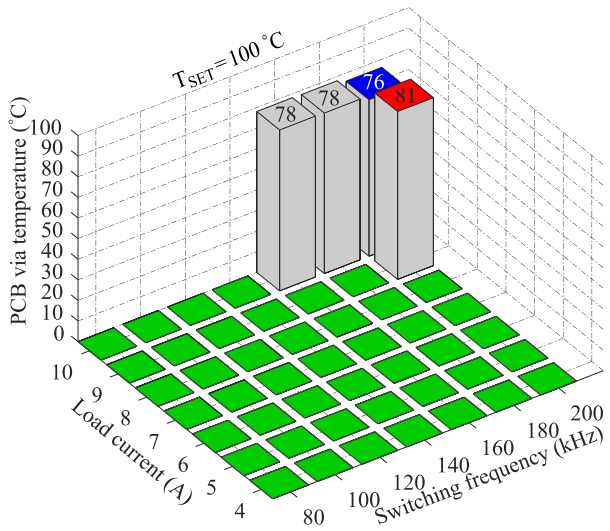

Fig. 22. Same test as Fig. 21 with heatsink fan.

The previous test is repeated with a 2 W fan on the heatsink; see Fig. 22. It can be seen that the trip temperatures remain the same; however, a larger operating range is now available.

Next, identical tests to those of Fig. 21 (without the fan) are carried out, with higher threshold temperature settings of 120 and 140 °C. The results are shown in Figs. 23 and 24, respectively. The results with a temperature setting of 140 °C indicate that the protection circuitry reported in this article allows GaN devices to operate in the steady state close to their rated limits of 150 °C.

Self-heating of the device die results in heterogeneous temperature distribution and may create hot spots on the die [32], [33]. This should be considered during the design; and if the device is

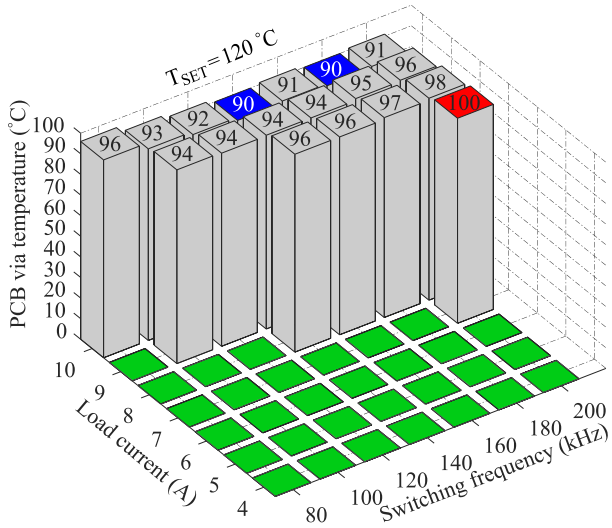

Fig. 23. Measured trip temperatures against load current and switching frequency, for a junction threshold temperature setting of 120 °C (no fan).

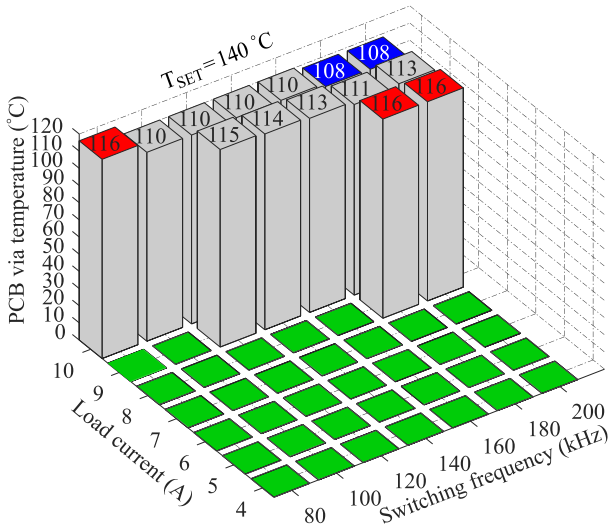

Fig. 24. Measured trip temperatures against load current and switching frequency, for a junction threshold temperature setting of 140 °C (no fan).

operating close to the specified maximum temperature, a safety margin needs to be taken into consideration. This is not peculiar to the presented method and applies to other overtemperature protection concepts if the trip level is set close to the device operating temperature limit.

B. Junction Temperature Sensing Response Time

The aim of this study is to evaluate the response time of the protection circuit. With a switching frequency of 500 kHz and load current of 10 A, the power losses are increased to well over twice the value that would cause the temperature protection to trip in the steady state. The measured response time until the converter is shut down by the overtemperature protection circuit, for a starting temperature of 22 °C, is shown in Fig. 25. The protection circuit is set to shut the power converter down at 120 °C.

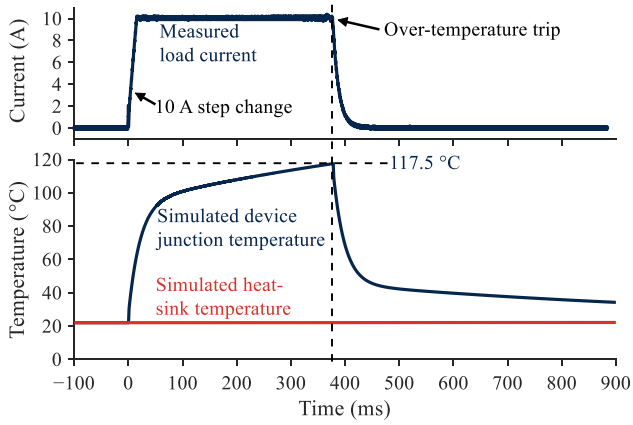

Fig. 25. Demonstration of safe shutdown on highly overloaded GaN bridge-leg power converter operating at 10 A, 2 kW, and 500 kHz. The high switching losses at 500 kHz result in rapid heating of the GaN devices.

In addition, the simulated junction and heat sink temperature is shown, derived from an experimentally calibrated thermal model. It can be observed that the protection circuit deactivates the circuit when the simulated junction temperature reaches 117.5 °C. This confirms that 1 ms is a reasonable sample rate, and that even with this high rate of switching loss, the sensing and protection method is fast enough to protect the devices.

C. Discussion of Protection Circuit Performance and Tradeoffs

A particular benefit of temperature sensing directly at the device junction is the very fast response time in situations of rapid device heating such as that shown in Fig. 25. Here, it is seen that the heatsink temperature does not change, due to its large thermal capacity. Hence, monitoring the heatsink temperature does not give any information about the device temperature. Mounting a sensor on the PCB close to the power device (which in itself is challenging without compromising the power-circuit layout) would also be response-time limited by the thermal capacities of the PCB and temperature sensor.

One tradeoff necessary to deliver this quick response is a protection-circuit power consumption of around 2 W, mainly due to the relatively high quiescent current of the isolated dc–dc converter, wideband op-amps, and high-speed comparators employed. For a kW-scale converter operating at maximum load, such power consumption would have minimal impact on overall system efficiency. However, for a system with a broad range of loading conditions, the power consumption of the protection circuit could adversely affect efficiency with light loads. However, in such situations, it may be acceptable to exploit the fact that light loading corresponds to lower losses in the power devices, making it unnecessary to monitor their temperature. The protection circuit could, therefore, be disabled under light-load conditions.

VIII. Conclusion

A temperature-sensing and overtemperature protection method for hard-switched GaN devices, using a noncontact

di/dt sensor, has been implemented and validated. The circuit peak-detects a GaN device's di_s */dt* signal and based on that determines if the junction temperature has risen above a preset limit, in which case the converter is shut down. The threshold of the peak *di/dt* comparator circuit is automatically adjusted as a function of load current, in order to maintain a constant trip-temperature.

Before operation in the running converter, the circuit must be calibrated to account for device parameters and circuit parasitics. Further work is to identify ways in which the calibration procedure could be simplified, automated, or obviated.

Since the protection circuit directly measures a parameter that is sensitive to die junction temperature, it can detect the overtemperature very quickly ($\sim$1 ms), especially compared to a "direct" sensor such as a thermistor that for discrete devices would inevitably have to be mounted outside the device case. The system is demonstrated to safely trip a 2 kW, mains-voltage GaN converter even under extreme conditions. Trip temperature tolerances are shown to be of the order of $\pm$5 °C. The concept uses a sensor that can be implemented with low-cost two-layer PCB technology, whilst the overtemperature protection circuit is implemented in analogue circuitry with low cost with respect to the cost of a kW-scale power converter. The design and calibration procedure described here enables engineers to adopt the concept in a variety of GaN-based power converters.

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