Overview on ESD Protection Designs of Low-Parasitic Capacitance for RF ICs in CMOS Technologies

Ming-Dou Ker, *Fellow, IEEE*, Chun-Yu Lin, *Member, IEEE*, and Yuan-Wen Hsiao, *Member, IEEE*

***Abstract*—CMOS technology has been widely used to implement radio-frequency integrated circuits (RF ICs). However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of RF ICs. Therefore, on-chip ESD protection designs must be added at all input/output pads in RF circuits against ESD damages. To minimize the impacts from ESD protection circuit on RF performances, ESD protection circuit at input/output pads must be carefully designed. An overview on ESD protection designs with low parasitic capacitance for RF circuits in CMOS technology is presented in this paper. The comparisons among these ESD protection designs are also discussed. With the reduced parasitic capacitance, ESD protection circuit can be easily combined or co-designed with RF circuits. As the operating frequencies of RF circuits increase, on-chip ESD protection designs for RF applications will continuously be an important design task.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuits, low capacitance, radio-frequency integrated circuit (RF IC).**

I. Introduction

RADIO-FREQUENCY integrated circuits (RF ICs) have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production. Electrostatic discharge (ESD), which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all ICs, including the RF front-end circuits [1]. In the RF front-end circuits, the input/output (I/O) pads are usually connected to the gate terminal or silicided drain/source terminal of the metal-oxide-semiconductor field-effect transistor (MOSFET), which leads to a very low ESD robustness if no appropriate ESD protection design is applied. Once the RF front-end circuit is damaged by ESD, it cannot be recovered and the RF functionality is lost. Therefore, on-chip ESD protection design must be provided for all I/O pads in RF ICs.

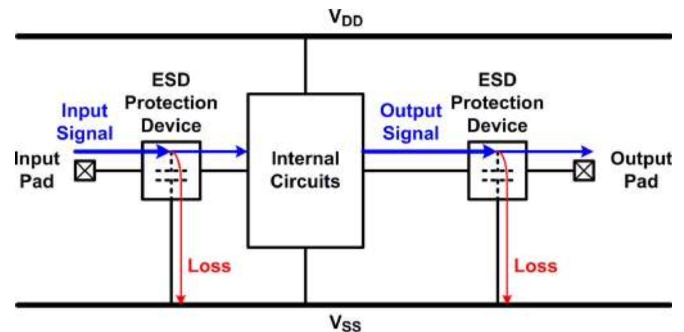

Fig. 1. Signal loss at input and output pads of IC with ESD protection devices.

However, ESD protection devices cause RF performance degradation with several undesired effects [2]–[5]. Parasitic capacitance is one of the most important design considerations for RF ICs. Conventional ESD protection devices with large dimensions have the parasitic capacitance which is too large to be tolerated for RF front-end circuits. As shown in Fig. 1, the parasitic capacitance of ESD protection devices causes signal loss from the pad to ground. Moreover, the parasitic capacitance also changes the input matching condition. Consequently, RF performance is deteriorated.

To mitigate the performance degradation caused by ESD protection devices, some design techniques had been developed to reduce the parasitic capacitance of ESD protection devices. The ESD protection circuit with reduced parasitic capacitance can be easily combined or co-designed with RF circuits [6]–[8]. In this paper, the RF ESD protection designs with low parasitic capacitance in CMOS processes are reviewed.

II. Design Consideration for ESD Protection

To achieve effective ESD protection, the voltage across the ESD protection device during ESD stresses should be carefully designed [9]–[12]. Fig. 2 shows the ESD design window of an IC, which is defined by the power supply voltage $(\mathrm{V_{DD}})$ of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage $(\mathrm{V_{BD}})$ of MOSFET. First, the trigger voltage (V_{t1}) and holding voltage (V_{h}) of ESD protection device must be lower than the gate-oxide breakdown voltage of MOSFET to prevent the internal circuits from damage before the ESD protection device is turned on during ESD

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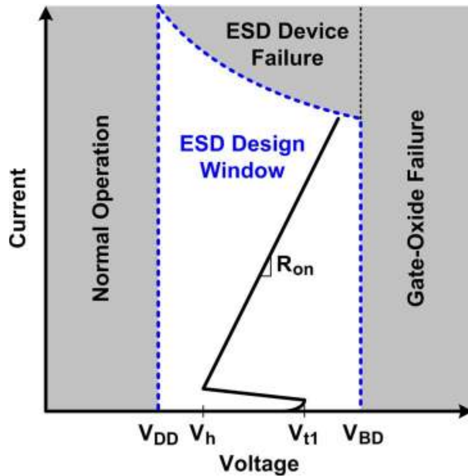

Fig. 2. ESD design window defined by the power supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of the MOSFET.

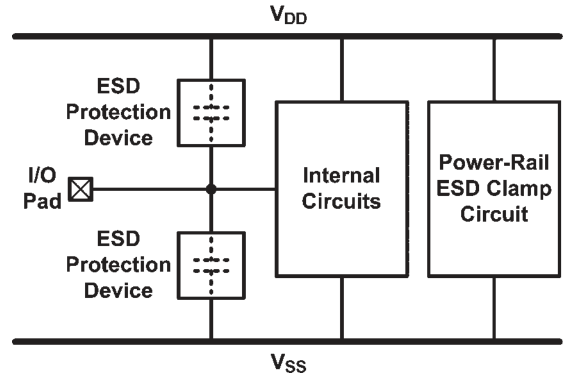

Fig. 3. Conventional ESD protection scheme.

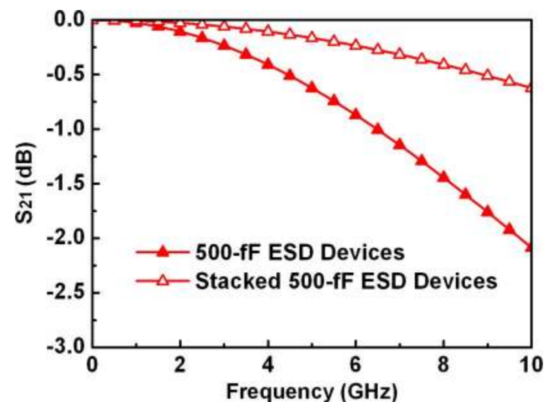

Fig. 4. Simulated S_{21}-parameters of conventional ESD protection scheme with 500-fF ESD devices, and ESD protection scheme with stacked 500-fF ESD devices (equivalent to 250 fF).

stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power supply voltage of the IC to prevent the ESD protection devices from being mistriggered under normal circuit operating conditions. Moreover, the turn-on resistance (R_{on}) of ESD protection device should be minimized to reduce the joule heat generated in the ESD protection device and the clamping voltage of the ESD protection device during ESD stresses. As CMOS technology is continuously scaled down, the power supply voltage is decreased and the gate oxide becomes thinner, which leads to reduced gate-oxide breakdown voltage of MOSFET. Typically, the gate-oxide breakdown voltage is decreased to only ~5 V in a 65-nm CMOS process with gate-oxide thickness of ~20 Å [13]. As a result, the ESD design window becomes much narrower in nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharging paths in time.

III. Solutions to RF ESD Protection Designs

A. Conventional ESD Protection Circuit

The conventional on-chip ESD protection scheme is shown in Fig. 3, where two ESD protection devices at I/O pad are assisted with the power-rail ESD clamp circuit to prevent internal circuits from ESD damage [7], [14], [15]. In Fig. 3, the ESD protection devices at I/O pad can be realized with STI diodes [14], poly diodes [15], silicon-controlled rectifier (SCR) devices [7], or other low-capacitance ESD protection devices. Fig. 4 shows the simulated insertion loss (S_{21}-parameter) of the conventional ESD protection scheme with 500-fF capacitance.

However, this scheme is only suitable for small ESD protection devices because the parasitic capacitance of the ESD protection device is directly contributed at the I/O pad. The device dimensions of ESD protection devices should be decreased to reduce the parasitic capacitance at I/O pad, which in turn reduces RF performance degradation caused by the parasitic capacitances of the ESD protection devices. However, ESD robustness needs to be maintained, so the minimum device dimensions of ESD protection devices cannot be shrunk unlimitedly.

B. Stacked ESD Protection Devices

In order to reduce the parasitic capacitance from ESD protection devices without sacrificing ESD robustness, the ESD protection devices in stacked configuration had been presented, as shown in Fig. 5 [16], [17]. With two stacked ESD protection devices, the overall equivalent parasitic capacitance theoretically becomes $C_{ESD}/2$, where C_{ESD} is the parasitic capacitance of each ESD protection device. The simulated S_{21}-parameters of the stacked ESD protection devices are also shown in Fig. 4. More stacked ESD devices lead to more significant parasitic capacitance reduction. Besides reducing parasitic capacitance, using stacked configuration can also reduce the leakage current of ESD protection devices under normal circuit operating conditions. Although stacked ESD protection devices can reduce the parasitic capacitance and leakage current, this technique is adverse to ESD protection because the overall turn-on resistance and the clamping voltage of the stacked ESD protection devices during ESD stresses are increased as well.

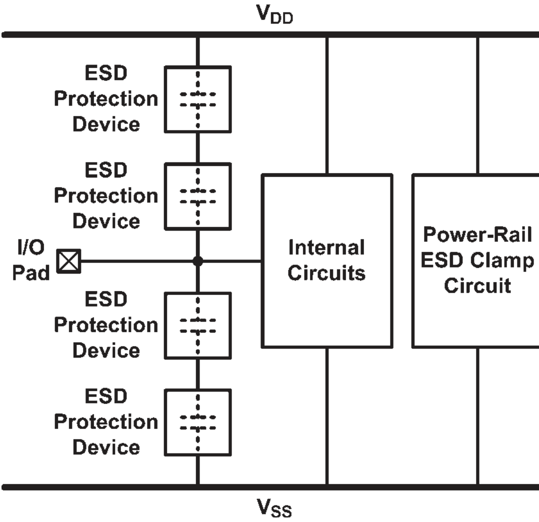

Fig. 5. Stacked ESD protection devices to reduce the parasitic capacitance.

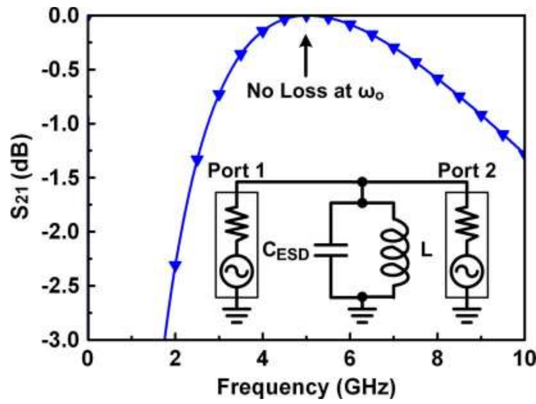

Fig. 6. Ideal parallel *LC* resonator and the simulated S_{21}-parameters under different frequencies.

C. Parallel LC Resonator

The technique of using parallel *LC* resonator to reduce equivalent parasitic capacitance is also called the impedance cancellation. In such a resonator, the resonant frequency (ω_o) is

$$\omega_o = \frac{1}{\sqrt{LC_{\mathrm{ESD}}}} \tag{1}$$

where L and C_{ESD} denote the added parallel inductance and parasitic capacitance of ESD protection device, respectively. An ideal parallel *LC* resonator and the simulated S_{21}-parameters under different frequencies are shown in Fig. 6. The signal loss at the resonant frequency is ideally zero, which means that the equivalent capacitance at the resonant frequency is zero. With the parallel *LC* network resonating at the operating frequency, the shunt impedance of the resonator becomes very large, which can effectively suppress signal loss. Therefore, the ESD protection design using parallel *LC* resonator can mitigate the impacts on RF performances for circuits operating in a narrow frequency band. Based on this concept, the on-chip spiral inductor had been designed to resonate with the parasitic capacitance of ESD protection devices [18], [19]. Furthermore, the inductor cannot only resonate with the parasitic capacitance of the ESD protection device but also serve as an ESD protection device by itself. In this configuration, the parallel *LC* resonator can be realized as shown in Fig. 7. The inductor (L_{ESD}) serves as an ESD protection device between I/O pad and V_{DD}, while the capacitive ESD protection device provides ESD current path between I/O pad and V_{SS}. The inductor and the parasitic capacitance of the ESD protection device are designed to resonate at the operating frequency of the RF front-end circuit to minimize performance degradation caused by the ESD protection device. With an inductor directly connected between the I/O pad and V_{DD}, the ESD protection device is reverse-biased with the largest possible dc voltage under normal circuit operating conditions, which leads to the minimum the parasitic p-n junction capacitance in the ESD protection device. The placement of the inductor and the ESD protection device can be interchanged to provide the same function. Since the inductor is dc short, a dc blocking capacitor (C_{block}) is required to provide a separated dc bias for the internal circuits.

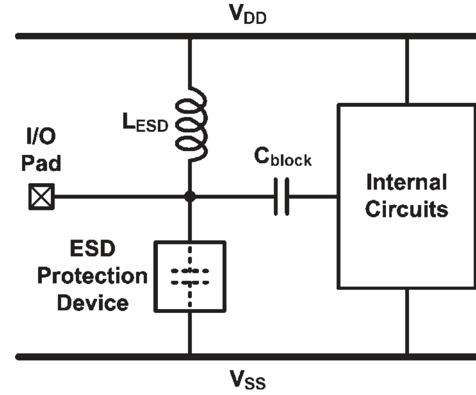

Fig. 7. ESD protection design with the parallel *LC* resonator, where the inductor L_{ESD} provides ESD current path between V_{DD} and the I/O pad.

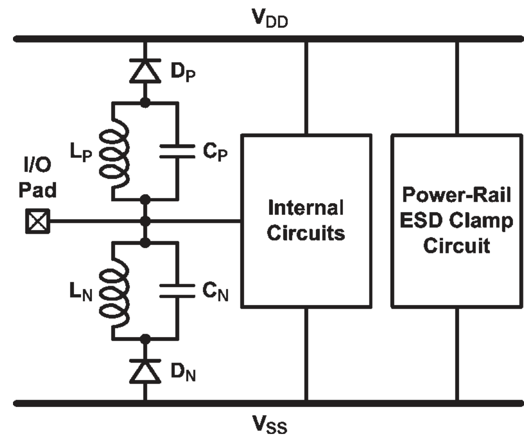

Fig. 8. ESD protection design with *LC* tanks.

D. LC Tank

LC tank has been reported for low-capacitance ESD protection design, which consists of an inductor, a capacitor, and an ESD diode [20]–[22]. As shown in Fig. 8, a pair of the *LC* tanks is placed at the I/O pad. One *LC* tank consists of

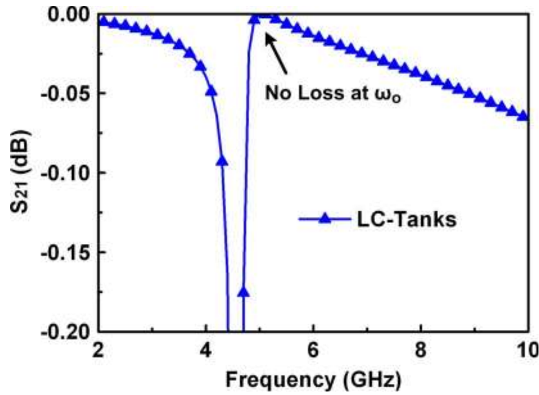

Fig. 9. Simulated S_{21}-parameters of ESD protection scheme with *LC* tanks.

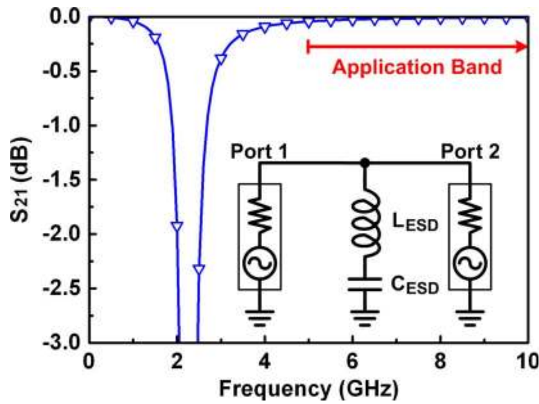

Fig. 10. Ideal series *LC* resonator and the simulated S_{21}-parameters under different frequencies.

the inductor L_P and the capacitor C_P is placed between the I/O pad and ESD diode D_P. Another *LC* tank consists of the inductor L_N and the capacitor C_N is placed between the I/O pad and ESD diode D_N. The ESD diodes D_P and D_N are used to block the steady leakage current path from V_{DD} to V_{SS} under normal circuit operating conditions. Furthermore, the capacitors C_P and C_N can also be realized by ESD protection devices. The simulated S_{21}-parameters of the *LC* tanks are shown in Fig. 9. At the resonant frequency of the *LC* tank, there is ideally infinite impedance from the signal path to the ESD diode. Consequently, the parasitic capacitances of the ESD protection devices are isolated, which can mitigate the parasitic effects from the ESD protection devices. To further reduce the parasitic capacitance from the ESD protection devices, two or more *LC* tanks can be stacked to provide better impedance isolation at resonant frequency, and the impacts of the ESD protection devices can be significantly reduced.

E. Series LC Resonator

For the wideband RF front-end circuits, the series *LC* resonator can be used for ESD protection. The simulated S_{21}-parameter of an ideal series *LC* resonator under different frequencies is shown in Fig. 10. With series inductance (L_{ESD}) and capacitance (C_{ESD}), the resonant frequency (ω_o) is identical to that shown in (1). There is a notch at the resonant frequency where the signal loss is very large, and the signal is totally lost. However, at frequencies above the resonant frequency, the inductor dominates the magnitude of impedance. Therefore, the magnitude of impedance increases to reduce the signal loss significantly. Thus, wideband ESD protection can be achieved by designing the application band of the series *LC* resonator to cover the frequency band of the RF signal. During ESD stresses, the ESD current can be discharged through the inductor and the ESD protection device. ESD protection design utilizing the series *LC* resonator is shown in Fig. 11, where a pair of the series *LC* resonators is placed at the I/O pad [23]. ESD current paths from the I/O pad to both V_{DD} and V_{SS} are provided by the inductors and the series ESD protection devices.

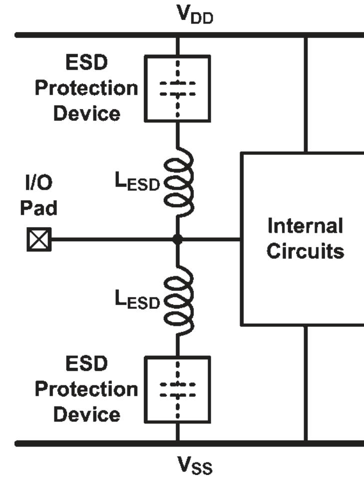

Fig. 11. ESD protection design with the series *LC* resonator.

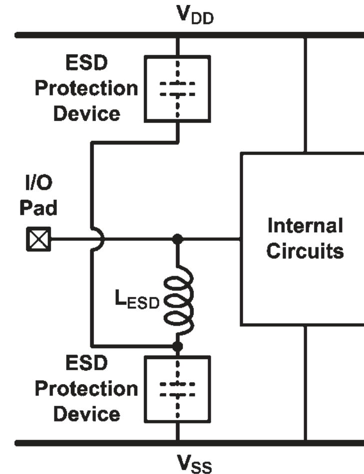

Fig. 12. ESD protection design with modified series *LC* resonator, where only one inductor is connected in series with two ESD protection devices.

To reduce the inductors used in the series *LC* resonators, a modified design using only one inductor is shown in Fig. 12 [18]. One inductor is connected in series with two ESD protection devices connected to V_{DD} and V_{SS}, respectively. Because the capacitance in the series *LC* resonator is the sum of the parasitic capacitances of these two ESD protection devices, the inductance used in Fig. 12 is smaller than that used in Fig. 11 under the same resonant frequency. Consequently, total cost can be reduced in this modified design.

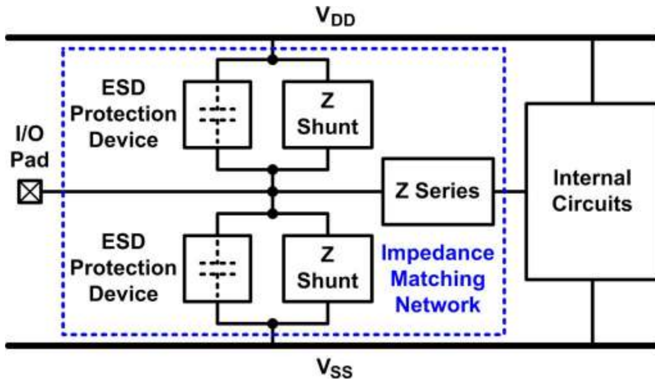

Fig. 13. ESD protection design with impedance matching by using shunt and series components.

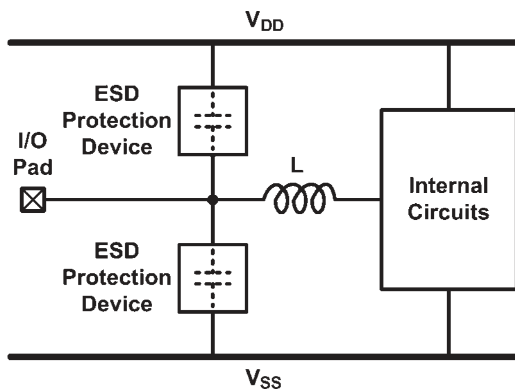

Fig. 14. Example of ESD protection design with impedance matching.

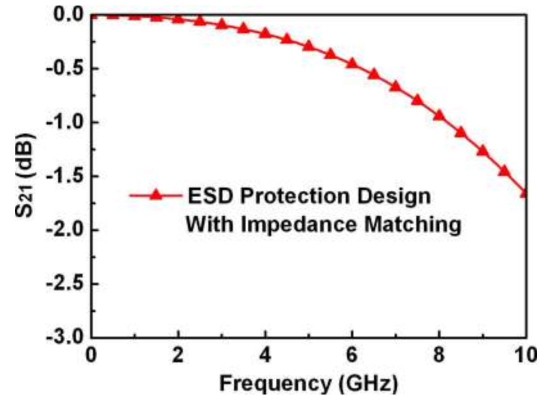

Fig. 15. Simulation results of ESD protection design with impedance matching.

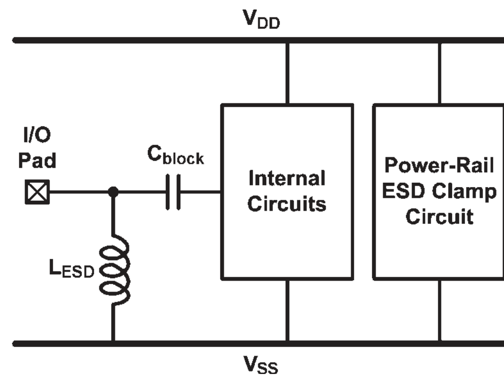

Fig. 16. Inductive ESD protection design.

F. Impedance Matching

To achieve satisfactory ESD robustness, the size of ESD protection devices must be large enough. However, parasitic effects increase with the dimensions of ESD protection devices. To solve this dilemma, ESD protection devices can be treated as a part of the impedance matching network at the I/O pad. By co-designing the ESD protection circuit and the impedance matching network, large ESD protection devices can be used to achieve high ESD robustness without sacrificing RF performance [24]. The impedance matching technique of ESD protection device had been proposed. Fig. 13 illustrates the idea of matching the parasitic effects of ESD protection devices [25]. In this configuration, ESD current can be discharged from the I/O pad through the ESD protection devices to $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$. The combined impedance of the shunt and series impedance is designed to provide impedance matching at the I/O pad with ESD protection. The shunt and series impedance can be realized by various components.

One example of ESD protection design with impedance matching technique is shown in Fig. 14 [26], which uses inductance to match the parasitic capacitances of ESD protection devices. The ESD protection devices are placed next to the I/O pad, and provide ESD protection for the internal circuits. The inductive component L, which can be an inductor or a transmission line, is connected in series with the signal line, and matches the parasitic capacitances of the ESD protection devices. The design goal is to neutralize the capacitance of ESD protection devices at the operating frequency by using the inductance of L. The simulated $\mathrm{S_{21}}$-parameters of the ESD protection design with impedance matching are shown in Fig. 15.

G. Inductive ESD Protection

ESD protection design for RF circuits by using inductor as the ESD protection device had been reported. In Fig. 16, the ESD protection inductor $(\mathrm{L_{ESD}})$ is placed between the input pad and $\mathrm{V_{SS}}$ [27]–[30]. The simulated $\mathrm{S_{21}}$-parameters of the inductive ESD protection under different frequencies are shown in Fig. 17. Inductors exhibits higher impedance at higher frequencies. Since the frequency component of ESD is much lower than that of the RF signal, the inductor can pass the ESD current while block the RF signal. To efficiently sink the ESD current, the metal width of the ESD protection inductor should be wide enough to enhance the current handling capability and to reduce the parasitic series resistance. However, inductors realized very wide metal traces occupy large chip area. This is the main design concern in the inductor-based ESD protection. Besides, a dc blocking capacitor $(\mathrm{C_{block}})$ is needed in this design to provide a separated dc bias for the internal circuits.

Another inductor-based ESD protection design is shown in Fig. 18 [31]. The ESD protection inductor can be merged with the gate inductor to save the chip area since the typical low-noise amplifier (LNA) needs a gate inductor connected between the input pad and the gate terminal of the input MOS transistor.

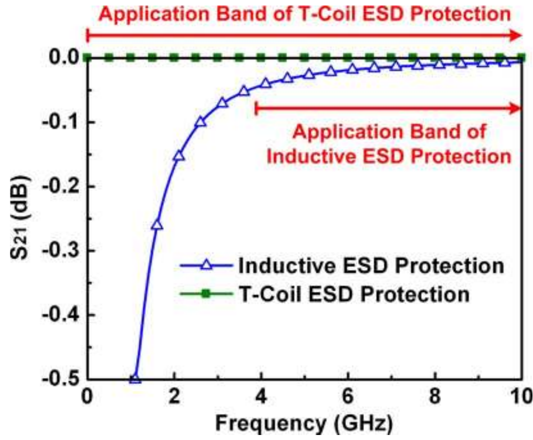

Fig. 17. Simulation results of inductive ESD protection and T-coil-based ESD protection.

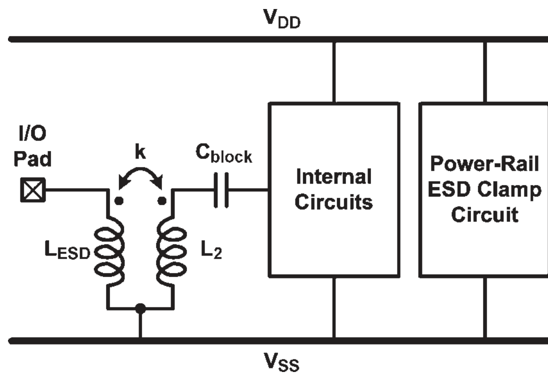

Fig. 18. Inductive ESD protection design with transformer.

The ESD protection inductor is placed under the gate inductor to form a transformer. Consequently, the transformer-based ESD protection design provides not only the gate inductor in the impedance matching network but also the ESD protection for the input pad.

H. T-Coil

The ESD protection design with T-coil for wideband applications had been reported. As shown in Fig. 19, with proper impedance matching design, this circuit can provide a purely resistive input impedance of R_T [32]. Once the following expressions hold, the input impedance Z_{in} remains resistive at all frequencies

$$L_{ESD} = L_2 = \frac{C_{ESD} R_T^2}{4}\left(1 + \frac{1}{4\zeta^2}\right) \tag{2}$$

$$C_B = \frac{C_{ESD}}{16\zeta^2} \tag{3}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{4}$$

where ζ is the damping factor of the network transfer function V_X/I_{in}. With proper design, large ESD protection devices can be used without degrading RF performance. The NMOS and PMOS transistors with gate-coupled technique are used in the first ESD protection design with T-coil [32]. The SCR has also been used as the ESD protection device in the T-coil-based ESD protection design for a high-speed transmitter [33]. The return loss of the transmitter was improved with the T-coil which compensated the parasitic effects of the SCR.

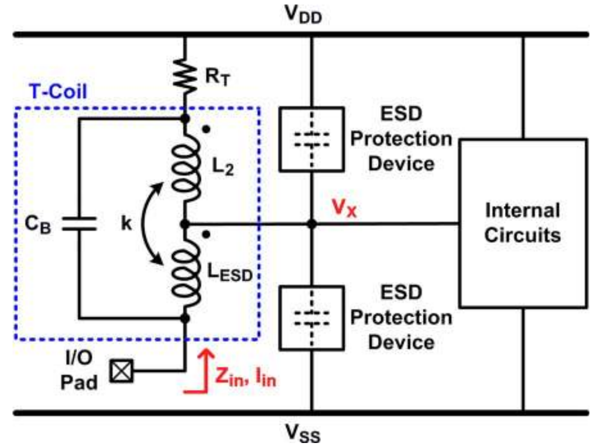

Fig. 19. ESD protection design with T-coil.

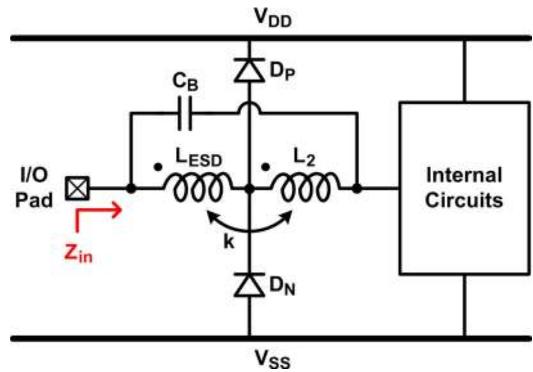

Fig. 20. ESD protection with T-diode.

The simulated S_{21}-parameters of the T-coil-based ESD protection under different frequencies are also shown in Fig. 17. Since the T-coil-based ESD protection design can overcome the band-limiting problems in the narrowband ESD protection circuits, they are suitable for wideband RF front-end circuits. However, the design concern for the T-coil-based ESD protection is the inductor L_{ESD} which must be realized by wide metal trace and in turn occupies large chip area.

Another wideband LNA with the transformer plus diode (T-diode) had been reported, as shown in Fig. 20 [34]. This is another T-coil-based ESD protection design. In this design, the capacitor C_B in the T-diode can be realized with the parasitic capacitance between the inductors L_{ESD} and L_2.

I. Distributed ESD Protection

The π-model ESD protection scheme had been presented to achieve wideband impedance matching with ESD protection devices. The ESD protection devices are divided into two sections and are impedance matched by the transmission line or inductor, as shown in Fig. 21 [35], [36].

Another distributed ESD protection scheme had been presented, as shown in Fig. 22 [37]. With the ESD protection devices divided into small sections and matched by the transmission lines, such a distributed ESD protection scheme can

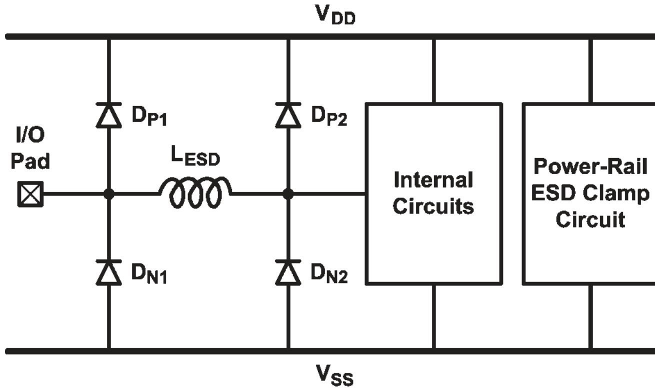

Fig. 21. π-model ESD protection scheme.

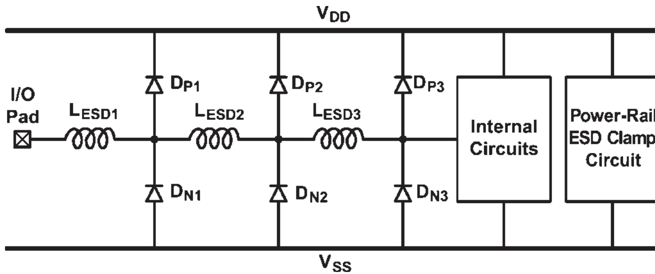

Fig. 22. Distributed ESD protection scheme with equal-size ESD diodes.

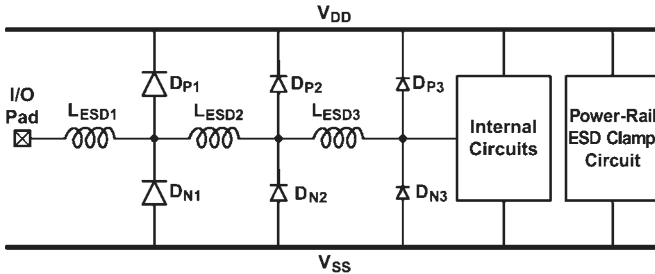

Fig. 23. Distributed ESD protection scheme with decreasing-size ESD diodes.

achieve wideband impedance matching. The number of ESD protection devices can be varied to optimize the performance. In Fig. 22, the ESD protection diodes are equally divided into three sections. However, most of ESD current is expected to flow through the first section which is closest to the I/O pad. To improve ESD robustness of distributed ESD protection scheme, the modified design of the decreasing-size distributed ESD protection scheme had been reported. The decreasing-size distributed ESD protection scheme is shown in Fig. 23, which allocates the ESD protection devices with decreasing sizes from the I/O pad to the internal circuit [38]. With larger ESD protection devices close to the I/O pad, ESD robustness is improved. It had also been verified that good wideband impedance matching is still maintained in this ESD protection scheme. The simulated S_{21}-parameters of the π-model ESD protection scheme and distributed ESD protection scheme with equal-size ESD diodes are compared in Fig. 24.

Recently, the distributed ESD protection scheme has been reported to protect 60-GHz broadband RF circuits [39]. Fig. 25 shows the measurement results on the S_{11}- and S_{21}-parameters of this distributed ESD protection circuit. This ESD protection

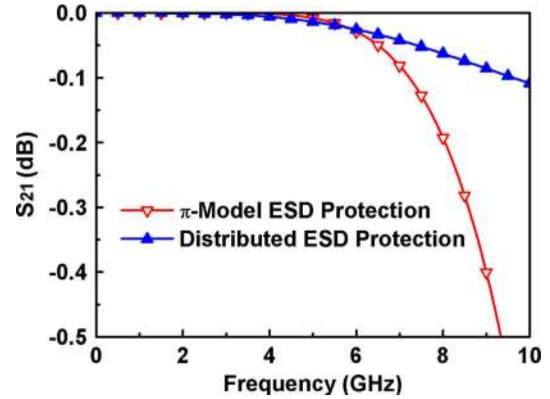

Fig. 24. Simulation results of π-model ESD protection scheme and distributed ESD protection scheme with equal-size ESD diodes.

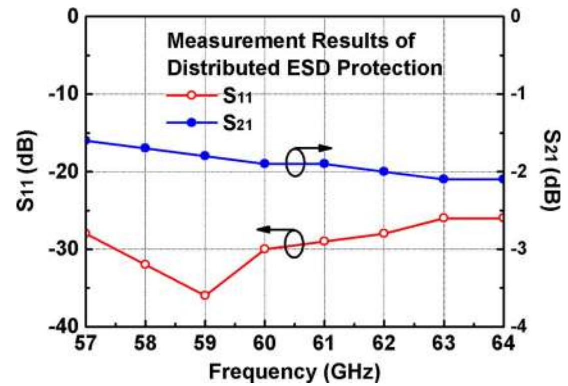

Fig. 25. Measurement results of distributed ESD protection scheme with decreasing-size ESD diodes on S_{11}- and S_{21}-parameters.

circuit passes 2-kV human body model (HBM) ESD test with only 2-dB insertion loss in 60-GHz band.

IV. Discussion and Comparison

The reported ESD protection designs for RF circuits have been reviewed in previous section. The comparison among various ESD protection designs for RF front-end circuits is summarized in Table I. The evaluated parameters are explained as following.

- Suggested Operating Frequencies:

  Each ESD protection circuit is suggested to be used in different frequencies, such as < 5 GHz, < 10 GHz, or > 5 GHz. Some of the ESD protection circuits can only be used in a specific narrow band.

- Design Complexity:
  - "Low": The stand-alone ESD protection device is the ESD protection circuit without extra inductive component.
  - "Moderate": The stand-alone ESD protection device is the ESD protection circuit without extra inductive component, but the layout of the ESD protection device needs careful consideration.
  - "High": Besides the ESD protection device, extra inductive components are needed, and the auxiliary components should be carefully designed.

TABLE I
COMPARISON AMONG ESD PROTECTION DESIGNS FOR RF CIRCUITS

ESD Protection Design	Suggested Operating Frequencies	Design Complexity	Equivalent Parasitic Capacitance	Signal Loss	Clamping Voltage at Internal Circuits	HBM / CDM Robustness	Area Efficiency
A. Conventional ESD Protection Circuit	< 5 GHz	Low	Dozens ~ Hundreds of fF	Worst at High Frequency	1 R_{ESD}	Better / Better	Good
B. Stacked ESD Protection Devices	< 10 GHz	Moderate	Dozens ~ Hundreds of fF	Worse at High Frequency	2 R_{ESD}	Good / Good	Good
C. Parallel LC Resonator	> 5 GHz (Narrow Band)	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD}	Better / Better	Poor
D. LC-Tank	> 5 GHz (Narrow Band)	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD} + 1 L_{ESD}	Good / Poor	Poor
E. Series LC Resonator	> 5 GHz	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD} + 1 L_{ESD}	Good / Poor	Poor
F. Impedance Matching	> 5 GHz	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD}	Better / Better	Poor
G. Inductive ESD Protection	> 5 GHz	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 L_{ESD}	Better / Poor	Poor
H. T-Coil	> 5 GHz	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD}	Better / Better	Poor
I. Distributed ESD Protection	> 5 GHz	High	~ 0 at Designed Frequency	~ 0 at Designed Frequency	1 R_{ESD}	Better / Better	Poor

- Equivalent Parasitic Capacitance:
  - "$\sim$0 at Designed Frequency": The equivalent parasitic capacitance of the ESD protection circuit at the I/O pad can be very small with proper design.
  - "Dozens $\sim$ Hundreds of fF": The equivalent parasitic capacitance of the ESD protection circuit at the I/O pad is about dozens of fF or hundreds of fF, according to the used ESD protection devices and fabrication processes.
- Signal Loss:
  - "$\sim$0 at Designed Frequency": The simulated S_{21}-parameters of the ESD protection circuit closed to 0 dB at its operating frequencies.
  - "Worse at High Frequency": The simulated S_{21}-parameters of the ESD protection circuit are worse at high frequency.
  - "Worst at High Frequency": The simulated S_{21}-parameters of the ESD protection circuit are distant from 0 dB at high frequency.
- Clamping Voltage at Internal Circuits:
  - "R_{ESD}": The clamping voltage seen at the internal circuits under ESD stress consists of the clamping voltage of one resistive/capacitive ESD protection device.
  - "L_{ESD}": The clamping voltage seen at the internal circuits under ESD stress consists of the clamping voltage of one inductive ESD protection device.
- HBM / CDM Robustness:
  - "Poor": The HBM or charged device model (CDM) ESD robustness is poor due to the higher clamping voltage at internal circuits.
  - "Good": The HBM or CDM ESD robustness is good due to the moderate clamping voltage at internal circuits.
  - "Better": The HBM or CDM ESD robustness is better due to the lower clamping voltage at internal circuits.
- Area Efficiency:
  - "Poor": The area efficiency of the ESD protection design is poor.
  - "Good": The area efficiency of the ESD protection design is good.

The different RF front-end circuits have different requirements on operating frequency, matching, noise, and other specifications for the designs. The comparison of suggested operating frequencies, design complexity, equivalent parasitic capacitance, signal loss, clamping voltage at internal circuits, HBM/CDM robustness, and area efficiency among various ESD protection designs in Table I can provide the useful information for RF circuit designers to apply ESD protection solution to their RF circuits.

The figure of merit used to compare the RF performance and ESD robustness is (signal loss) $\times$ (clamping voltage at internal circuits). With the lower signal loss and clamping voltage at internal circuits, the ESD protection design will be more suitable for RF circuits. The conventional ESD protection circuit

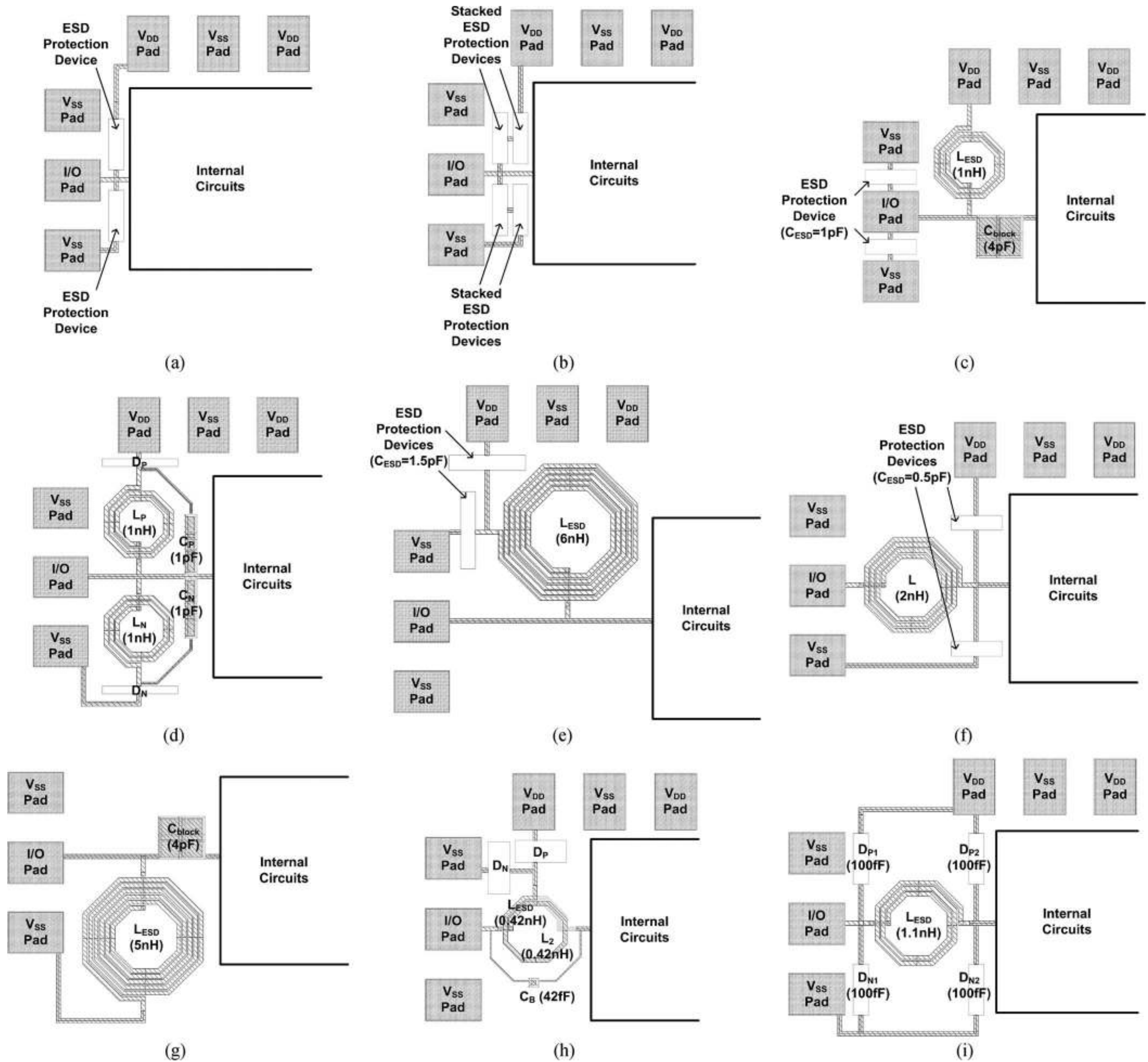

Fig. 26. Sample layout of (a) conventional ESD protection circuit (Fig. 3), (b) stacked ESD protection devices (Fig. 5), (c) parallel *LC* resonator (Fig. 7), (d) LC tank (Fig. 8), (e) series *LC* resonator (Fig. 12), (f) impedance matching (Fig. 14), (g) inductive ESD protection (Fig. 16), (h) T-coil (Fig. 20), and (i) distributed ESD protection (Fig. 21).

or stacked ESD protection devices may be suitable for some RF circuits operated with lower frequencies. As the operating frequencies of RF front-end circuits increase, on-chip ESD protection designs with extra inductive components are needed. According to Table I, the reported ESD protection designs with additional components can lower the equivalent parasitic capacitance and signal loss at the I/O pad and mitigate the impacts caused by the ESD protection circuit. By utilizing the proper design, the ESD protection device can be realized with large device dimensions to achieve good ESD robustness because the parasitic capacitance from the ESD protection device can be compensated or cancelled. By using the scheme of parallel *LC* resonator, impedance matching, T-coil, or distributed ESD protection, the internal circuits can be clamped to the clamping voltage of one resistive/capacitive ESD protection device. The inductive ESD protection will clamp the internal circuits to the clamping voltage of one inductor. The *LC* tank and series *LC* resonator exist higher clamping voltage, since the ESD current paths consist of one inductor and one resistive/capacitive ESD protection device. With the lower clamping voltage at internal circuits, the ESD protection design performed better ESD robustness, particularly in nanoscale CMOS processes with thinner gate oxide. It should be noted that the inductor has large voltage overshoots during the CDM ESD stress, which typically has a fast rise time of < 1 ns [40]. Therefore, the *LC* tank, series *LC* resonator, and inductive ESD protection must be

carefully selected to prevent from the large voltage overshoots during CDM ESD stress. Besides, ESD protection designs with extra inductive components substantially increase the chip area, so the area efficiency of the schemes C ∼ I in Table I are all poor. The fabrication costs also raise as the chip area increase.

In nanoscale CMOS technology, the thinner gate oxide and the silicided drain/source terminal seriously degrade the ESD robustness of RF circuits. The clamping voltage across the RF circuits under ESD stress must be reduced to improve ESD robustness of the RF circuits. Therefore, the ESD current path of ESD protection circuit must be shortened. Among the ESD protection schemes in the literature, the conventional ESD protection circuit [14], impedance matching [24], inductive ESD protection [27], [29], [31], T-Coil [33], [34], and distributed ESD protection [39] with lower clamping voltage have been verified in sub-100 nm CMOS processes with oxide thickness of < 20 Å. Besides, the series *LC* resonator [23], inductive ESD protection [27], and distributed ESD protection [39] have been designed to operate with frequencies > 20 GHz. Therefore, some ESD protection designs, such as inductive ESD protection and distributed ESD protection, are still useful for RF circuits fabricated in advanced CMOS processes and operating at higher frequencies in the future.

V. Layout Examples of RF ESD Protection Devices

With various conditions, such as different ESD protection devices, inductors, capacitors, pad styles, operating frequencies, and fabrication processes, the layout style of every RF ESD protection scheme should be different. In this section, the sample layout of every RF ESD protection circuit operating at 5 GHz is provided in Fig. 26(a)–(i). The used resistive/capacitive ESD protection devices are STI diodes, and the other used devices include spiral inductors and metal-insulator-metal capacitors. The circuits are arranged with the pad style of ground-signal-ground and power-ground-power.

Fig. 26(a)–(i) show the sample layout of the conventional ESD protection circuit (Fig. 3), stacked ESD protection devices (Fig. 5), parallel *LC* resonator (Fig. 7), *LC* tank (Fig. 8), modified series *LC* resonator (Fig. 12), impedance matching (Fig. 14), inductive ESD protection (Fig. 16), T-diode (Fig. 20), and π-model ESD protection (Fig. 21), respectively. In Fig. 26(c), the $\mathrm{L_{ESD}}$ and $\mathrm{C_{ESD}}$ used in parallel *LC* resonator are 1 nH and 1 pF, respectively; therefore, the resonant frequency is ∼5 GHz. In Fig. 26(d), the L_P and C_P (L_N and C_N) used in LC tank are also 1 nH and 1 pF, respectively, to resonate at ∼5 GHz, so the parasitic effects of diodes (D_P and D_N) are isolated at ∼5 GHz. In Fig. 26(e), the larger $\mathrm{L_{ESD}}$ (6 nH) and $\mathrm{C_{ESD}}$ (1.5 pF) are used in modified series LC resonator to resonate at < 2 GHz, and the application band covers 5 GHz. In Fig. 26(g), the large $\mathrm{L_{ESD}}$ (5 nH) is also needed in inductive ESD protection to behave high impedance at 5 GHz. In Fig. 26(h), the $\mathrm{L_{ESD}}$ (0.42 nH), $\mathrm{L_2}$ (0.42 nH), C_B (42 fF), and D_P and D_N (500 fF) are used to realize ESD protection with T-diode. In Fig. 26(i) of π-model ESD protection, the used $\mathrm{L_{ESD}}$ is 1.1 nH, and each ESD diode is 100 fF. It should be note that the ESD inductors must be realized with wide metal traces and occupy large chip area, so the inductors usually dominate the layout area of ESD protection circuits.

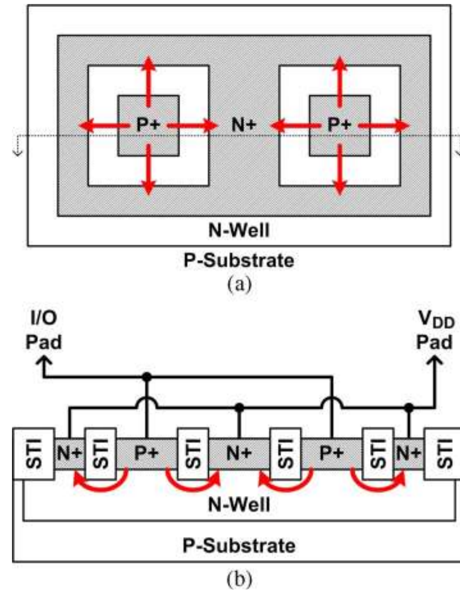

Fig. 27. (a) Layout top view and (b) device cross-sectional view, of p+n-well diode in waffle layout structure.

Besides, the resistive/capacitive ESD protection devices used in every circuit can be carefully drawn to reduce their parasitic capacitance in layout. The waffle layout structures for diodes and SCR devices have been presented [41]–[43]. The ESD protection device with the maximum ratio of perimeter to area is preferred because it has the maximum ratio of ESD robustness to parasitic capacitance. Fig. 27 shows the layout top view and cross-sectional view of two waffle p+n–well diodes connected in parallel. The p+ diffusions are implemented in the n-well region and surrounded by the n+ diffusions. The arrows in Fig. 27 show the ESD current paths. The ESD currents can be discharged through four directions from each p+ diffusion. Under the same parasitic capacitance, the waffle diodes have the better ESD robustness than the traditional ESD diodes. In other words, the parasitic capacitance of ESD protection devices in waffle layout can be reduced under the same ESD robustness.

Although the sample layout of RF ESD protection designs are provided in this section, the actual layout in real case must be carefully considered to optimize both RF performance and ESD robustness simultaneously.

VI. Conclusion

A comprehensive overview in the field of ESD protection design for RF front-end circuits has been presented. To optimize both RF performance and ESD robustness simultaneously, the undesired parasitic effects from ESD protection devices must be minimized or cancelled. Furthermore, the ESD protection circuits and RF front-end circuits can be co-designed to achieve

both good circuit performance and high ESD robustness. The on-chip ESD protection designs for RF circuits will continuously be an important design task, as the operating frequencies of RF circuits increase.

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