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Oxide TFT Rectifiers on Flexible Substrates Operating at NFC Frequency Range

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ABSTRACT This paper presents the experimental characterization of different rectifier circuits using indium–gallium–zinc-oxide thin-film transistor technologies either at NFC or a high frequency range (13.56 MHz) of RFID. These circuits include a single ended rectifier, its differential counterpart, a bridge rectifier, and a cross-coupled full wave rectifier. Diodes were implemented with transistors using conventional processing steps, without requiring short channel devices (L=15 μm). Hence, there is no need for either extra masks or processing steps unlike the Schottky diode-based implementation. These circuits were fabricated on a PEN substrate with an annealing temperature not exceeding 180 °C. This paper finds a direct application in flexible low-cost RFID tags since they enable integration of the required electronics to implement tags with the same fabrication steps.

INDEX TERMS a-IGZO TFT, rectifiers, flexible electronics, RFID tags.

I. INTRODUCTION

RFIDs are playing a vital role in many applications spanning from item level tracking in warehouse, supply chain to security [1]. In near field communication range (< 1 m) high frequency (HF) passive RFID tags can become even more attractive in tremendous applications if they can be implemented on flexible substrates with low cost. Indium-Gallium-Zinc-Oxide Thin-Film Transistors technology (IGZO TFT) is a perfect choice to implement HF passive RFID tags due to unique technology advantages, such as, compatibility with low-cost and low-temperature fabrication techniques [2], [3]. Moreover, robust operation under mechanical stress can be achieved by using thin flexible substrates and considering neutral strain point principles for stack design [4].

A typical RFID or NFC system with a passive tag is shown in Fig. 1. Passive tags do not require on-chip power supply. When the reader sends a signal to the tag, the printed antenna in the tag receives the RF signal. In order to receive maximum power, a proper matching network is needed. This RF energy will be converted into DC with the help of a rectifier circuit, where this DC voltage acts as the supply for the digital circuits in the tag. Based on the data driven by this digital circuit the modulation element (a simple TFT) together with antenna sends the data to the reader for identity verification. It can be noticed that the rectifier is one of the important functional blocks in this passive tag.

Many works have been reported on rectifiers implementation with organic and oxide TFT technology [5]–[12]. The cross-coupled rectifier output amplitude is compromised at 13.56 MHz due to inferior mobility of organic TFTs [5]. Though lower frequency of operation is noticed from [6], cross-coupled designs with oxide TFTs [7], [8] have shown superior performance at this frequency. In fact, the fullwave and halfwave rectifier reported in [9] and [10] are able to

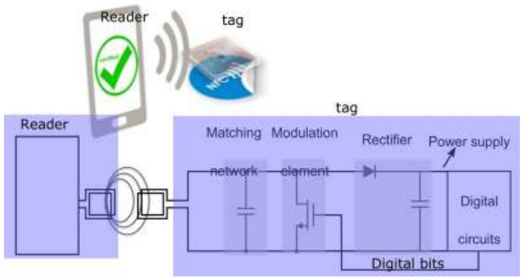

FIGURE 1. Typical RFID communication block diagram.

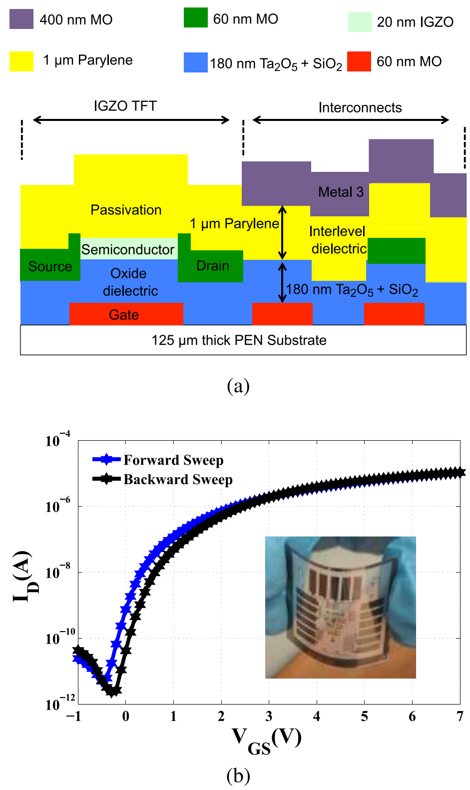

FIGURE 2. (a) Cross sectional view of the TFT and interconnects adopted in this work (b) Linear transfer characteristics of a single TFT with W = 320 μm and L = 15 μm at V_{DS} = 0.1 V. Subset containing individual TFTs, rectifiers and other circuits fabricated on a 125μm thick PEN flexible substrate.

meet UHF range with schottky diodes. While [9] reports rectifier on glass, the rectifier reported in [10] is on flexible substrate. Coming to the schottky diode based implementation, the processing steps and masks are different from the conventional TFT fabrication process, which increases the fabrication cost.

It should be noted that when the complete RFID tag is being implemented with same processing steps without increasing the number of masks, low fabrication cost can be attained, which is the main requirement of many real world applications that need RFIDs. It is also worth to note that all reported works with oxide TFTs [7], [8] are limited to high temperatures ($\geq$ 300°C) and rigid substrates, whereas, real-world applications mostly demand electronics on flexible substrates. In addition, [11], [12] report interesting works on RFID tags using organic p-type TFTs on foil. Here, the complete system and the rectifiers are operated at a supply voltage $\geq$ 18 V whereas, low power IOT system demands low supply voltages. As a route to overcome these limitations, the present work reports and compares, for the first time ever, rectifiers with different architectures based on a low-temperature flexible oxide TFT process, able to achieve 13.56 MHz operating frequency with only <6 V supply voltage. The process is fully compatible with polyethylene naphthalate (PEN) substrates and makes use of large-sized transistors (L=15 μm), fully compliant with current large area electronics fabrication tools. Note that the adoption of miniaturized devices (e.g., L=2 μm), besides imposing many challenges to conventional lithographic tools, can bring undesirable short-channel effects [13].

II. DEVICE AND CIRCUIT FABRICATION

A 60 nm thick Mo gate electrode is sputtered on a 125 μm thick PEN substrate. Then, a 180 nm thick multilayer/multicomponent dielectric is cosputtered without intentional substrate heating, using SiO_2 and Ta_2O_5 targets, followed by dry etching process in SF_6 atmosphere; A 20 nm thick semiconductor layer is then deposited without intentional substrate heating, using ceramic IGZO target (In:Ga:Zn atomic ratio of 2:1:2) and Ar+O_2 atmosphere and patterned by liftoff. Source and drain electrodes are sputtered with 60 nm thick Mo. Gate, dielectric and source/drain patterning is done by dry etching process in SF_6 atmosphere; The interlevel dielectric is 1 μm thick parylene layer, patterned using a dry etching process in O_2 atmosphere; On top of this layer, metal 3 is deposited: by sputtering 400 nm thick Mo, followed by dry etching process in SF_6 atmosphere. The devices were annealed at 180°C for 1 hour in air before source/drain deposition and at the end of the process. The cross sectional schematic view of the IGZO TFT and interconnects are presented in Fig. 2(a). In order to minimize the parasitics due to interconnects (overlap of gate to source/drain) and to further improve the yield of the process for circuits operation with this technology, metal 3 (400 nm thick Mo) is being used. This brings the additional advantage of achieving IGZO back-channel surface passivation with the interlevel dielectric, i.e., no extra processing steps are required to assure robust operation of the TFTs. Inset of Fig. 2(b) shows a PEN substrate containing isolated TFTs and various circuits including rectifiers. It also demonstrates linear transfer characteristics of the TFT with W = 320 μm and L = 15 μm. These devices are showing a turn-on voltage of −0.5 V, mobility of 12 cm^2/V.s and on-off ratio exceeding 10^7. Small clockwise hysteresis, concomitant with charge trapping phenomena at dielectric/semiconductor interface, is noticed from the plot.

Transistor performance is unaffected by bending radius of at least 15 mm [14].

III. CIRCUIT DESIGN

Four rectifier circuits are being considered in this work; (i) Single ended (ii) Differential (iii) Cross-coupled and (iv) Bridge. All these circuits are implemented with the IGZO TFTs and their circuit schematics and micrographs are presented in Figs. 3 and 4. In these circuits, the conductive path during positive and negative half cycles are being demonstrated by red dashed line and violet dotted line, respectively, as can be noticed from Fig. 5. In single ended implementation, the input capacitor (C_1) blocks the dc value and feeds only signal to diodes (D_1 and D_2). During positive half cycle, D_1 turns 'ON' and D_2 turns off. The load capacitor charges with the current flowing in the circuit and V_{out} is almost equal to one threshold voltage (V_{TH}) less than V_{in}, i.e., $V_{in} - V_{TH}$, where V_{TH} drop is due to diode-connected TFT used for realizing D_1. During the negative half cycle these diodes interchange their roles and C_1 is connected to ground. When there is a no leakage path at the output, the same voltage level at previous positive half cycle is maintained at the output. The operating principle can be adapted to the differential version implementation (see Fig. 5(b)). This acts as a full wave rectifier. Especially when there is finite resistive load, full wave rectifier gives improved output compared to the single ended or half wave counter part, as there is always a conductive path in the circuit for both positive and negative half cycle of the input. Same analysis can be applied to the cross-coupled and bridge rectifiers. Their conductive paths for different inputs can be observed in Fig. 5(c) and (d). Differential output in case of bridge rectifier is almost 2(V_{in} - V_{TH}), whereas, in the cross-coupled design, one V_{TH} drop is being replaced with the overdrive voltage (V_{OD}) of T_1 or T_2 (see Fig. 5(c)). By making these TFTs wider, it is possible to reduce the overdrive voltage and improve output dc compared to the bridge rectifier.

IV. RESULTS AND DISCUSSION

All the measurements were carried out at normal ambient with the help of passive agilent oscilloscope probes (10 MΩ//15 pF) and fixed probe with keysight B1500A. The frequency response and voltage transfer characteristics (output dc voltage *versus* input ac voltage peak value) can be noticed at 13.56 MHz from Fig. 6. Expected V_{TH} drop can be observed from the voltage transfer characteristics, where V_{TH} variations are within ± 0.2 V. For these circuits, TFTs have a channel length of 15 μm and widths are ranging from 80 to 320 μm.

At higher frequencies (> 15 MHz), the output voltage is degraded significantly, since it is expected that the transistors cannot show proper functionality beyond their unity gain current cutoff frequency [13]. At these high frequencies, there is not enough time for the devices to form the

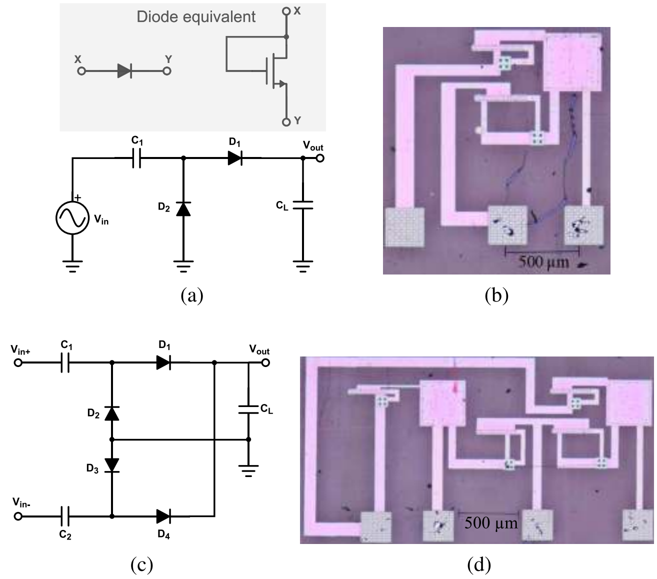

FIGURE 3. Rectifiers with different configurations: (a) Single ended circuit schematic (b) Single ended micrograph (c) Differential rectifier circuit schematic (d) Differential rectifier micrograph. All diodes in these schematics are being implemented with diode-connected transistors as shown in Fig. 3 (a).

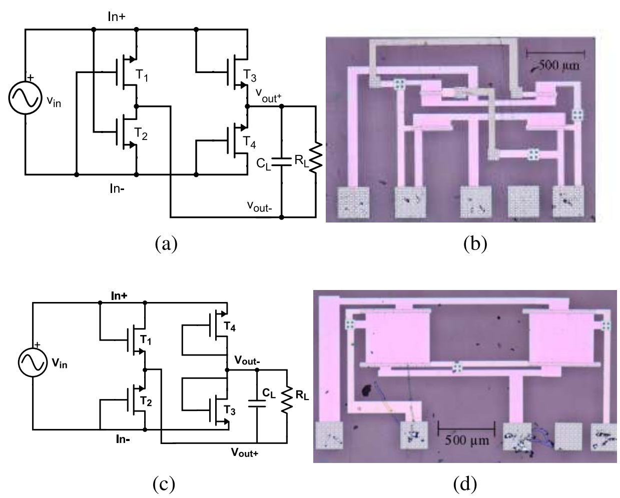

FIGURE 4. Rectifiers with different configurations: (a) Cross coupled rectifier circuit schematic (b) Cross-coupled rectifier micrograph (c) Bridge rectifier circuit schematic (d) Bridge rectifier micrograph.

conductive channel in 'ON' state and discharge the complete channel charge, when it moves to the 'OFF' state. Nevertheless, operational yield of the rectifiers at NFC range can be improved by decreasing the TFT's channel length and/or decreasing gate-to-source/drain overlaps [13]. Though bridge rectifier is showing slightly higher voltage at the output compared to other configurations due to nominal V_{TH} variations, by employing wider devices, cross-coupled configuration can ensure improved output voltage since V_{TH} drop will be replaced by the V_{OD} of the TFT. As the device becomes wider, V_{OD} can be close to zero volts. In fact, by replacing the diode connected TFTs in Fig. 5(c), with

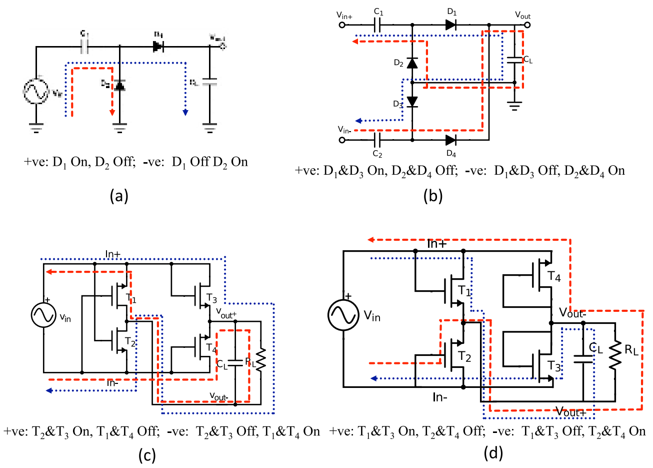

FIGURE 5. Circuit operation during positive (conductive path denoted by red line) and negative (conductive path denoted by violet line) half cycle of the input: (a) Single ended (b) Differential (c) Cross-coupled [8] (d) Bridge rectifier.

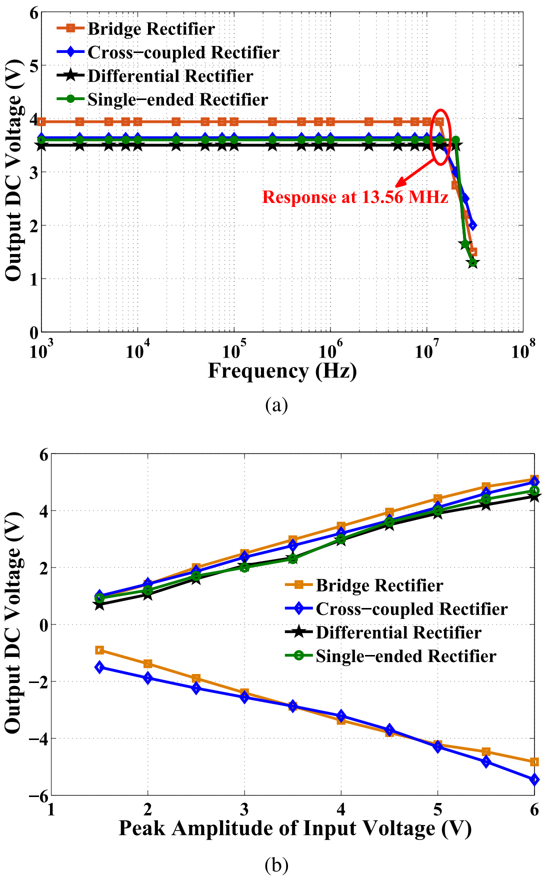

FIGURE 6. Rectifiers measured response: (a) Frequency response with an input signal peak voltage of 4.5 V (b) Amplitude sweep when the input signal frequency is 13.56 MHz.

cross-coupled TFTs, it is possible to eliminate voltage drop in the circuit and output voltage can be equal to the peak value of the input voltage, if there is no discharging path at the output.

V. CONCLUSION

This work analysed different rectifiers from flexible substrates for NFC applications. Expected behaviour can be noticed from measured result at relatively low voltages to ensure low-power operation, without requiring miniaturized devices for 13.56 MHz operation. Since all the rectifiers were fabricated with the same processing steps and masks as the standard oxide TFT fabrication process at low temperature, this work opens a window for low-cost flexible RFID tags that can be used in different applications ranging from item level tracking to security.

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REFERENCES

[1] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards, Radio Frequency Identification and Near-Field Communication*. Chichester, U.K.: Wiley, 2010. doi: 10.1002/9780470665121.
[2] K. Nomura *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Oct. 2004.
[3] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, 2010, Art. no. 044305.
[4] Y.-H. Kim, E. Lee, J. G. Um, M. Mativenga, and J. Jang, "Highly robust neutral plane oxide TFTs withstanding 0.25 mm bending radius for stretchable electronics," *Sci. Rep.*, vol. 6, May 2016, Art. no. 25734.
[5] R. Rotzoll *et al.*, "Radio frequency rectifiers based on organic thin-film transistors," *Appl. Phys. Lett.*, vol. 88, no. 12, 2006, Art. no. 123502.
[6] S. H. Cho *et al.*, "Oxide thin film transistor circuits for transparent RFID applications," *IEICE Trans. Electron.*, vol. E93.C, no. 10, pp. 1504–1510, 2010.
[7] B. R. McFarlane *et al.*, "AC/DC rectification with indium gallium oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 314–316, Apr. 2010.
[8] T. Kawamura *et al.*, "Oxide TFT rectifier achieving 13.56-MHz wireless operation," *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 3002–3008, Nov. 2012. doi: 10.1109/TED.2012.2213091.
[9] A. Chasin *et al.*, "An integrated a-IGZO UHF energy harvester for passive RFID tags," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3289–3295, Sep. 2014. doi: 10.1109/TED.2014.2340462.
[10] J. Zhang *et al.*, "Flexible indium gallium zinc oxide Schottky diode operating beyond 2.45 GHz," *Nat. Commun.*, vol. 6, Jul. 2015, Art. no. 7561.
[11] E. Cantatore *et al.*, "A 13.56-MHz RFID system based on organic transponders," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 84–92, Jan. 2007.
[12] J. Genoe, K. Myny, S. Steudel, and P. Heremans, "Design and manufacturing of organic RFID circuits: Coping with intrinsic parameter variations in organic devices by circuit design," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 496–499.
[13] P. G. Bahubalindruni *et al.*, "Influence of channel length scaling on InGaZnO TFTs characteristics: Unity current-gain cutoff frequency, intrinsic voltage-gain, and on-resistance," *J. Display Technol.*, vol. 12, no. 6, pp. 515–518, Jul. 2016.
[14] P. G. Bahubalindruni *et al.*, "High-gain transimpedance amplifier for flexible radiation dosimetry using InGaZnO TFTs," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 760–765, Jun. 2018.

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