P-11: DC/AC Electrical Instability of R.F. Sputter Amorphous In-Ga-Zn-O TFTs

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Abstract

The paper presents the study of electrical instability of RF sputter amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) induced by negative steady-state (or D.C.) bias-temperature-stress (BTS). Similarly to positive BTS results [8], the stress time evolution of the threshold voltage shift (ΔV_{th}) induced by negative BTS under different stress voltages and temperatures can all be described by the stretched-exponential model. For the first time, we also present the results for ΔV_{th} under pulse (or A.C.) BTS. The ΔV_{th} for positive A.C. BTS is found to have a pulse-period dependence while a huge reduction of ΔV_{th} is found for all negative A.C. BTS results. This might suggest the time for holes to accumulate near the a-IGZO/ SiO_2 interface is much longer than the time for electrons. The effect of bi-polar stressing is also discussed.

1. Introduction

During the past few years, there have been great interests in using amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) in AM-FPDs. Because the electrons are drifting through ionic metal s-orbital, which permit a band-like conduction even in amorphous phase, a-IGZO TFTs have a higher field-effect mobility (μ_{eff}) than traditional covalent bond semiconductors (e.g. a-Si:H) [1]. These properties make a-IGZO TFTs one of the ideal choices for future large area (e.g. 82-inch) ultra-definition (up to 4k×4k pixels, [2,3]) display backplane technology.

To ensure a robust product based on a-IGZO TFTs, it is essential to evaluate their electrical stability. The long-term constant current-temperature stress (CTS) study has shown that the a-IGZO TFT has a stable electrical properties with a threshold voltage shift (ΔV_{th}) much smaller (0.2V) than the ΔV_{th} for a-Si:H TFT (>1.8V) under the same AM-OLED stress conditions (3μA, 60^0C, 20 hours) [4]. The proper passivation layer for the back channel was also found to play an important role in improving the TFT CTS reliability [5]. Recent studies further extended investigation of a-IGZO stability into the bias-temperature stress (BTS) measurements. A positive shift of TFT V_{th} was observed under a positive (gate bias) BTS while the V_{th} shifted to negative values for negative BTS [6]. Furthermore, a simple power law relation is able to fit the stress time trend of measured ΔV_{th} [7]. A great reduction (~75%) in BTS induced degradation was found when additional post thermal annealing step during fabrication is performed. Although the nature of this reduction is not clear, the defect states located in bulk active layer or near the interface are suspected to be of its origin [6].

Despite all the progress in a-IGZO TFTs so far, our knowledge of the physical origin of its electrical stability is very limited, and should be addressed more in-depth. We have conducted a detail analysis of the positive BTS induced threshold voltage shift (ΔV_{th}) for RF sputter a-IGZO TFTs, and modeled both stress bias voltage and temperature dependence by the well developed stretched-exponential equation [8]. In this work, we further explore the ΔV_{th} for RF sputter a-IGZO TFT under prolonged (steady-state, D.C.) negative BTS. Since the TFTs are driven by external clock signal during operation, TFT stability under A.C. stress should be addressed as well. Therefore, we report in this paper on pulse (e.g. A.C.) BTS for RF sputter a-IGZO TFTs. The effect of pulse period and bipolar pulse stressing is also discussed.

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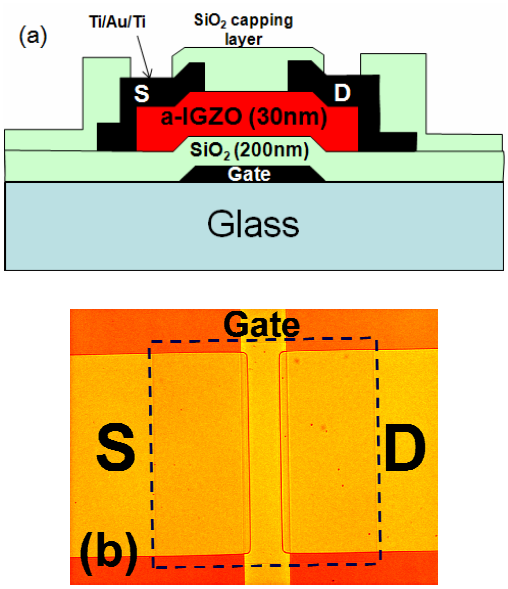

Figure 1. (a) Cross-sectional and (b) top view of the RF sputter a-IGZO TFT device used in this study. Dash square indicates the region of a-IGZO active layer.

2. Experimental

2.1. TFT Structure

The cross-sectional view of the a-IGZO TFT used in this study is shown in Fig. 1(a). The detail processing steps were discussed elsewhere [9]. The TFT has an inverted-staggered bottom-gate structure. The Ti/Au/Ti stacking layers are used for gate and source/drain (S/D) electrodes. The SiO_2 gate insulator and a-IGZO active layer is about 200nm and 30nm thick, respectively. Both layers are deposited by RF magnetron sputtering. After the island formation and S/D electrodes definition, an additional sputter SiO_2 capping layer is added which serves as a protection layer for the TFT back channel. Finally, a thermal annealing step (200^0C, 1 hour in air) is applied. The die photo of the final RF sputter a-IGZO TFT is shown in Fig. 1(b).

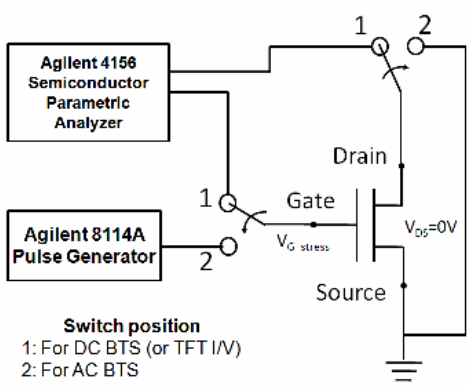

Figure 2. The schematic of the circuit setup used for DC and AC BTS experiments. Switch matrix (HP E5250A) positions are also indicated.

2.2. Electrical Measurement

A series of D.C. and A.C. BTS experiments were conducted by using a semiconductor parametric analyzer (Agilent 4156C), pulse generator (Agilent 8114A), switch matrix (HP E5250A) and a light tight probe station (Figure 2). The entire setup is controlled by an in-house LabView^{TM} driving program. During BTS (both D.C. and A.C.), a predetermined stress voltage (V_{G_stress}) is applied to the gate electrode and to ensure a uniform electrical field distribution along the SiO_2/ a-IGZO interface, the drain terminal of TFT is shorted to its source terminal (V_{DS}=0V, Figure 2). We monitor the evolution of device degradation by interrupting the BTS at predetermined time steps and measuring the TFT saturation region (V_{DS}=20V) transfer properties. In order to ensure a consistent comparison of extracted parameter between different BTS time steps, a fixed data range is defined for parameter extraction. In this study, threshold voltage (V_{th}) and field-effect mobility (μ_{eff}) were extracted from the linear fit of the saturation region transfer curves between $(I_{DS})^{1/2}$=0.01~0.001 $A^{1/2}$ to the standard MOSFET equation (cf. Figure 3):

$$\sqrt{I_{DS}} = \left(\frac{\mu_{eff} C_{ox} W}{2L}\right)^{1/2} (V_{GS} - V_{th}) \qquad (1)$$

where C_{ox} is gate insulator capacitance per unit area, W and L are channel width and length, respectively. For reference, our RF sputter a-IGZO TFTs have following room temperature properties: μ_{eff} =8.02 cm^2/Vs, V_{th}=2.2 V, sub-threshold swing (S)~0.4 V/dec, off state drain current~10^{-13}A and on-to-off current ratio over 10^9. These indicated a very good electrical performance of the a-IGZO TFT used in this study. Finally, it should be notice that all the BTS induced electrical instability can be fully recover after a thermal annealing step (2 hour, 200^{0}C) [8]. Each series of BTS experiment is performed on the same TFT and to ensure consistent initial TFT properties, the thermal annealing is applied before each new BTS experiment is conducted.

3. Results and Discussion

3.1. Negative, D.C. BTS Experiment

Figure 3 shows a typical evolution of the a-IGZO TFT I_{DS}-V_{GS} curves under negative D.C. BTS. A uniform negative shift is observed for both ON and sub-threshold regions. To demonstrate the

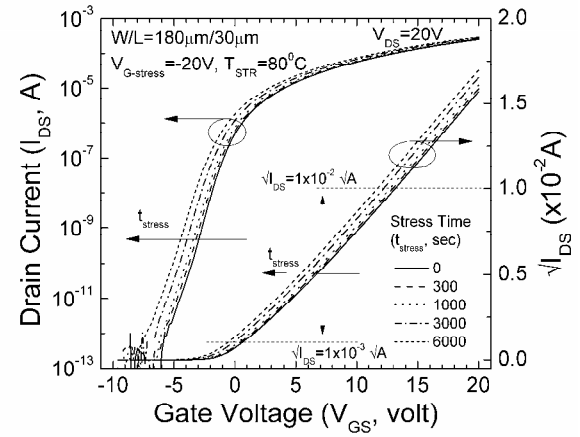

Figure 3. The evolution of the RF sputter a-IGZO TFT transfer characteristics for steady-state (D.C.) negative BTS (V_{G_stress}=-20V, T_{STR}=80^{0}C).

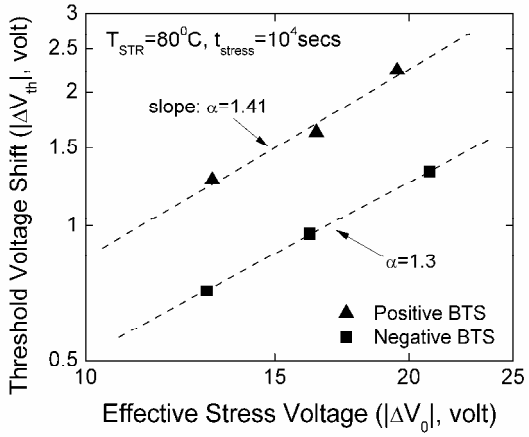

Figure 4. The evolution of the RF sputter a-IGZO TFT transfer characteristics for steady-state (D.C.) negative BTS (symbol: ■, V_{G_stress}=-20V, T_{STR}=80^{0}C). Data for positive BTS (symbol: ▲, adopt from [8]) is also shown as reference.

validity of using stretched-exponential model to describe the negative BTS results, we followed a similar methodology that has been developed for positive BTS experiments [8]. The stretched-exponential model describes the ΔV_{th} by the following formula [10]:

$$|\Delta V_{th}| = |\Delta V_0|^{\alpha} \left\{1 - \exp\left[-\left(\frac{t_{stress}}{\tau}\right)^{\beta}\right]\right\} \qquad (2),$$

where $\Delta V_0 = V_{G\_stress} - V_{th\_initial}$ (3)

and $\tau = \tau_0 \exp\left(\frac{E_\tau}{kT_{STR}}\right)$ (4).

In the above equations, ΔV_0 is the effective voltage drop across the gate insulator; $V_{th\_initial}$ is the initial threshold voltage; α is the exponent for ΔV_0 dependence and β is the stretch-exponential exponent. E_τ is the average effective energy barrier for carrier in channel to overcome before they can enter the insulator, with τ_0

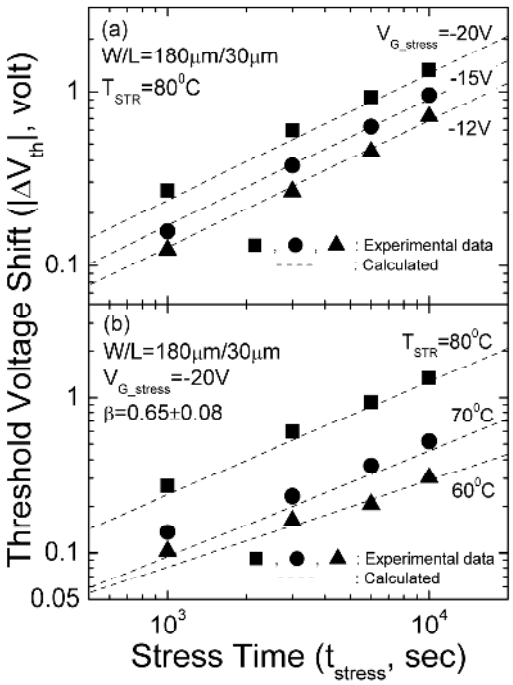

Figure 5. ΔV_{th} versus stress time (t_{stress}) for various (a) stress voltage (V_{G_stress}=-20V, -15V and -12V) and (b) temperature (T_{STR}=80^{0}C, 70^{0}C and 60^{0}C). Symbols represent the experimental data while dashed lines are the calculated fits to stretched-exponential model (eq.(2)).

being the thermal pre-factor for emission over barrier. Series of negative D.C. BTS experiments under different V_{G_stress} (= -12~ -20V) and stress temperature (T_{STR}=60^{0}C ~80^{0}C) were performed. The α is first extracted from the log(ΔV_{th}) vs. log(ΔV_0) plot as depicted in Figure 4. Corresponding data for positive D.C. BTS is also shown as reference [8]. The extracted α for positive BTS (=1.41) is larger than the one extracted for negative BTS (=1.3); this result suggests that the ΔV_{th} for positive BTS is more sensitive to V_{G_stress}. Figure 5 show the evolution of ΔV_{th} as a function of stress time (t_{stress}) under different negative BTS conditions. The dash lines are the numerical fits to eq.(2). The characteristic trapping time, τ, is treated as fitting parameter and plotted as a function of 1/kT_{STR} in Figure 6. In Figure 5, error was observed between experimental and calculated data for short stress time (<10^3 secs). This is because the ΔV_{th} for these data points are very close to the measurement resolution (~0.2V) set in this study. Despite the errors, the stretched-exponential model is able to universally reproduce the trend of experimental data, regardless of magnitude of the stress voltage or stress temperature.

To determine the ΔV_{th} dependence on stress temperature, we extract the E_τ and τ_0 by applying eq.(4) to the τ vs. 1/kT_{STR} plots (Figure 6). Table I summarizes all the parameters used in the stretched-exponential model. The extracted E_τ for positive BTS (0.78eV) is smaller than the value of negative BTS (2.16eV). This suggest that the electrons are experienced a lower energy barrier than holes do during the charge injection process near the a-IGZO/SiO_2 interface. It should be noticed that there is an exponential dependence of τ_0 on the y-axis intercept of the linear fit of data in Figure 6. Therefore, the extracted τ_0 can be very sensitive to the y-axis intercept and significant error can occur in our extraction due to the limited number of data points. This can explain abnormally low τ_0 value obtained for negative BTS.

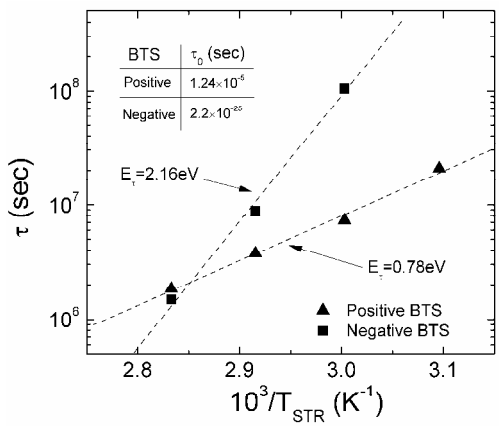

Figure 6. The characteristic trapping time (τ) for positive (symbol:▲, adopt from [8]) and negative (■) BTS as a function of 1/T_{STR}. (T_{STR} range: 50^{0}C ~ 80^{0}C). Dash line: numerical fit to eq.(4).

Table I. Fitting parameters for stretched-exponential model

Model Parameters	Value	
	Positive BTS*	Negative BTS
α	1.41	1.30
β	0.75	0.65
τ_0 (sec)	1.24×10^{-5}	2.2×10^{-25}
E_τ (eV)	0.78	2.16

*** Adopt from [8].**

3.2. A.C. BTS Experiment

To study the change on TFT I/V properties under A.C. operation, a periodic pulse signal was applied to RF sputter a-IGZO TFT gate terminal during the A.C. BTS experiments. The inset of Figure 7 illustrates the waveform of the gate pulse signal. The pulse period (PD) is changed from 10ms to 100ms (or corresponding to 100Hz to 10Hz) during the A.C. BTS. The signal is in its "pulse state" for duration of pulse width and the duty-cycle of the signal is defined as ratio between pulse width (PW) and period (PD):

$$Duty\ cycle = \frac{PW}{PD} \quad (5).$$

Since the duty cycle in this study is set to be 50%, the pulse widths for all A.C. BTS experiments are half of their corresponding period. All pulse signals have a base line of 0V and the V_{G_stress} is defined as the polarity/amplitude of the pulse signal. Both positive and negative A.C. BTS are conducted. Figure 7 shows the evolution of ΔV_{th} as a function of effective stress time, which is defined as the accumulated time when the gate signal is at its high level (HL). The results show that the ΔV_{th} for positive A.C. BTS is pulse width (or period) dependent. A shorter period can correspond to a smaller shift in threshold voltage. For a 100Hz gate pulse signal the reduction of ΔV_{th} can be as large as 50% as compare with the corresponding positive D.C. BTS value. The negative A.C. BTS result show even larger reduction of the threshold voltage shift. For all the gate pulse period we investi-

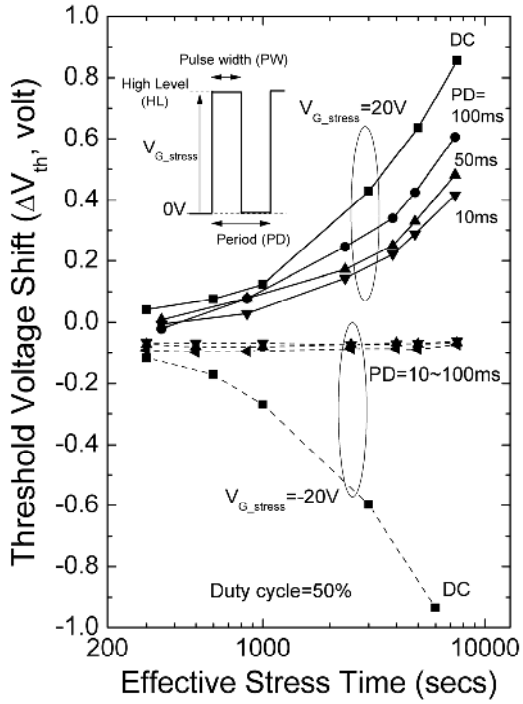

Figure 7. The ΔV_{th} versus effective stress time for both positive (V_{G_stress}=20V, solid curves) and negative (V_{G_stress}=-20V, dash curves) A.C. BTS. The pulse period (PD) is changed from 10ms to 100ms and D.C. BTS results are also shown as reference. The a-IGZO TFT used in this study has a channel width over length ratio of 180µm/30µm.

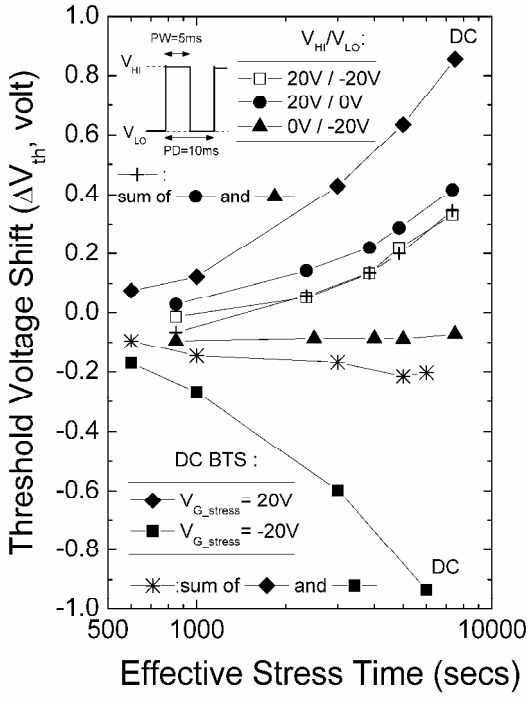

Figure 8. The ΔV_{th} versus effective stress time for (● ,▲) uni-polar and (□) bi-polar A.C. BTS. The inset and table illustrate the pulse waveform for each individual condition. The pulse width, period and duty cycle for all A.C. BTS are 5ms, 10ms and 50%, respectively. The D.C. BTS (◆ , ■) results are also shown as reference.

gated (10~100ms), the negative A.C. BTS induced ΔV_{th} is very small (<0.1V) without a clear dependence on pulse period. Such behavior is quite different from what we observed under positive A.C. BTS. This might suggest a very long characteristic time for hole to accumulate at the SiO_2/a-IGZO interface under negative bias and the pulse width of the negative A.C. BTS applied in this study could be too short for hole to accumulate. Therefore, carrier injection/ trapping events are greatly reduced and results in a minimum ΔV_{th} observed.

The effect of bi-polar pulse stressing is also studied. To better describe the waveform, the voltage of pulse high and low states are specified as V_{HI} and V_{LO}, respectively. Figure 8 shows one example by employing a bipolar gate stress signal with V_{HI} /V_{LO} = 20V/-20V. Compare to the uni-polar stress (V_{HI}=20V), bi-polar A.C. BTS shows about 20~30% reduction of ΔV_{th}. Such reduction is primarily due to the contribution from the negative cycle of the stress. As illustrated in Figure 8, the ΔV_{th} induced by bi-polar A.C. BTS (symbol: □) is approximately equal to the ΔV_{th} obtained by simply adding up the ΔV_{th} for corresponding uni-polar A.C. BTS values (symbol: +). In addition, due the dependence of ΔV_{th} on pulse period, add up the ΔV_{th} obtained from positive and negative D.C. BTS (symbol: *) is not able to predict the bi-polar A.C. BTS results.

4. Conclusion

We have investigated both D.C. and A.C. BTS stability in RF sputter a-IGZO TFT. The stretched-exponential formula is proposed for accurate D.C. BTS stability modeling. Furthermore, ΔV_{th} dependence on stress voltage and temperature can be described. The TFT degradation under a periodic, pulse gate stress voltage is also investigated. The results show the ΔV_{th} induced by positive A.C. BTS is pulse width (or period) dependent. On the other hand, a huge reduction in ΔV_{th} is observed for all the negative A.C. BTS results (with pulse period = 10ms~100ms). Such behavior should be studied in more detail to predict the device life-time. Finally, ΔV_{th} induced by bi-polar stressing is found to be approximately equal to the ΔV_{th} obtained by simply adding up the ΔV_{th} for corresponding uni-polar A.C. BTS values.

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