P/G TSV Planning for IR-drop Reduction in 3D-ICs

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***Abstract*—In recent years, interconnect issues emerged as major performance challenges for Two-Dimensional-Integrated-Circuits (2D-ICs). In this context, Three-Dimensional-ICs (3D-ICs), which consist of several active layers stacked above each other, offer a very attractive alternative to conventional 2D-ICs. However, 3D-ICs also face many challenges associated with the Power Distribution Network (PDN) design due to the increasing power density and larger supply current compared to 2D-ICs. As an important part of 3D-IC PDNs, Power/Ground (P/G) Through-Silicon-Vias (TSVs) should be well-managed. Excessive or ill-placed P/G TSVs impact the power integrity (e.g. IR-drop), and also consume a considerable amount of chip real estate. In this work, we propose a Mixed-Integer-Linear-Programming (MILP)-based technique to plan the P/G TSVs. The goal of our approach is to minimize the average IR-drop while satisfying the total area constraint of TSVs by optimizing the P/G TSV placement. Therefore, the locations, sizes and the total number of the P/G TSVs are co-optimized simultaneously. The experimental results show that the average IR-drop can be reduced by 11.8 % in average using the proposed method compared to a random placement technique with a much smaller runtime.**

I. Introduction

At present, *Three-Dimensional-Integrated-Circuits* (3D-ICs), using *Through-Silicon-Vias* (TSVs) and die-stacking to connect several active layers, have emerged as a promising option to overcome the interconnect issues related to modern 2D-ICs [1]. Using 3D integration with TSVs, the interconnection length between vertically stacked ICs can be significantly reduced compared to traditional 2D-ICs. This translates into less wire delay and higher performance. For this reason, TSV-based 3D-ICs are undoubtedly gaining momentum and become a promising solution for the design of high performance complex systems. For example, Sony's new "Exmor RS" image sensor uses already 3D-ICs [2]. However, there are many challenges involved in the design of 3D-ICs.

Among the existing design issues of 3D-ICs, including thermal challenges [3], [4], [5] and routing congestion [6], the reliable power supply design is one of the major challenges in 3D-ICs [7]. In particular, smaller footprints combined with multiple stacked dies imply more severe power delivery problems [8]. Moreover, due to routing congestions, the number of available TSVs for *Power/Ground* (P/G) nets is limited. Thus, it becomes a challenging task to deliver enough current to all parts of the 3D stack while guaranteeing high power integrity for the stable operation of 3D-ICs, i.e., low voltage drop in DC components (IR-drop) and low voltage fluctuation in AC components (Ldi/dt). In 3D-ICs, IR-drop is particularly important since die stacking has a higher impact on IR-drop than Ldi/dt noise [9]. Therefore, to enhance power integrity in 3D-ICs, the *Power Distribution Network* (PDN) has to be carefully designed to minimize IR-drop.

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Since, P/G TSVs are an integral part of the 3D PDN, they should be optimally planned, to realize a reliable power supply design in 3D-ICs. Therefore, it is necessary to consider the TSV placement [1], [10] as well as the TSV sizes [11] when minimizing the IR-drop of 3D-ICs. Moreover, the area demand of P/G TSVs, which can lead to routing congestion, should also be taken into account. However, there is a potential conflict between IR-drop and area demand: using bigger and more P/G TSVs can reduce the IR-drop at the expense of an increased area demand, i.e., increased routing complexity and the possibility of routing congestion. Therefore, it is necessary to co-optimize the location, size and number of TSVs.

Currently, only a few techniques have explored P/G TSV planning, and most of them focus only on the placement of P/G TSVs. In [8], [9], [12], a regular P/G TSV placement is considered, i.e. the density and the location of P/G TSVs are predetermined. In [13], the density of P/G TSVs in each P/G tile is optimized to meet power noise requirements by inserting P/G TSVs after the placement for simultaneous power integrity and thermal optimization. However, the nonlinear optimization in this work makes the algorithm less applicable to large designs. In [14], a non-regular P/G TSV placement algorithm is proposed to reduce the number of P/G TSVs while achieving a given IR-drop requirement, in order to mitigate routing congestion in 3D-ICs. However, the impact of the P/G TSV size is ignored. In fact, in a realistic 3D-IC design, various P/G TSV sizes can be used, which can affect both IR-drop and routing congestion. Thus, a refined plan for the size of P/G TSV is also needed for a reliable 3D PDN design, besides the optimization of the location and the number of P/G TSVs. However, to the best of our knowledge, none of the existing techniques considers these three factors (number, location and size) simultaneously during the 3D PDN design.

In this work, we present a comprehensive P/G TSV planning considering the P/G TSV locations, sizes and the total number in a 3D chip. Our objective is to minimize the average IR-drop while meeting a given area constraint. To solve this multi-dimensional optimization problem, we propose an algorithm based on *mixed integer linear programming* (MILP). Unlike existing techniques, in which TSV sizing and placement are performed independently, and the PDN optimization is performed in an iterative process, we provide a fast and scalable MILP-based method for co-optimization of TSV sizing and placement for IR-drop reduction in just one step.

The rest of this paper is organized as follows. Section II presents the background of PDN in 3D-ICs. Section III motivates the main idea of this work. Section IV describes our MILP-based methodology. In Section V, we report our experimental results. Finally, conclusions are drawn in Section VI.

II. Background

In 3D-ICs, the supply power is fed from the package through Controlled Collapse Chip Connection (C4) bumps and is distributed over the bottom-most layer via the on-chip PDN. To reach upper layers, the supply power travels through TSVs that connect the different layers. The on-chip PDN is based on a mesh structure (or grid), as shown in Fig. 1. In this structure, the mesh pitch determines the distance between each P/G line, and the mesh width determines the thickness of each power wire. As shown in Fig. 2, a P/G mesh can be constructed for 3D-ICs to supply power by using a global level mesh routed in the top metal layers, where there is one P/G network for the entire chip. For each layer, there is an individual 2D P/G mesh, which is connected using TSVs.

In general, there are two types of 3D P/G network topologies: uniform and non-uniform grids. In a uniform mesh the pitches in different layers are the same, while in non-uniform topologies different layers can have different layouts. Without loss of generality, we use a uniform mesh to construct the global mesh in this work, where the pitch of each tier's 2D mesh is equal. However, our proposed methodology can also handle non-uniform network topologies. Moreover, since we focus on the IR-drop in this work, the PDN is optimized using a resistive model, where the branches and TSVs are modeled as resistances.

Once the PDN is created, it needs to be analyzed by calculating all the voltages at the nodes and estimating the IR-drop. Traditionally, the static analysis of a PDN can be formulated as a linear system as shown in [15]:

$$GV = I, \tag{1}$$

where G represents the conductance matrix of the mesh for the interconnected resistors; V is a vector containing all the unknown voltages of the nodes; and I is a vector of current loads. The dimensions of V and I are equal to the number of nodes in the PDN. The detailed structure of matrix G_{2D} is illustrated in [15].

For a 3D case, the conductance matrix G_{3D} of a two-layer IC, each with a power mesh containing N nodes, can be expressed as follows:

$$G_{3D} = \begin{pmatrix} G_{2D_1} + G_{TSV_{1,2}} & -G_{TSV_{1,2}} \\ -G_{TSV_{1,2}} & G_{2D_2} + G_{TSV_{1,2}} \end{pmatrix} \in \mathbb{R}^{2N \times 2N} \tag{2}$$

where $G_{2D_i} \in \mathbb{R}^{N \times N}\,(i = 1, 2)$ is the conductance matrix on layer i without TSVs. $G_{TSV} \in \mathbb{R}^{N \times N}$ represents the conductances due to the TSVs and can be written as:

$$G_{TSV} = diag(..., 0, ..., g_{tsv_1}, ..., 0, ..., g_{tsv_2}, ..., g_{tsv_m}, ...) \tag{3}$$

where g_{tsv_j} is the conductance of the TSV placed at node j of the corresponding power mesh. Since there are at most as many TSVs as nodes in the power mesh, $m \leq N$.

If there are more than two layers in the 3D-IC, both equations can be setup in a similar way, but with Equation (2) being pair-wisely applied between adjacent layers.

Once the PDN without P/G TSVs is created on each layer, the matrix G_{2D} is constant. Hence, the conductance matrix of 3D-ICs G_{3D} depends only on the matrix of TSVs G_{TSV}, which itself is highly dependent on the location, size and the number of P/G TSVs. First, different TSV locations and numbers will affect the position and number of non-zero elements on the diagonal of G_{TSV}. Second, the non-zero values in G_{TSV} depend on the TSV sizes (in this work, the TSV diameter). Based on the analytical expression of the TSV resistance given in [11], the conductance of a TSV is:

$$g_{tsv_{\mathrm{DC}}} = \frac{\pi r_{tsv}^2}{\rho h_{tsv}}, \tag{4}$$

where ρ is the resistance of the conducting material. h_{tsv} and r_{tsv} represent the height and radius of the TSV, respectively. Conventionally, the TSV height is always equal to the die thickness [16]. Hence, the conductance of one TSV only depends on the size of the TSV for a specific TSV fill material. As a result, different TSV sizes will also impact the 3D PDN. Thus, it is necessary to consider the location, size and number of P/G TSVs simultaneously during the 3D PDN design.

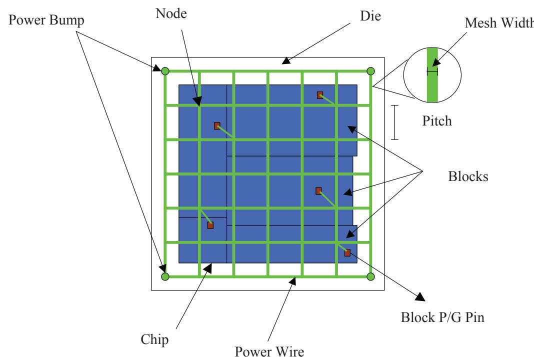


Fig. 1. On-chip power distribution network

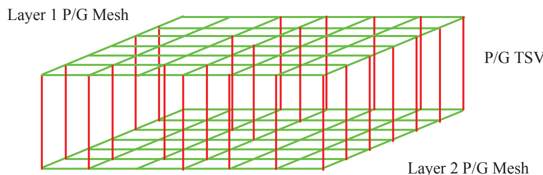
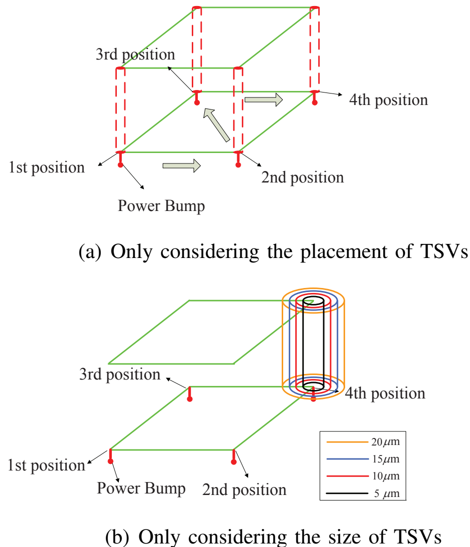


Fig. 2. Three-dimensional uniform P/G network

III. Motivational Example

As motivated, PDN design is an essential procedure in the VLSI design flow. Moreover, 3D integration introduces new challenges for the PDN design due to higher current density and more sophisticated power delivery paths in comparison to 2D-ICs. Since P/G TSVs are fundamental components of PDNs, several P/G TSV planning techniques have been



(a) Only considering the placement of TSVs

(b) Only considering the size of TSVs

Fig. 3. The schematic of two cases: only considering the placement of TSVs and only considering the size of TSVs

recently proposed. In general, they can be classified into two categories: **S1)** *TSV-placement* and **S2)** *TSV-sizing*.

S1: The objective of TSV-placement techniques is to reduce the average IR-drop of the PDN by determining the best placement of the TSVs as well as the optimal number of TSVs [14]. However, in this class of techniques, the sizes of all TSVs are considered to be the same. To illustrate the key idea behind these approaches, consider Fig. 3(a) as an example. In this example the chip consists of two layers, where each of which has a PDN with a 2×2 grid. Hence, there are 4 possible positions to place at most 4 P/G TSVs. Out of the 15 possible configurations, the TSV-placement techniques will pick the one resulting in the lowest IR-drop.

S2: The other category of PDN design techniques attempts to minimize the IR-drop by optimizing the sizes of P/G TSVs [17], while the placement and the total number of P/G TSVs is considered to be constant. For instance, in our example we can fix a single TSV in a specific node (e.g., 4th position in our case as shown in Fig. 3(b)), and then vary the size of the TSV from 5 μm to 20 μm.

Shortcomings of the techniques S1 & S2: In the aforementioned conventional PDN design methods, the optimizations of the TSV-placement and TSV-sizing are performed independently. However, there is a strong interdependence between these two phases. For example, it is impossible to judge without detailed knowledge if it is better to use 10

TABLE I
MOTIVATIONAL EXAMPLE

S1: TSV-placement [14]		
average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs
1.24	31400	100
S2: TSV-sizing [17]		
average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs
1.22	31301.9	200
Proposed method: simultaneous co-optimization of location, total number of size		
average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs
1.19	31400	133

"small" TSVs or 5 "large" ones. Therefore, it is necessary to combine the two optimization steps, which is ignored in existing methods. Moreover, since P/G TSVs occupy a considerable portion of chip real estate, it is impossible to insert too many P/G TSVs into the power grid, which would cause routing problems. The typical size of a via-first TSV ranges from 1 μm to 5 μm, whereas that of via-last TSVs ranges from 5 μm to 20 μm [18]. As a result, a P/G TSV diameter is larger than a standard cell height. Hence, it is inevitable that a single power (ground) TSV covers the region that ground (power) nets are supposed to be routed in. Thus, ground (power) nets should detour power (ground) TSV in order to avoid shorts between power and ground, which is an additional source of routing congestion. Therefore, the total area of TSVs, which depends on the numbers and sizes of TSVs, should be limited.

Our novel idea and a real example: *In our work, we consider and optimize the placement, the total number and the sizing of the P/G TSVs simultaneously*. Moreover, the limited total area of TSVs will be also taken into account. To illustrate the necessity and the advantages of such an approach compared to the traditional TSV planning techniques S1 and S2, let us take the b19 benchmark circuit (taken from the ITC'99 benchmark suite) with a 10×10 PDN as a motivational example. As shown in Table I, our proposed method outperforms the traditional TSV planning techniques in terms of IR-drop. It reduces the IR-drop by 4.2% and 2.5% compared to TSV-placement and TSV-sizing, respectively. At the same time our envisioned method does not come with a higher area demand than the classical TSV-placement and compared to the TSV-sizing approach, our technique requires fewer TSVs. Hence, the routing complexity using our method will not increase.

IV. MILP-based Method

In this section, we present our MILP optimization approach to minimize the average IR-drop by the co-optimization of the locations, sizes and the number of P/G TSVs. We have chosen an MILP-based technique, as MILP can extract feasible solutions in a short amount of time and can also handle the complex co-optimization of TSV sizing and placement in a single optimization step. Therefore, the objective function is

$$\text{Minimize} \left\{ \quad V_{drop_{avg}} = \frac{\sum_{i=1}^{N}(V_{DD} - V_i)}{N} \right\}, \tag{5}$$

where N is the number of nodes in the power grid, and V_i is the effective supply voltage seen at node i. The average IR-drop is chosen as optimization target in this work in order to minimize the effect of IR-drop on the circuit delay [19]. Since supply voltage V_{DD} and N are constants, the objective function for our MILP optimization is equal to

$$\text{Maximize} \quad \sum_{i=1}^{N} V_i. \tag{6}$$

To solve this optimization problem, the conductance matrix G, with $GV = I$, needs to be known according to Equation (1).

Therefore, we use the following equations to express the conductance for each possible TSV position i:

$$\begin{aligned} g_{tsv_i} = g_1 x_{i1} + g_2 x_{i2} + ... + g_n x_{in} \quad (i = 1, 2, ...M) \\ x_{i1} + x_{i2} + ... + x_{in} \leq 1 \\ x_i \in \{0, 1\} \, . \end{aligned} \tag{7}$$

n represents the number of different TSV sizes available for the design and hence x_{ij} is an indicator function showing if size j is used by the TSV placed at position i. Accordingly $g_{tsv_i} = 0$, if no TSV is placed at position i and $g_{tsv_i} = g_j$, if the TSV at location i uses the jth size option. For all size options the corresponding conductance values $g_1, \dots, g_n$ are calculated using Equation (4) for a single P/G TSV. Furthermore, M is the number of possible TSV positions, which is equal to

$$M = \frac{(L-1)\,N}{N}, \tag{8}$$

where L is the number of layers of the 3D-IC.

After extracting the conductance expressions for all the TSVs, Equation (3) can be formulated and based on this we can get the 3D conductance matrix G_{3D} from Equation (2) as well as the linear system $G_{3D}V = I$ with the independent current vector I. Instead of solving this linear system, which is very time-consuming, we use the equations in the linear system directly as constraints for our MILP optimization. For the sth equation in the linear system, we get the following constraint:

$$\sum_{t=1}^{N} G_{3D_{st}} V_t = I_s \tag{9}$$

Due to the structure of G_{3D}, there are some nonlinear terms in Equation (9), which have the following structure:

$$g_{tsv_m} V_t = g_1 x_{m1} V_t + g_2 x_{m2} V_t + ... + g_n x_{mn} V_t \tag{10}$$

In Equation (10), both x_m and V_t are variables. For these nonlinear constraints in which the products of variables are incorporated, we have to linearize them first. In general, a product of two variables can be replaced by one new variable, on which a number of constraints is imposed. In this work, considering the binary variable x_m and the continuous variable V_t (for which $0 \leq V_t \leq u$), their product, $x_m V_t$, can be replaced by an additional continuous variable $y = x_m V_t$. The following constraints force y to take the value of $x_m V_t$:

$$\begin{aligned} y &\leq u x_m \\ y &\leq V_t \\ y &\geq V_t - u(1 - x_m) \\ y &\geq 0 \end{aligned} \tag{11}$$

Another constraint comes from the limited total area of P/G TSVs. As explained in Section III, if the total area of P/G TSVs increases, routing congestion may occur and the total chip area may increase. Thus, the total area of inserted P/G TSVs should be limited. Therefore, the following constraint is used:

$$A = \sum_{i=1}^{M} A_i x_i \leq k A_{TSV_{max}} \quad \text{with} \quad 0 < k \leq 1, \tag{12}$$

where A_i is the area of the TSV at position i, and A is the total area of all inserted P/G TSVs. $A_{TSV_{max}}$ is the maximum possible total area of P/G TSVs, which can be obtained by inserting the biggest TSV into all possible locations. For different 3D-IC designs just k needs be adjusted to satisfy the constraint of the total TSV area.

For each node in the 3D PDN, we also set a constraint for the IR-drop, which is given as:

$$\begin{aligned} &V_t \leq V_{DD} \\ &V_t \geq (1-d)V_{DD} \quad (0 < d < 1)\, . \end{aligned} \tag{13}$$

These constraints are based on the assumption that the circuit block near the node t cannot work properly, if the voltage supplied to that node has an IR-drop larger than dV_{DD}. It is worth to note that k and d are user-defined values, i.e., these can be adjusted by the designers to set the appropriate constraints for the particular 3D circuit design.

In summary, to solve the objective function given in Equation (6) an MILP approach is used with the constraints detailed in Equations (9), (11), (12) and (13).

A. Scalability

Scalability is always a critical issue for LP-based methods. However, our approach offers a very good scaling behavior for circuits with increasing gate count as we explain below.

Suppose we consider a 2D circuit with the number of gates N_{gate}, and we partition it into an L-layer 3D-IC. For each layer, the number of gates is roughly N_{gate}/L. Assuming that each node in the power grid can drive at most s gates at most, the number of possible P/G TSV positions, N_{TSV}, is equal to

$$N_{TSV} = \frac{(L-1)}{L} \frac{N_{gate}}{s}. \tag{14}$$

Hence, the number of P/G TSVs scales linearly with the number of gates. In addition, the number of total variables N_{var} in the model is equal to

$$N_{var} = [(n+6)\frac{(L-1)}{L} + 1]\frac{N_{gate}}{s}, \tag{15}$$

where n is the number of size options of P/G TSVs. So the number of total variables also scales linearly with the number of gates. Thus, we can expect a good scalability of our method for larger circuits.

V. Experimental Results

A. Experimental Setup and Flow

Fig. 4 shows the flow of the proposed MILP-based approach to minimize the average IR-drop in 3D-ICs. The experiments are conducted on benchmarks circuit selected from the IWLS 2005 benchmark suite [20] using the Nangate 45nm library [21]. The experiments were performed on a server with four AMD Opteron 6174 and 256GB RAM. In this work, we assume that a via-last approach is used in 3D-ICs fabrication, in which routing issues are more severe compared to the via-first approach. Furthermore, we consider three different P/G TSV sizes: $5\mu m$, $10\mu m$, and $20\mu m$ [18].

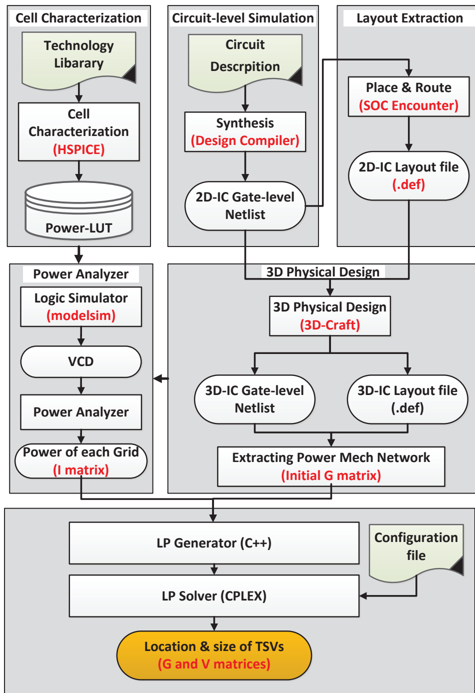


Fig. 4. The detailed flow of the proposed methodology

As shown in Fig. 4, first, all standard cells in the library are characterized using accurate SPICE simulations to obtain the corresponding leakage and dynamic power. This information is then stored in Look-Up-Tables (LUTs). Next, the gate-level netlist and the layout file of the 2D-IC are extracted using Synopsys DesignCompiler and Cadence SoC Encounter, respectively. The UCLA 3D physical design flow is exploited to convert the 2D-IC into a 3D-IC [22]. From the 3D gate-level netlist and layout file, we can obtain the exact location of each gate in a certain power tile in each layer. In the next step, the 3D gate-level netlist, the 3D layout file and the leakage/dynamic power LUTs are used to calculate the independent current vector I in Equation (1). Afterwards, the conductance matrix G in Equation (1) is constructed using Equation (2). Finally, an LP format is generator with the procedure explained in Section IV and CPLEX [23], an LP solver, is used to obtain the optimal locations, sizes and total number of P/G TSVs resulting in a minimum total IR-drop while satisfying a given area constraint for the total TSV area.

B. Co-optimization of TSV-placement and TSV-sizing

To illustrate the effectiveness of our proposed approach compared to conventional techniques, in which TSV-placement and TSV-sizing are optimized independently, we investigated a three-layer 10×10 power grid on four different benchmark circuits b17, b18, b22 and aes_core. For a three-layer 10×10 power grid, there are 300 nodes in the power grid and 200 possible positions to insert the P/G TSVs. Without loss of generality, we set the limited area parameter $k = 0.5$, which means that the total area of TSVs should be no more than 50% of the maximum possible total area of TSVs A_{max}. Here, A_{max} is equal to $200 \times \pi \times (10\mu m)^2$.

Table II compares the results obtained from our proposed co-optimization technique compared to TSV-placement [14] and TSV-sizing [17] techniques. From the result, we can conclude that the proposed method reduces the average IR-drop better than the method that only considers placement. For the benchmark B18, although the reduction of IR-drop is smaller compared with other cases, the total TSV area is reduced, which is beneficial for the routing. Compared to the approach which only optimizes the TSV size our proposed approach is also superior in terms of IR-drop. Although the differences are smaller, the total number of TSVs can be significantly reduced with our technique, which again is favorable from the routing perspective. In addition, also the fabrication costs will benefit, due to the lower complexity of the interconnect design. Therefore, considering these factors comprehensively, the proposed method can decrease the average IR-drop with minimum cost. However, the price is an increases solution time (for the optimization problem).

Please note that for larger problem sizes, a divide-and-conquer approach [24] can be used with the proposed method to improve runtime. Therefore, the original PDN is first mapped to a coarse grid. Afterwards, this small problem is solved and the solution is mapped back to the original problem through interpolation.

C. Accuracy and Runtime

Table III shows the results of the proposed MILP-based method in comparison with a random search (RS) method. For each benchmark circuit, we used four different sizes of power grid to partition the chip: 10×10, 15×15, 20×20, and 25×25. The limited total area of TSVs is also taken into account. We take the limited area parameter k as variable, and shift it from 1 to 0.1. For each benchmark circuit, RS simulations are performed for 10,000 different random P/G TSVs plans. The minimum value of the average IR-drop obtained by RS is chosen and compared with the result obtained using the proposed method. As shown in this table, the proposed technique can obtain significantly smaller IR-drop values (7.1% to 17.9%) within a much shorter time compared to RS (upto 29x improvement). These results also show that Monte-Carlo simulations are not feasible to solve the optimization problem, since these would consume even

TABLE II
COMPARISON WITH PREVIOUS TECHNIQUES

	TSV-placement [14] (fixed size=20μm, fixed number=100)			
	average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs	runtime $[s]$
b17	1.76	31400	100	11.40
b18	7.87	31400	100	12.10
b22	1.24	31400	100	10.00
aes_core	1.15	31400	100	8.93
	TSV-sizing [17] (fixed places, fixed number=200)			
	average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs	runtime $[s]$
b17	1.74	23412.6	200	19.83
b18	7.77	30830.9	200	168.57
b22	1.22	31301.9	200	8.39
aes_core	1.12	28652.5	200	8.27
	Proposed Method			
	average IR-drop $[mV]$	total area of TSVs $[\mu m^2]$	number of TSVs	runtime $[s]$
b17	1.70	31400	118	43.16
b18	7.77	31164.5	124	163.53
b22	1.19	31400	133	38.20
aes_core	1.05	31400	145	27.86

TABLE III
COMPARISON OF THE PROPOSED METHOD (MILP) WITH A RANDOM SEARCH (RS) IN TERMS OF IR-DROP, AREA AND RUNTIME

Benchmark Circuit	# of Gates	PDN	# of $\text{TSV}_{\max}$	Average IR-drop $[mV]$								Average runtime $[s]$	
				$A \leq A_{\max}$		$A \leq 0.7A_{\max}$		$A \leq 0.4A_{\max}$		$A \leq 0.1A_{\max}$			
				MILP	RS	MILP	RS	MILP	RS	MILP	RS	MILP	RS
b17	37117	10×10	200	1.6883	1.8411	1.7103	1.8492	1.7460	1.9435	2.2470	2.4503	30.02	763.81
		15×15	450	1.2985	1.4825	1.3081	1.3781	1.3693	1.5799	1.8154	2.0485	197.28	3226.79
		20×20	800	1.0582	1.0751	1.0913	1.1405	1.1336	1.4326	1.2556	1.3478	393.25	15432.85
		25×25	1250	0.8980	1.0147	0.9779	1.0441	1.1089	1.3960	1.1726	1.2074	673.45	21678.91
b18	92048	10×10	200	7.7687	8.4184	7.8217	8.4328	7.8070	8.5104	8.5367	9.2761	54.92	2059.44
		15×15	450	5.8870	6.3855	6.8127	7.3972	5.9757	6.3471	6.6972	7.3827	160.86	9031.77
		20×20	800	4.9149	5.0262	5.0940	5.5173	5.6142	5.9257	6.4361	6.7273	287.34	12476.38
		25×25	1250	4.0397	4.1658	4.7238	5.1394	4.9173	5.3682	6.2375	6.5128	1413.82	49126.43
b22	28317	10×10	200	1.1613	1.3035	1.3287	1.3641	1.1917	1.2041	1.6103	1.7044	29.35	542.40
		15×15	450	0.9566	0.9761	0.9576	0.9799	0.9834	1.0937	1.0745	1.1362	162.37	2935.21
		20×20	800	0.5519	0.7619	0.6561	0.7035	0.8163	0.9871	0.9558	1.0351	211.62	3760.49
		25×25	1250	0.5150	0.6276	0.5609	0.6294	0.7416	0.9267	0.9235	0.9872	952.41	35682.59
aes_core	20795	10×10	200	1.0751	1.2466	1.2349	1.3963	1.2557	1.4531	1.4772	1.5035	15.71	457.92
		15×15	450	0.8473	0.9567	0.8731	0.9846	0.9041	0.9357	0.9341	0.9469	98.76	2056.30
		20×20	800	0.5034	0.6124	0.5367	0.6893	0.5671	0.7045	0.5935	0.7258	178.57	2583.97
		25×25	1250	0.4367	0.5692	0.4682	0.5874	0.4875	0.6320	0.5036	0.6431	861.24	24567.45

more time to reach an acceptable confidence-level.

VI. CONCLUSION

Recently, the development of 3D-ICs has been accelerated. Besides the benefits over conventional 2D-ICs, 3D-ICs also have many challenges associated with the reliable PDN design due the increasing power density compared to 2D-ICs. In 3D-ICs, P/G TSVs play a key role in the PDN. In order to enhance the DC power integrity (i.e., IR-drop), the P/G TSVs have to be planned carefully. Besides the placement of TSVs, their sizes can also have a non-negligible impact on the IR-drop of 3D-ICs, which is ignored in previous work. Moreover, due to the routing congestion issue, the total area of TSVs, which is related to the number and size of TSVs, should also be considered during the P/G TSVs planning. In this paper, a new MILP-based approach is proposed to solve this multi-dimensional optimization problem. To minimize the IR-drop, we co-optimize the locations, sizes and the total number of P/G TSVs simultaneously. According to our simulation results, the proposed method can handle these issues effectively. Compared to random simulations, the MILP-based approach can obtain a smaller minimum average IR-drop with a much smaller runtime.

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