P2M: A 2MPixel CMOS Image Sensor for Soft X-Ray Detection

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***Abstract*— High brilliance synchrotrons and Free Electron Lasers (FELs) require high performing detector systems to realise their full potential. High dynamic range, low noise and high frame rate are all of great importance. In this paper we describe the P2M CMOS sensor, designed for soft X-ray detection at such facilities. We refer to previous work on test devices demonstrating a noise of <16e-, a full well capacity of >5Me- and quantum efficiency of >80% at 400eV (and with good sensitivity even below this value). Initial test results on the first Front Side Illuminated (FSI) 2 Megapixel device are also presented, and an outline of future work is described.**

Keywords*— CMOS, PERCIVAL, Image Sensor, Soft X-ray, PTC, Column-parallel ADC

I. INTRODUCTION

Detector systems for modern X-ray sources (such as 3rd generation synchrotrons and FELs) have high specifications, which have continued to grow as the capabilities of these machines have increased. Brilliance in particular has risen considerably [1], requiring detectors with very high dynamic range or full well capabilities to cope with peak signals. Achieving a high dynamic range however, must not come at the cost of good noise performance, which is required to allow the detection of signals down to the level of a single X-ray photon. Modern synchrotrons and FELs also have high repetition rates, requiring high frame rates from the equivalent detectors. Large area coverage is also required, which brings challenges in both reading out a larger sensor at high speed, and in delivering good production yield for large sensors. In this paper, we describe a sensor designed to meet these needs.

II. SPECIFICATIONS

To meet the requirements outlined in the introduction, our goal was to design a sensor with the specifications in Table I.

TABLE I. TARGET SPECIFICATIONS

Target Specifications		
Specification	***Unit***	***Value***
Noise	e-	15
Full Well	Me-	5
Frame Rate	fps	120
Energy Range	eV	250 - 1000
Quantum Efficiency	%	>80
Output	N/A	Fully Digital

III. SYSTEM OVERVIEW

A complex detector system such as this is built from many components. In this paper we will focus mainly on the CMOS sensor itself, but it should be noted that this is controlled and read out by a complex camera system as shown in Figure 1.

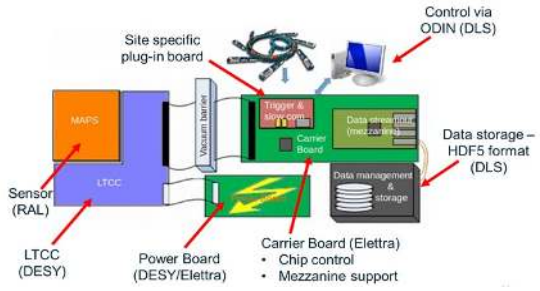

Fig. 1. The PERCIVAL Camera System

The camera system is comprised of the following components:

- A supporting circuit board for the sensor
- A power board which generates power supplies and biases

- A carrier board which provides control signals and reads out data through a plug-in "mezzanine board"
- Data storage and control though the ODIN Data Acquisition (DAQ) system.

IV. Sensor Overview

A top-level overview of the sensor is shown in Figure 2.

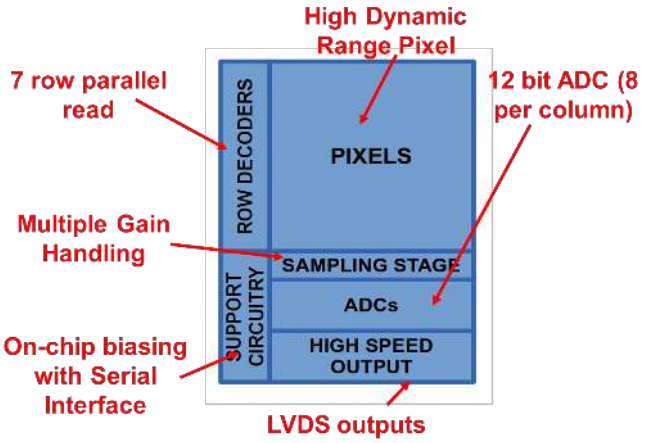

Fig. 2. The PERCIVAL Sensor

As can be seen from the diagram, the sensor is composed of the following components:

- A High Dynamic Range Pixel of the Lateral Overflow (LOFIC) type [2].
- Circuitry which permits seven rows to be read in parallel to allow high frame rates to be achieved.
- A "Multiple Gain Handling" block. This allows the sensor to determine which of the pixel's overflow capacitors contains useful data and only pass this data to the ADC.
- A dual-slope ADC for data conversion.
- A high speed serialiser for data output. This also contains an LVDS line driver.

Some of these blocks are described in more detail in the following section.

V. Circuit Details

In this section we provide some details of the various circuit blocks in the sensor.

A. Pixel

The pixel is of the LOFIC type as shown in Figure 3. C0 is chosen to be larger than the diode capacitance and C1 to be larger than C0.

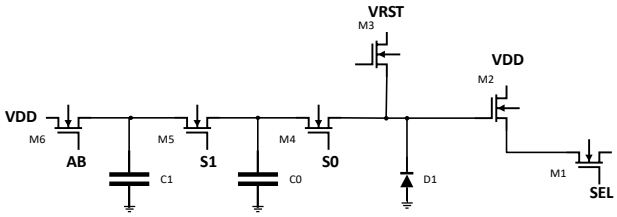

Fig. 3. The PERCIVAL pixel

In operation, the diode, C0 and C1 are reset to VRST using the transistor M3. M4 and M5 are biased near their threshold voltage. When illuminated, photo-generated charge carriers accumulate on the diode, reducing its voltage. Once the diode voltage has fallen low enough to turn on M4, further photo-generated carriers reduce the voltage on C0. Once illumination is complete, each diode and capacitor can be read out in turn. This allows small signals (which accumulate only on the diode) to be read out with a high conversion gain (and hence low read noise), whilst large signals can still be accumulated on larger capacitors, leading to a high dynamic range.

Further improvement in noise performance for the high conversion gain mode is achieved by making use of Correlated Double Sampling (CDS). This removes kTC noise introduced when resetting the pixel. This is done by reading the pixel value after reset, and again after the signal has been collected. Subtracting these values cancels the kTC noise. This technique is only effective when reading in high conversion gain mode, as reading twice increases the noise contribution from the readout chain to the total noise by a factor of $\sqrt{2}$. In high conversion gain mode, the input referred effect of this is less than the removed kTC noise, so a net benefit is achieved. For lower conversion gains, the extra readout noise contribution dominates the removed kTC noise, leading to no net gain.

B. Multiple Gain Handling

Having accumulated charges in this manner, it is necessary to determine which of the set of diodes and capacitors is non-saturated and thus contains information to be passed to the ADC. This is done by reading each of the Diode, C0 and C1 in turn, and then using a comparator to compare each to a threshold. The first which is above threshold is determined to be non-saturated and is passed to the ADC for conversion as shown in Figure 4. Each of the pixel gains is coded as a two bit binary value, and the value corresponding to the selected gain is stored and output together with the result of the ADC conversion so that the DAQ system is aware which gain has been selected. The sampling stage also contains a Programmable Gain Amplifier (PGA) to reduce input referred noise from the ADC.

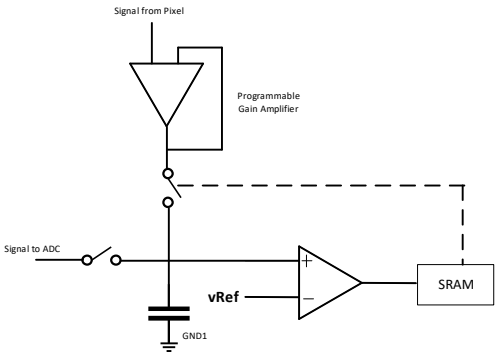

Fig. 4. Multiple Gain Handling Circuitry

C. ADC

The ADC is a dual-slope type, which performs a 5 bit coarse conversion followed by an 8 bit fine conversion leading to a 13 bit overall result. The schematic is shown in Figure 5

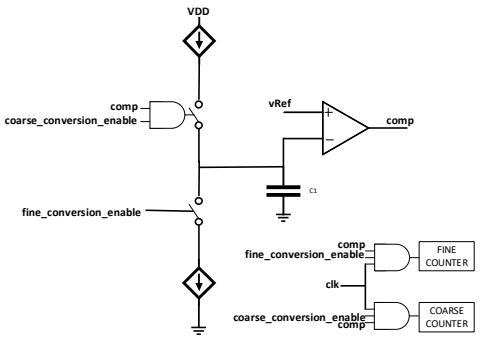

Fig. 5. ADC schematic

When performing an ADC conversion, the ADC is first put in coarse conversion mode, and a switched current charges the sample in large discrete steps until a threshold is reached. The fine phase is then started, and a smaller current is used to discharge the sample node until the threshold is again reached. During each phase, the charge and discharge are timed by a clock, which is used to clock a counter and generate the digital result. Figure 6 shows this process.

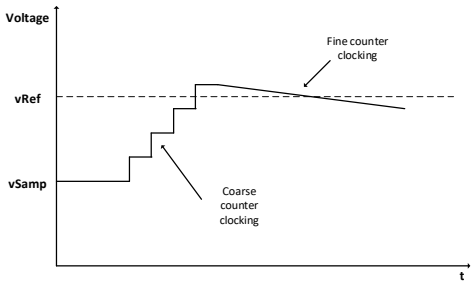

Fig. 6. Effect of ADC conversion phase on sampled voltage

D. High Speed Data Output

Data is transmitted off-chip by means of 45 LVDS data lines running at 420 Mbit/s Double Data Rate. Data is provided to the LVDS lines by means of a digital serialiser operated by a 240 MHz clock. This clock is generated from a slower input clock by means of a PLL, which steps up the input by 16x.

V. Sensor Performance

Several test structures were completed prior to the fabrication of a large scale device, and their performance has been previously reported [3]. The first 2 MPixel chips are now available and testing of Front Side Illuminated (FSI) devices is underway, with some results already reported [4]. Figure 7 shows an image of the device connected to its camera system and undergoing testing.

Fig. 7. The sensor mounted on the supporting LTCC and undergoing testing

Here we report some of the first results from this characterization.

A. ADC and PGA Testing

The readout chain can be tested independently from the pixel by holding the reset transistor M3 on. The PGA can be operated with a gain of 1, 4 or 6. The readout chain was tested in this manner, and Figure 8 shows some example output traces with the PGA in Gain 6 for several columns. Table II reports the results of the tests.

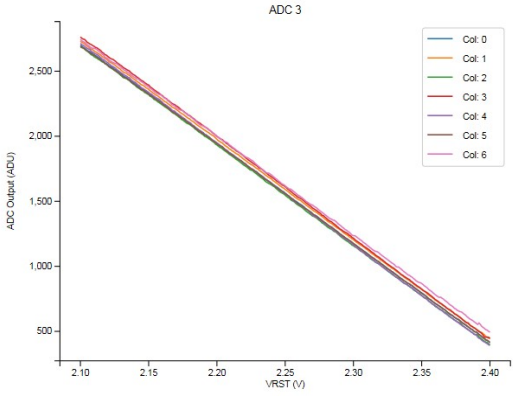

Fig. 8. Example ADC traces for a nominal PGA gain of 6

TABLE II. READOUT CHANNEL PERFORMANCE

Specification	*Unit*	*Gain 1*	*Gain 4*	*Gain 6*
Average Gain	V/V	-2050	-7775	-10943
Average Noise	uV rms	902	419	422

B. *Optical Testing by Photon Transfer Curve*

Following characterization of the readout chain, characterization of the pixel and optical response was undertaken by means of the Photon Transfer Curve (PTC) method. Characterization was first carried out for the diode with the PGA configured in Gain 1 and Gain 6. Gain 1 results are acquired without the use of Correlated Double Sampling (CDS) which, as explained previously, is only effective in the highest conversion gain mode. Gain 6 results use CDS. Results are reported in Table III.

TABLE III. HIGH COVERSION GAIN PERFORMANCE

Specification	*Unit*	*Value (PGA Bypass)*	*Value (PGA Gain 6)*
Maximum Full Well	ke-	53.7	6.6
Linear Full Well	ke-	52.5	4.7
Gain	ADU/e-	0.067	0.394
Noise	e-	49.8	15.9

These results give the performance from the high conversion gain part of the pixel. Testing has also been carried out on the low conversion gain section (i.e. the capacitors) and the results are reported in Table IV. These results are all taken with the PGA bypassed. The diode parameters were re-measured at the same time to allow easy comparison. From this table and Table III, the importance of the LOFIC system in achieving high dynamic range performance can be clearly seen. Low noise for low signals (where full well is unimportant) is achieved using the diode, and high full well for large signals (which are shot noise limited, so read noise is less important) is achieved with the capacitors.

TABLE IV. LOW CONVERSION GAIN PERFORMANCE

Specification	*Unit*	*Value (Diode)*	*Value (C0)*	*Value (C1)*
Gain	ADU/e-	0.059	6.12e-3	6.4e-4
Mean Noise	ADU	3.2	2.3	4.7
Mean Noise	e-	55.9	379	7350
Max Full Well	ADU	2988	3214	3321
Max Full Well	e-	51k	525k	5.2M

Figure 9 gives a visual illustration of the different sensitivities and capacities of the diode and the capacitors.

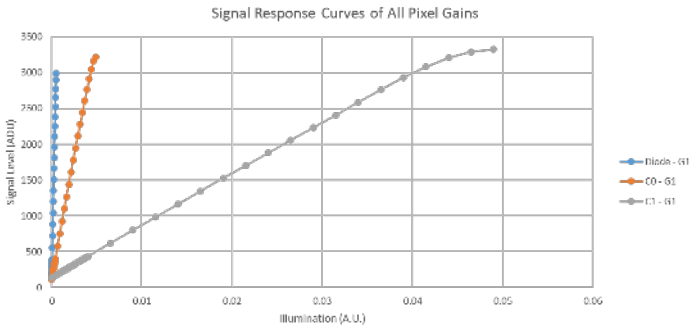

Fig. 9. Signal Response Curves for the Diode, C0 and C1

VI. ENERGY RANGE

The sensor will be back-thinned using the delta-doping process developed at the Jet Propulsion Laboratory (JPL) [5]. This process has already been performed for the test structures previously discussed, and a Charge Collection Efficiency of greater than 80% has been observed down to 400 eV. Even as low as 125 eV, a CCE of 51% has been measured [6].

VII. CONCULSIONS

In this paper, we have presented initial test results for the P2M FSI sensor and summarized previous testing on the energy range of the device. Future work will include demonstrating the full functionality of the gain switching architecture, optimisation of sensor performance and operation at higher frame rates. Backside processing for soft X-ray detection is also underway.

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