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Packaging and Antenna Integration for Silicon-Based Millimeter-Wave Phased Arrays: 5G and Beyond

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(Invited Paper)

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ABSTRACT This article reviews current research and development as well as future opportunities for packaging and antenna integration technologies for silicon-based millimeter-wave phased arrays in emerging communication applications. Implementations of state-of-the-art silicon-based phased arrays below 100 GHz are discussed, with emphasis on array architectures for scaling, antenna integration options, substrate materials and process, antenna design, and IC-package codesign. Opportunities and challenges to support phased array applications beyond 100 GHz are then presented, including emerging packaging architectures, interconnect characterization requirements, thermal management approaches, heterogeneous integration of multifunction chiplets, and novel antenna technologies.

INDEX TERMS 5G, cellular communication, mobile communication, antenna arrays, electronic packaging, thermal management, flip-chip devices, integrated circuit interconnections, integrated circuit packaging, millimeter wave communication, millimeter wave integrated circuits, multichip modules, phased arrays, phased array scaling, phased array antenna module.

I. INTRODUCTION

Mobile communication technologies have evolved significantly in the past several decades. Now fifth generation (5G) technology is being developed and deployed commercially to help meet emerging technology demands such as Artificial Intelligence (AI) at the edge and the Internet of Things (IoT). At the same time, research initiatives that aim to explore further evolution of wireless communications towards the sixth generation (6G) of mobile technology have started across industry and academia around the world [1], [2].

Frequency utilization of millimeter-wave bands and improved spectrum utilization are among the key attributes of 5G new radio (NR) technology. In this context, silicon-based phased array technology, with its ability to create complex electromagnetic interference patterns in space (a.k.a. beamforming and beamsteering [3]) using innovative RFIC and packaging solutions, is one of the key enabling technologies to support cost effective and power efficient designs at millimeter-wave frequencies. Most silicon-based millimeter-wave phased array demonstrations below 100 GHz have used printed circuit board (PCB), multilayer laminate package, LTCC, or quartz-on-silicon, as shown in the survey in Fig. 1.

On the regulatory front, as illustrated in Fig. 2, frequency bands up to 52.6 GHz are currently supported in 5G NR. There is a significant amount of aggregate bandwidth available, e.g., in frequency range 2 (FR2) that covers 24.25 GHz to 52.6 GHz. The available bands are expected to include higher frequencies (to approximately 100 GHz) in future releases, e.g., in frequency range 4 (FR4) which covers V-band and W-band. It is assumed that radio waves at frequencies up to approximately 300 GHz (in FR5) will be considered for 6G applications [1].

In order to achieve desired link margin using silicon-based hardware, a large number of antenna elements needs to be supported. Toward this end, multiple Si-based ICs are often

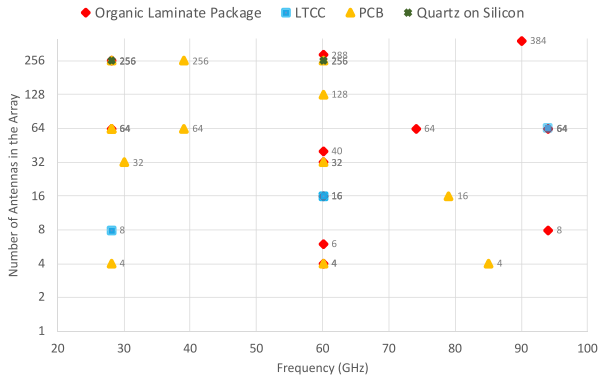


FIGURE 1. **A survey of substrate materials and process choices in recent silicon-based phased arrays below 100 GHz.**

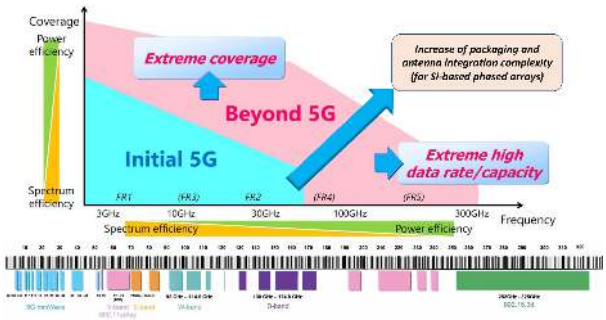


FIGURE 2. **Expansion of radio access technology with available bandwidth for 5G and beyond (modified from [1]).**

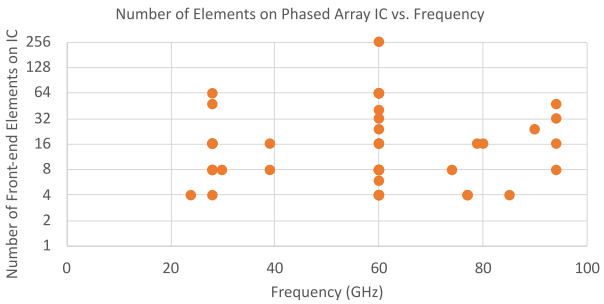


FIGURE 3. **Frequency popularity of recent silicon-based phased arrays at frequencies below 100 GHz [4].**

used in a modular fashion to control the antenna elements. The use of multiple ICs to scale the phased array to realize a larger antenna aperture is called phased array scaling [4]. With an appropriate scaling approach, the communication distance coverage can be extended to enable applications even beyond the requirements of current cellular systems (for e.g., satellite [5], [6]). Fig. 3 illustrates a recent survey of silicon (Si) RFIC-based phased array demonstrations using advanced CMOS and Silicon-Germanium (SiGe) technologies in the FR2 and FR4 bands at frequencies up to 100 GHz [4]. The number of front-end (FE) elements at the IC level ranges from 4 to 256. The applications are focused on FR2 for 5G NR (28 GHz, 39 GHz, etc.), the unlicensed V-band at 60 GHz, and E-band and W-band for radio backhaul and radar imaging applications.

TABLE I **Antenna Array Packaging Requirement and Implementation Functions**

Antenna Array Packaging Requirement	Functionalities
Impedance matching to IC at each port	Ensure sufficient power transfer to antenna
Radiate EM energy efficiently	Reduce interconnect loss in the package that impacts NF and EIRP
Feature low coupling between antenna elements	Coupling distorts radiation pattern and impedance matching. The effects are complex and potentially difficult to calibrate
Have equal signal delays between input ports and antenna feedlines, and equal radiation patterns among elements	Simplify calibration
Feature near-spherical radiation patterns	Overall array scanning angle is a function of individual array patterns
Feature sufficient layers for IC interconnects	Provide access to all IC inputs and outputs (including digital control) to the external world
Provide sufficient cooling to the ICs	Remove heat efficiently to keep device junction temperature under limit
Provide mechanical support to the ICs	It is crucial to prevent disassembly, disconnections ad mechanical fractures in the field
Feature low CTE mismatch with the ICs for mechanical stability over temperature	
Reliable mechanical connection to ICs and boards	

Table I summarizes key requirements for antenna array packaging and their corresponding performance-or system-driven objectives. The main challenges with respect to packaging include not only supporting co-design of the RFIC and antenna to ensure satisfactory antenna performance (i.e., bandwidth matching, radiation pattern, efficiency, etc.), but also thermal and mechanical integrity for reliability.

In this paper, we first review packaging and antenna integration work for Si-based phased array demonstration examples at frequencies below 100 GHz. In Section II, array architectures for scaling, substrate material and process, as well as co-design considerations between antenna and RFIC, are discussed in detail. Next, we discuss the challenges and opportunities for Si-based phased array packaging for frequencies beyond 100 GHz. Packaging concepts for supporting 2D arrays, trends in interconnect design and characterization, thermal management methods, heterogeneous integration of chiplets, and novel antenna technologies are described in Section III.

II. SILICON-BASED PHASED ARRAY INTEGRATION BELOW 100 GHZ

A. SI-BASED PHASED ARRAY ARCHITECTURES & PACKAGING OPTIONS

Beamforming can be performed in the RF, local oscillator (LO), intermediate frequency (IF), or digital domains [7]. Digital beamforming, with its ability to create simultaneous beams,[1] is becoming an attractive approach for phased arrays with fewer elements and low bandwidth in the FR1 bands below 7 GHz [10], [11]. For the FR2 and FR4 bands, the larger number of antennas (and corresponding frequency chains) and the larger bandwidth, makes digital beamforming expensive [12], [13]. Instead, RF beamforming or a combination of RF and IF beamforming is almost always used. Moreover, to support large numbers of antenna elements, phased array scaling with multiple Si-based ICs is employed [4], [14], [15]. The two popular beam forming architectures used in scaled phased arrays are (A) RF beamforming, and (B) a

[1]Note that other means to create simultaneous beams exist, using e.g. hybrid beamforming [8], and analog-FFT-based beamforming [9].

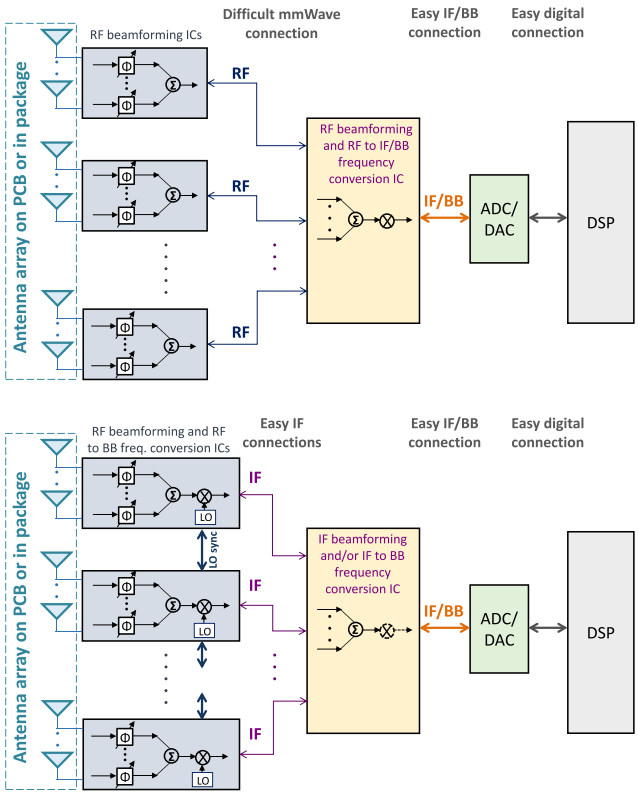


FIGURE 4. RF-beamforming and RF/IF-beamforming architectures for silicon-based phased array.

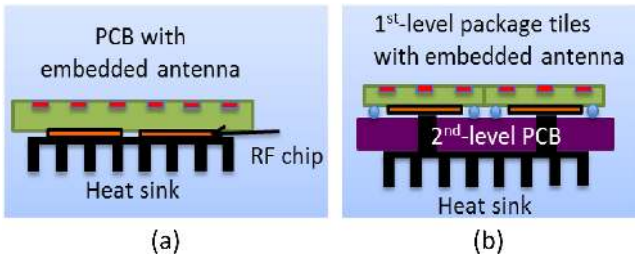


FIGURE 5. Antenna integration architectures: (a) antenna on PCB and (b) antenna in package.

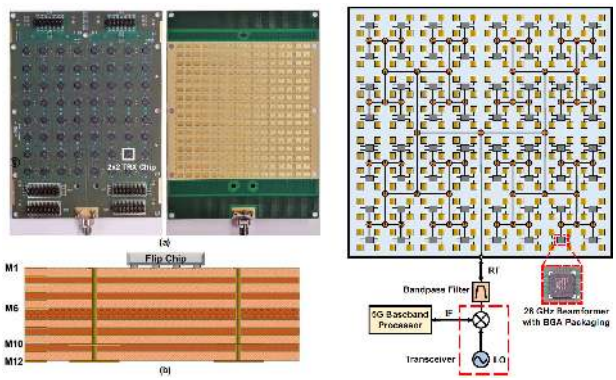


FIGURE 6. Implementation of a 28GHz antenna array with 256 antenna elements on PCB [16].

combination of RF and IF beamforming. (A) The exclusive RF beamforming architecture, an example of which is shown in Fig. 4, uses the least circuitry and includes the following functions: 1) RF phase shifting and combining/splitting, 2) frequency conversion, 3) analog-to-digital conversion, and 4) digital signal processing. These functions are often partitioned into a few different kinds of ICs to utilize the most appropriate process technology for each, as shown. One key challenge in this architecture is the need to route millimeter-wave signals in the package to connect the RF beamforming ICs with the frequency conversion IC, leading to the use of more expensive substrates. (B) The RF+IF domain beamforming architecture, an example of which is shown in Fig. 4, avoids millimeter-wave routing in the package, which enables the use of less expensive substrates. The architecture requires each beamforming IC to also up/down-convert the partially beamformed millimeter-wave signal to an IF. The much lower-frequency IF signals (typically 10 GHz and below) are then routed to an IF beamforming IC or on-board IF combiners. The ease of routing comes at the cost of additional on-chip circuitry (frequency converters in each beamforming IC) and the requirement for LO distribution and synchronization for the frequency conversion.

Si-based phased arrays at millimeter-wave frequencies require a tight antenna integration solution due to the spacing requirement between the antenna elements (typically half of the carrier signal wavelength). There are two major antenna implementation approaches to design antenna arrays. The first approach, referred as "antenna on PCB" as shown in Fig. 5(a), involves implementing antennas directly on the application PCB, an approach that potentially has the lowest cost. The RFICs, either in bare die form or prepackaged in a chip-scale or wafer-level fanout module, are bonded to the board on the side opposite the radiation direction. The second approach, referred as "antenna in package (AiP)" and illustrated in Fig. 5(b), includes implementing antennas on the first-level package. Together with flip-chip bonded ICs, the package forms an antenna array module. The module can be attached to a second-level PCB through ball-grid arrays (BGAs) to form a larger array. Next, several examples are described below to illustrate the two antenna packaging and integration approaches specifically for 28-GHz and 39-GHz 5G radio access applications.

Fig. 6 shows the block diagram and implementation of a PCB-based 256-antenna-element phased array from UCSD [16] using 4-channel packaged SiGe transceiver (TRX) beamformer ICs. The array, which supports RF beamforming and includes a Wilkinson power combiner network, is implemented on the PCB to combine the RF signals from beamformer ICs.

A 39-GHz phased array implementation (by Samsung) with antennas on PCB is shown in Fig. 7 [17]. For each 256-antenna sub-array, 16 CMOS-based 16-channel wafer-level packaged TRX chips are used. The array also supports RF

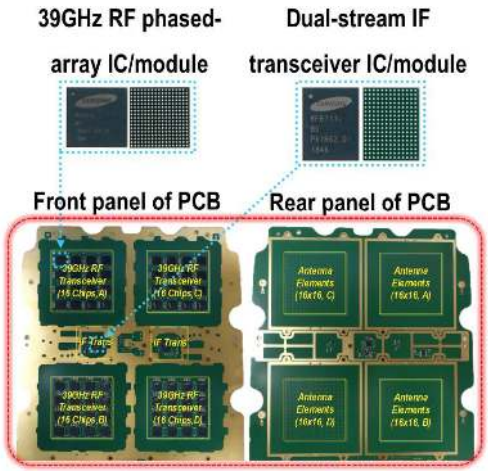


FIGURE 7. **Implementation of a 39 GHz antenna array with four subarrays of 256 antenna elements on PCB [17].**

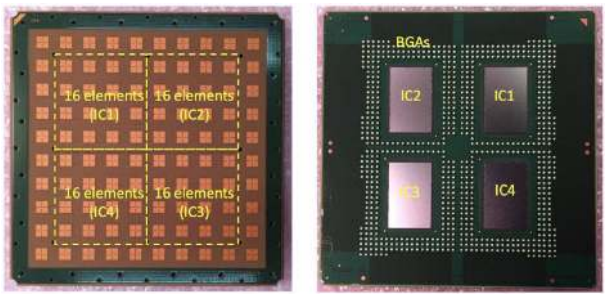


FIGURE 8. **Top and bottom views of 28-GHz phased array antenna module with antenna-in-package [19], [20].**

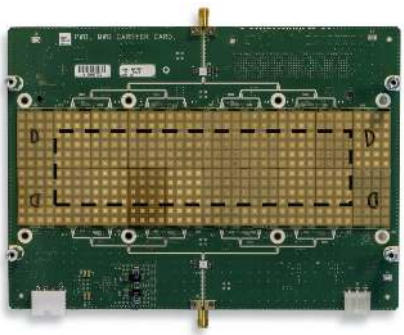


FIGURE 9. **Top view of tiled 28-GHz antenna-in-package modules on PCB [21].**

beamforming and includes an additional RF-to-IF frequency conversion IC for its baseband interface.

Fig. 8 illustrates a 28-GHz phased array antenna module that integrates 64 dual-polarized antenna elements in a package with four SiGe TRX RFICs (this was the first reported Si-based phased array demonstration for 5G) [18]–[20]. The array supports a 3-GHz IF interface to baseband as the frequency conversion and filtering functions are monolithically integrated in the RFIC.

Fig. 9 illustrates another example of applying an antenna-in-package solution to a 28-GHz scaled phased array demonstrated by Qualcomm [21]. In this case, 16 dual-polarized antennas are integrated in a unit package module. Sixteen such modules are tiled on a PCB to form a 256-antenna array. The array also uses IF beam forming with the combining tree implemented on the PCB.

B. SUBSTRATE MATERIAL AND PROCESS FOR PACKAGING

There is a wide variety of substrate technologies (in terms of materials and processes) that have the appropriate properties to integrate antennas and RFICs [22], including, but not limited to, conventional copper-clad PCB with low Dk (relative permittivity) and Df (loss tangent) dielectric, low temperature co-fired ceramic (LTCC), quartz-on-silicon, thin films on glass, wafer-level fan-out package, and multi-layer organic laminate (e.g., LCP package, build-up package, etc.). Selecting the right packaging substrate for antenna array implementation requires a holistic approach to analyze multiple factors (see Table I), including substrate layer count, interconnect types (e.g., via configuration), manufacturing tolerance (e.g., minimum trace width and spacing), electrical, thermal and mechanical properties of the dielectric, die mounting configuration (e.g. flip-chip vs. embedded), etc. For example, several representative cross-sections of different antenna and RFIC integration approaches are illustrated in Fig. 10.

C. ANTENNA AND RFIC CO-DESIGN CONSIDERATIONS

1) ANTENNA ELEMENT DESIGN AND OPTIMIZATION

In practical communication applications for which a millimeter-wave antenna array is implemented on PCB or in package, antenna performance needs to be optimized to achieve target gain, bandwidth, and radiation pattern. At the same time, antenna design must take into account not only substrate material properties and manufacturing process, but also system and circuit requirements driving the array size (i.e., the number of elements and spacing), and interconnect flexibility (e.g., for wiring power supplies and control signals), all while considerating thermo-mechanical compatibility, IC assembly, and board integration constraints. Antenna structures that can be easily integrated on PCB or in package include slot antennas [29], [30], grid antennas [31], magnetoelectric dipole antennas [32], Yagi antennas [33], dipole antennas [21], and variations of patch antennas [18], [21], [33]–[40] as shown in Fig. 11. However, for phased-array antennas used in many millimeter-wave applications, the aperture-coupled or probe-fed patch antenna is a preferred option since the antenna radiators and feed lines can be separated from each other by the antenna ground plane [36]. This arrangement advantage especially holds for aperture-coupled patch antennas. In this context, the antenna radiators and feed lines can be optimized almost independently. This feature is important since not only antenna feed line layout but also routing for many low-frequency signals and passive components (e.g., filters) must be taken into account in the design.

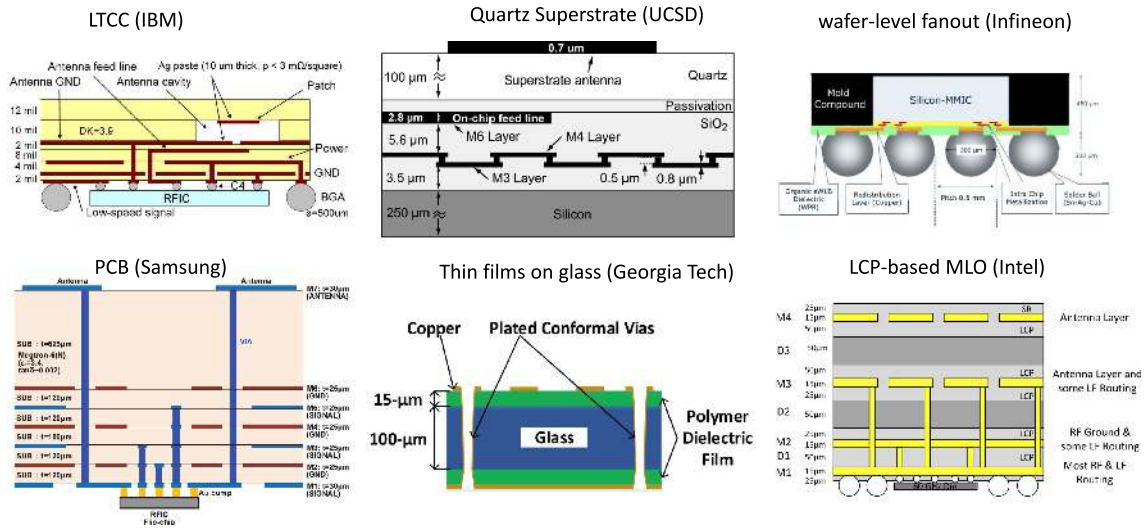


FIGURE 10. Cross-sections of various packaging substrates supporting millimeter-wave antenna integration [23]–[28].

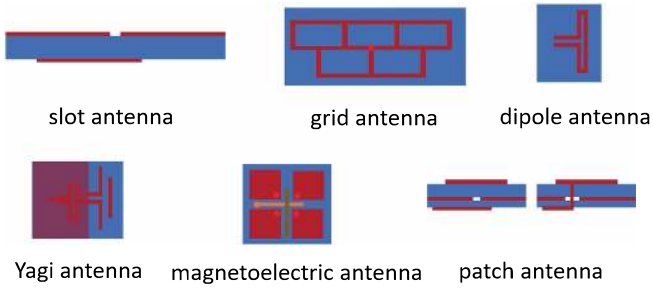


FIGURE 11. Different antenna types for phased array implementation.

For phased-array applications, front-end calibration should be simplified or even avoided (in principle) due to its complexity. Besides novel techniques in RFIC design such as phase and gain orthogonal control, reducing gain variation and antenna element coupling, and having equal feed line length are necessary to simplify or avoid requiring phased array calibration procedures [19], [20].

2) RFIC & ANTENNA CO-DESIGN EXAMPLES

In order to illustrate the importance of co-design among package, RFIC and antenna elements, two examples are provided below: (1) RFIC-package bump joint interface optimization and, (2) antenna feed line layout pattern design.

A three-dimensional (3D) electromagnetic model of a flip-chip bump interface on a 60-GHz phased array module is shown in Fig. 12 [41]. The geometries of the bump joint between the SiGe chip and multi-layered organic laminate package are parameterized within their manufacturing tolerance range, with parameters including transmission line width, pad size, pitch between adjacent signal and ground bumps, bump height and bump diameter. As shown by comparing the worst-case simulation result with the optimized simulation result, it is possible to improve the insertion loss of the transition by more than 2 dB.

Parameter	Best result	Worst result
Insertion Loss (dB)	0.34	2.43
T-line width (um)	125	75
Pad size (um)	70	100
Pitch (um)	250	150
Bump height (um)	90	90
Bump diameter (um)	60	120

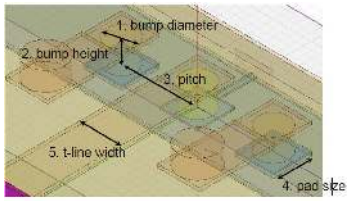


FIGURE 12. Modeling and optimization of a C4 flip-chip bump interface for 60GHz front-ends [41].

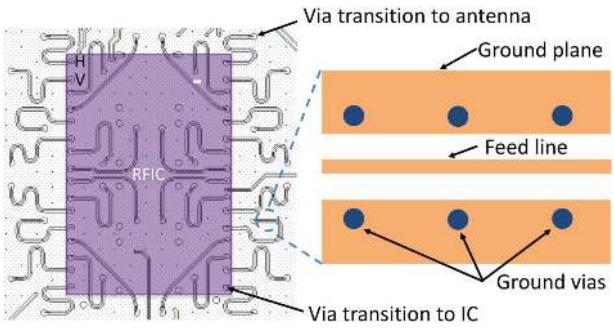


FIGURE 13. Example of a symmetrical 28-GHz antenna feed line fanout pattern inside the package [20].

A second example, shown in Fig. 13, illustrates a fan-out pattern of antenna feed lines from FE positions of a given RFIC inside a 28-GHz phased array antenna module [20]. All the antenna feed lines are length matched, which is important to ensure equal loss and phase responses across frequencies and therefore simplifies or even eliminates the need for front-end calibration. In this case, the feed lines are implemented using a stripline with ground plane on the same layer to further reduce the coupling between the RF signals.

3) ARRAY SCALING CONSIDERATIONS

It is well-known that for an N-element phased array, the effective isotropic radiated power (EIRP) in transmit mode scales as N^2 and signal-to-noise ratio in receive model scales as N. Scaling of the array is highly desired for not only enhancing performance (e.g., more range coverage), but also generating new system functions (e.g., more controlled simultaneous beams from sub-arrays).

At millimeter-wave frequencies below 100 GHz, phased array RFICs can be designed to be smaller in size than their corresponding antenna array.[2] This size relationship between the RFIC and the package enables direct scaling of the array, i.e., integrating multiple RFICs to create a larger antenna aperture, without sacrificing the number of active antenna elements that can fit in the array, a.k.a. antenna fill factor. Dense scaled arrays have been demonstrated with 100% antenna fill factor for two-dimensional (2D) arrays at 28 GHz [19]–[21], 39 GHz [17], [26], 60 GHz [42] and 94 GHz [43].

Besides antenna and RFIC co-design, other packaging aspects such as realizing the power distribution network (PDN), supporting digital control, and enabling successful thermal management, all need to be considered carefully in the context of array scaling. Specifically, it is desirable to have a PDN design that minimizes DC drop from BGAs to RFICs for each power domain, while suppressing any potential coupling to critical signals. The signal integrity of different topology options (e.g., multi-drop type or 1-to-N tree type) to support the required multiple digital buses needs to be evaluated carefully by simulation to achieve the best impedance match [4]. Despite its relatively low power density (e.g., < 22 W/cm^2 in the survey [4]) compared to III-V devices, a thermal solution sufficient to appropriately cool a Si-based RFIC die still requires system-level design consideration and trade-off analysis.[3]

At frequencies above 100 GHz, the size of the phased array RFIC becomes comparable to that of the antenna array. As a result, integrating antennas and packaging in the same footprint as the Si-based front-ends is significantly more challenging. Discussion of packaging concepts and of integration opportunities is provided in Section III.

III. PACKAGING AND INTEGRATION OPPORTUNITIES FOR APPLICATIONS ABOVE 100 GHZ

A. ANTENNA ARRAY PACKAGING CONCEPTS

Current design rules of PCB fabrication processes are unlikely to meet the requirements of integrating antenna arrays operating at frequencies beyond 100 GHz. For example, the standard trace width of a typical PCB process (around 75–100 μm) makes it difficult to route a sufficient number of signals and power where a half-wavelength spacing between antenna elements is 1.5 mm or less. Manufacturing tolerance, e.g., via registration, would make it even more challenging to keep antenna characteristics uniform across the array. Instead of antenna-on-PCB, antenna array packaging will involve integrating antennas in the package or even closer to the RFIC. Several feasible packaging concepts are illustrated and discussed below.

First, an antenna-in-package approach which has been recently demonstrated in an array operating in the W band [35], [39], [43] as illustrated in Fig. 14(a), can still be a viable solution in the D-band. In this case, silicon-based phased array ICs integrate key RF and digital functions monolithically and are then directly flip-chip attached to the package bottom surface.

In addition, this approach can be extended to include an interposer that supports hybrid phased array components that mix silicon chiplets and III-V chiplets, as shown in Fig. 14(b). Similar to packaging enabling the heterogeneous integration roadmap that is currently driving digital system packaging [44], the interposer layer supports finer bump pitch and denser interconnect connectivity that are beneficial to phased array integration.

A second packaging approach is to stack an antenna layer (e.g., implemented on quartz [42]) directly on the back side of a silicon-based phased array IC; this approach, referred to as a superstrate antenna, is shown in Fig. 14(c). Each monolithic integrated silicon chip also requires through-silicon vias (TSVs) for signal transmission and power delivery. The compact TSV-enabled RFICs can be tiled on a multi-layer carrier to form a scaled array. Due to the lack of direct heat dissipation opportunities as enabled in the antenna-in-package configuration, thermal management with efficient cooling will be one of the main challenges for this approach. As a result, considering a base substrate with a high heat conductivity such as AlN, plus thin-film-based (e.g., BCB) wiring layers, may be appropriate for this carrier choice.

Another alternative packaging approach is to integrate antennas on the multi-layer carrier directly as shown in Fig. 14(d). This approach can be applicable to hybrid phased arrays that involve silicon chiplets and III-V chiplets. In this case, selecting the right carrier substrate with appropriate dielectric and thermal properties is critical to delivering the performance of the antenna and interconnects while meeting overall cooling needs. It is worth noting that this approach is not ideal to support standard 2D array scaling (i.e., around $\lambda/2$ antenna spacing) since the antenna and front-end elements are placed laterally, an approach which is less area efficient than is vertical relative placement.

B. INTERCONNECTS

Interconnect performance is essential to ensure good impedance match and low insertion loss to achieve desired antenna efficiency. For operating frequencies over 100 GHz, it is feasible to design classic co-planar waveguide and transmission line structures with low-loss dielectric materials to achieve less than 1 dB/mm insertion loss [45]. For example, Fig. 15 plots measured microstrip insertion loss of about

[2]The array size is proportional to the antenna spacing in the order of one to several millimeters.

[3]Such analysis needs to consider, e.g., allocating areas on PCB for thermal via placement or cutout region for heat sink versus wiring flexibility for signals and power.

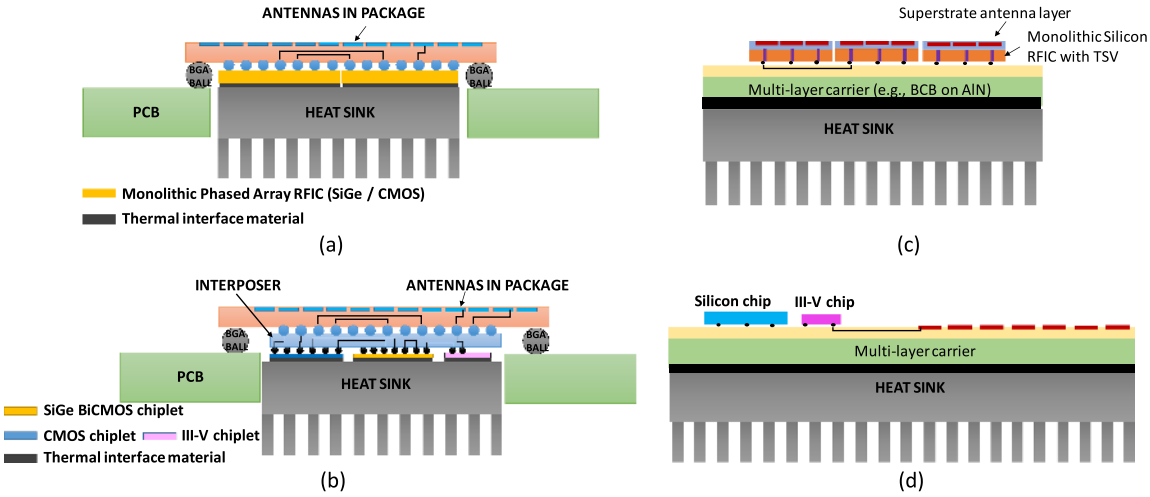


FIGURE 14. (a) Antenna-in-package implementation diagram with direct flip-chip attach of monolithic RFICs; (b) Antenna-in-package implementation with additional interposer for heterogeneous chiplets integration; (c) Superstrate antenna array concept with TSVs in monolithic RFIC over a multi-layer carrier; (d) Silicon and III-V chiplets on a multi-layer carrier with antennas.

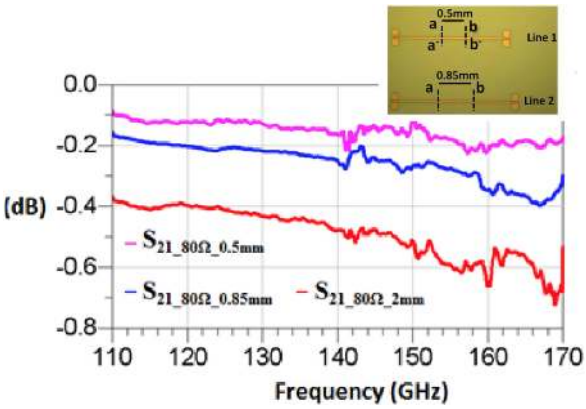


FIGURE 15. Insertion loss measurement of LCP-based microstrip in D-band [46].

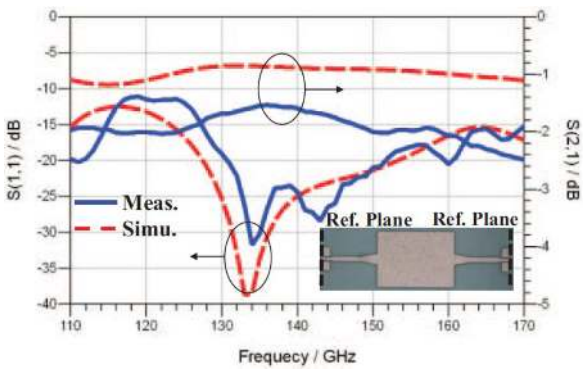


FIGURE 16. Insertion loss measurement of LCP-based SIW in D-band [47].

0.4 dB/mm up to 170 GHz using liquid crystal polymer (LCP) dielectric [46].

Substrate integrated waveguide (SIW) can also be leveraged to implement low-loss signal channels at these frequencies. Fig. 16 shows a measured SIW structure based on LCP substrate with insertion loss of 0.33 dB/mm in the D-band. The measurement data also demonstrates reduced surface roughness effects on the insertion loss, with an average of 0.35 dB/mm improvement [47] achieved.

TABLE II Electrical Properties of Dielectric Materials for Antenna and Interconnect

Substrate	Dk	Df	Reported Frequency
LCP	2.9 – 3.2	0.002 – 0.0045	30GHz – 110GHz
ABF dry-film buildup (GL102)	3.3	0.0044	5.8GHz
Borosilicate glass (e.g., Corning 7070)	4.1	0.002 – 0.003	10GHz – 50GHz
Fused Silica / Quartz	3.8	0.0001 – 0.0004	10GHz – 50GHz
BCB (liquid-based, e.g., DOW CYCLOTENE™ 3000/4000)	2.65	0.002	10GHz
Polyimide (for flexible substrate, e.g., DuPont Kapton HN 200)	3.31	0.011	10GHz

Table II lists several dielectric materials that have relative low Dk and Df values and are potentially suitable for interconnect implementation of phased array packaging. For example, fused silica and quartz have shown very low dielectric loss tangent up to 50 GHz which make them an excellent fit for the superstrate antenna layer as well as the signal routing layer of the base carrier. Notice that, other than LCP, interconnect characterization data of other materials at frequencies beyond 100 GHz is not readily available in the literature. This characterization data needs to be acquired, studied, and benchmarked carefully before system integration and design involving such materials takes place.

Regarding flip-chip bump interface to mount silicon chips [48], Fig. 17 illustrates the continuous evolution of bonding methods driven by digital applications [44]. Cu-pillar-based flip-chip bonding currently supports bump pitches of around 60 μm well. There are also thermal-compression based bonding methods in development that suggest a path to the use of Cu bump metallurgy and can be applied to even

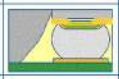
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level

FIGURE 17. Evolution of flip-chip bonding technologies [44].

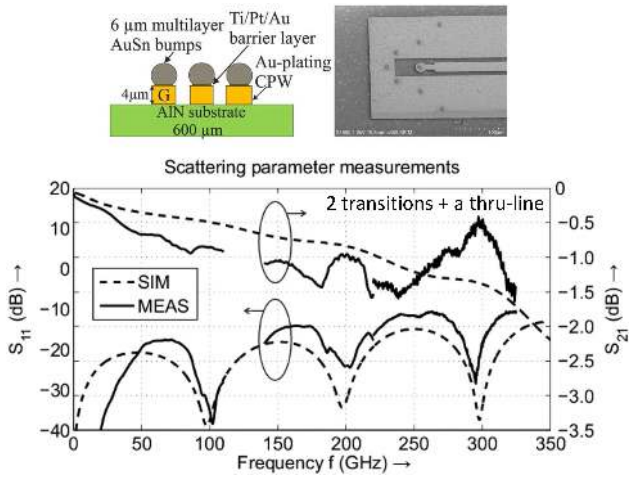


FIGURE 18. Flip-chip interconnect example for 250-GHz module [49].

smaller bump pitches for the heterogeneous integration of chiplets, including future phased array silicon chips.

For hybrid front-ends that include III-V chiplets, the use of solder balls or other interfaces that include solder compounds is less desirable. For this application, the bump interface ideally needs to be compatible with III-Vs that have Au interconnect. Fig. 18 illustrates a flip-chip interconnect example using AuSn microbumps that supports transition beyond 100 GHz up to 300 GHz [49]. Other reported insertion loss per transition from measurement data can achieve less than 1 dB at 500 GHz [50].

C. THERMAL MANAGEMENT

For Si-based phased-array RFICs beyond 100 GHz, chip power density numbers will likely increase to the range of tens of W/cm^2, significantly higher than that of designs operating below 100 GHz due to reductions in antenna spacing and overall chip size. For the antenna-in-package concept in Fig. 14(a) and Fig. 14(b), the chips are mounted on a package substrate opposite to the antenna aperture side. Depending on the actual heat dissipation, the heat from the chips can be removed using several cooling configurations with different degrees of complexity as shown in Fig. 19 [51]. The

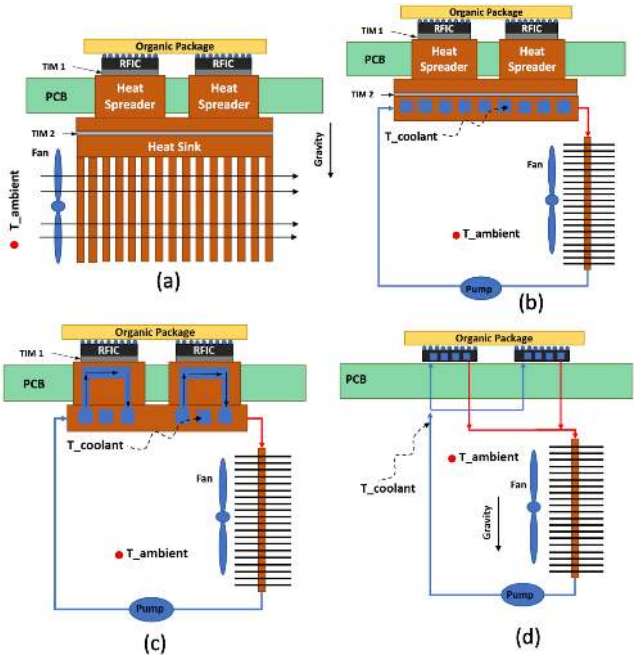


FIGURE 19. Cooling approaches for antenna array module: (a) forced air cooling; (b) and (c) liquid cooling; and (d) microfluidic cooling [51].

applicable cooling approaches include traditional forced air cooling, advanced pumped-liquid-cooling with a cold plate located at various distances from the chip, and next-generation chip-embedded microfluidic cooling configurations in which coolant fluid flows in microscopic channels etched on the chip.

For superstrate antenna array packaging in Fig. 14(c), having a TSV in the silicon chip not only brings signal and power directly out to the carrier, it also helps dissipate heat more efficiently. Here, it is worth reiterating the importance of minimizing thermal resistance of the carrier structure, particularly for the hybrid phased array packaging in Fig. 14(d). AlN ceramic substrate with heat conductivity around 300 W/m-K at 300 K can be a good choice in this context. Note further that AlN has thermal-expansion coefficient of $4.3 - 4.6 \times 10^{-6}/^{\circ}C$ that well matches that of silicon. It is also stable in inert atmospheres at temperatures over 2000 °C.

D. MULTI-FUNCTION CHIPLETS INTEGRATION

In this sub-section, we briefly review several additional package technologies that are driven by digital applications to support heterogeneous integration of multi-function chiplets. Such package technologies can also be explored to integrate silicon RFICs and antennas for phased array applications.

1) ORGANIC INTERPOSER PACKAGE

Fig. 20 and Fig. 21 illustrate two different types of organic interposer packages ("iTHOP" from Shinko [52] and "APX" from Kyocera [53]). In both cases, chip-to-chip interconnect bandwidth can be increased significantly as the technologies support less than 5 μm line/space design rules and bump pitch

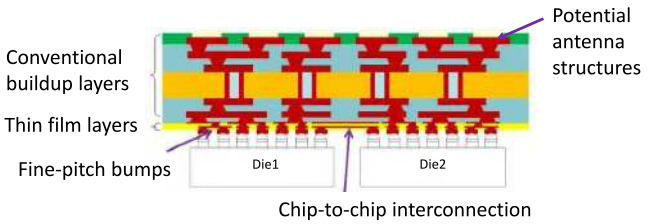


FIGURE 20. Modified illustration of organic interposer (i-THOP) cross-section from Shinko Electric Industries [52].

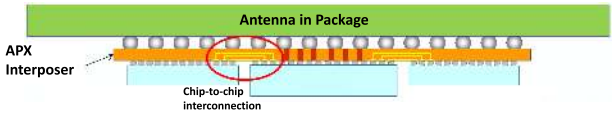


FIGURE 21. Modified illustration of APX organic interposer technology from Kyocera [53].

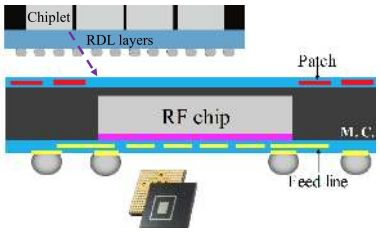


FIGURE 22. Illustration of INFO wafer-level fanout package for chiplet and antenna integration [54], [55].

as fine as 55 μm. Despite the fact that bandwidth is not necessarily the key driver and requirement for silicon-based phased arrays, the support of dense interconnect will benefit IC bump pitch and antenna array scaling that will be of particular value for arrays operating at frequencies beyond 100 GHz.

2) WAFER LEVEL PACKAGE

Wafer-level fanout technologies have undergone rapid development in recent years. Fig. 22 illustrates a conceptual diagram for one of the representative technologies (i.e., INFO process from TSMC) used to integrate multiple chiplets that are connected by a redistribution layer (RDL) with an ultra-fine pitch [54]. The INFO package has been demonstrated to integrate antenna elements recently for millimeter-wave applications [55]. Another wafer level packaging technology, eWLB, has been under development and shown to support antenna integration at frequencies beyond 100 GHz for radar imaging applications [56].

3) GLASS PACKAGE

Fig. 23 illustrates the cross-section of a glass-core based package that embeds an millimeter-wave chip inside a cavity [27], [57]. Low-loss thin film layers are deposited and patterned on both sides of the core layer to form an RDL with precision similar to that of a silicon back-of-the-line (BEOL) process. Enabled by thru-glass vias (TGVs), millimeter-wave antennas and passive components such as power combiners

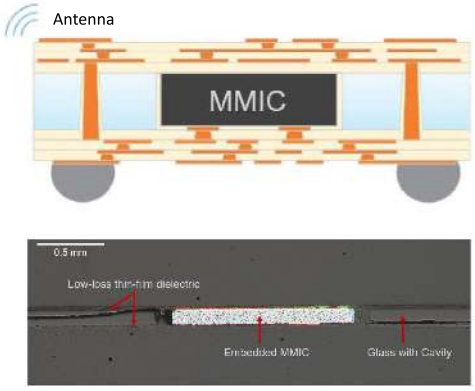


FIGURE 23. Illustration of glass-core package with embedded IC and antenna [57].

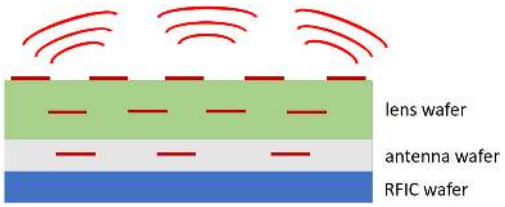


FIGURE 24. Illustration of antenna cross-section consisting of lens and antenna layers on top of RFIC using wafer-scale process.

and bandpass filters have been recently demonstrated [27]. Glass substrates also offer very good dimensional stability for large-panel processing which helps increase throughput and reduce manufacturing costs.

E. NOVEL ANTENNA TECHNOLOGIES

Since signal path-loss beyond 100 GHz is very severe,[4] large antenna arrays are necessary to compensate for the path loss. Designing such massive antenna arrays with high efficiency poses many challenges. It is important to optimize the system architecture to provide high dynamic range and high flexibility at a reasonable cost and power consumption.

Conventional PCB and package processes may not provide sufficient precision and tolerance to fabricate antennas at these frequencies, especially for operation beyond D-band. It is more likely that wafer-scale process will be required for fabrication in this case. Due to small antenna size, the antennas can be placed directly on the top metal layer of RFIC chip, or they can be fabricated on glass (or other material-based wafer) and then attached to an RFIC, as shown in Fig. 24; the bottom layer in the figure is the RFIC which contains all active and passive components. Antenna elements can be placed here if space permits. Otherwise if better antenna performance is desired, a separate antenna wafer can be used. To further improve antenna or array performance metrics such as gain

[4]Note that all electromagnetic waves travel losslessly through free space. The higher free space path loss at higher frequencies is due to the assumption that a smaller receive antenna will be used at higher frequencies. The higher free space path loss can be compensated using multiple (smaller) antennas to create an antenna array at high frequencies.

or beamforming capability, a lens wafer layer can be used. Such a lens layer can comprise 3D-printed semi-spherical silicon lenses, metamaterial-based lenses, or reconfigurable intelligent surfaces.

IV. CONCLUSION

Packaging integration of antenna array and scalable RFICs is one of the key enabling technologies to drive silicon-based millimeter-wave phased array development for many critical applications, including 5G and future 6G mobile communication systems. Recent demonstrations at frequencies below 100 GHz rely on RF and RF+IF domain beam-forming architectures and have explored the use of a variety of substrate technologies to integrate antennas, mainly involving antenna-on-PCB and antenna-in-package approaches. Looking ahead, there are tremendous new opportunities for research and development of silicon-based phased array packaging for arrays operating at frequencies beyond 100 GHz. Novel scaling architectures, interconnect, and antenna technologies, supported by heterogeneous integration of multi-function chiplets with efficient cooling capabilities, will be the cornerstones of future phased array systems that push silicon technologies to a new exciting era of directional beam-based communication and sensing. Beyond phased array front ends, we expect upcoming beamforming paradigms such as millimeter-wave digital beamforming [58] and software defined phased array beamforming [59], that currently rely on COTS components and have relatively large form factors, to be co-integrated in advanced system-on-package solutions in the future.

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