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PAD: A New Interactive Knowledge-Based Analog Design Approach

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Abstract. This paper presents a new **P**rocedural **A**nalog **D**esign tool called **PAD**. It is a chart-based design environment dedicated to the design of analog circuits aiming to optimize design and quality by finding good tradeoffs. This interactive tool allows step-by-step design of analog cells by using guidelines for each analog topology. Its interactive interface enables instantaneous visualization of design tradeoffs. At each step, the user modifies interactively one subset of design parameters and observes the effect on other circuit parameters. At the end, an optimized design is ready for simulation (verification and fine-tuning). The present version of PAD covers the design of basic analog structures (one transistor or groups of transistors) and the procedural design of transconductance amplifiers (OTAs) and different operational amplifier topologies. The basic analog structures' calculator embedded in PAD uses the complete set of equations of the EKV MOS model, which links the equations for weak and strong inversion in a continuous way [1, 2]. Furthermore, PAD provides a layout generator for matched substructures such as current mirrors, cascode stages and differential pairs.

Key Words: analog, CAD tools, knowledge-based, CMOS circuit design, systematic design

1. Introduction

Many CAD tools and environments have been proposed to facilitate the design task and increase circuit quality. At system-level, the design flow for mixed-mode circuits uses different methodologies to design and layout analog and digital parts (Fig. 1).

For digital circuitry, the design procedure can be strongly automated. It consists of: circuit specification, behavioral modeling, circuit synthesis, layout generation, layout extraction and post layout simulation. This design flow is capable today to automate digital functionalities from behavioral modeling to physical implementation without any transistor-level manipulation, therefore facilitating cells' retargeting and technologies' migration.

However, for analog functions, the design method depends strongly on the type of the circuit that has to be designed and needs a lot of knowledge at transistor level. CAD tools for analog design available in the market today do not provide circuit synthesis from the behavioral description. The problem of topology selection and circuit synthesis leads to transistor-level sizing. This makes the analog design procedure very complicated and automation without user optimization can be very restrictive. Therefore, retargeting and reuse of circuit topologies is not always possible and needs designer's intervention.

In the recent years, many behavioral simulator tools were proposed. They allow designers to simulate their systems at high level. Some of them (VHDL-AMS, VerilogA etc.) use a Spice-like netlist to simulate analog parts of mixed-mode circuits, therefore achieving behavioral and transistor level simulation.

The proposed PAD tool is dedicated to structured transistor-level design of analog cells. This chart-oriented design tool is very suitable for the design of analog circuits by optimizing design choices and by reducing efforts in determining tradeoffs. The best way to find an optimal solution is to combine both approaches: procedural analog design—transistor level simulation and behavioral simulation (Fig. 2). The two main purposes of the PAD tool are to reduce expert analog designer's development time and help to hand on analog knowledge toward system level designers. It

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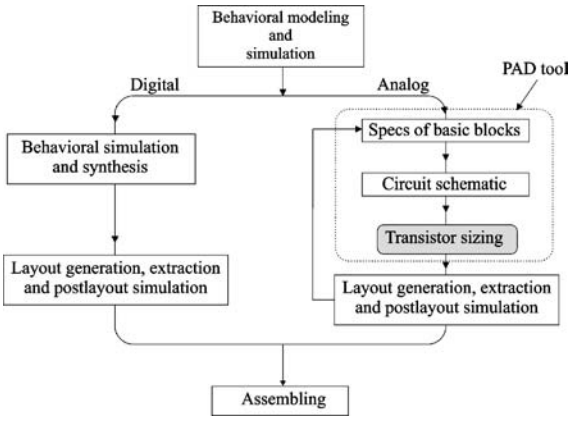

Fig. 1. Top down system design approach.

also facilitates migration of analog libraries from one technology to another.

2. PAD Structure

The PAD tool introduces a new interactive knowledge-based design methodology for analog structures' sizing and layout generation. It assists the user by presenting the necessary theoretical knowledge and tips from an experienced designer. Furthermore, its interactive interface allows instantaneous visualization of the design tradeoffs. The tool structure is illustrated in Fig. 3.

A transistor-level calculator, based on the complete set of equations of the EKV MOS model [1, 2], is capable of exploring complex relations and displays the results on charts, which the user can interact with. The EKV model is chosen because it is strongly based on device physics dedicated to the design of analog circuits. It links the equations for weak and strong inversion in a continuous way, has a small number of parameters and a very good accuracy. Moreover, it is possible to find solutions for different input parameter sets without using complex numerical methods. Large number of transistor parameters, which are important for analog design, can be extracted from the model, such as: inversion factor, saturation voltage, Spice-like threshold voltage, Early voltage, small signal parameters, parasitic capacitances, g_m/I_D ratio, transconductance efficiency factor.

The charts enable the transcription of mathematical relations into appropriate interactive graphical representations. The designer can change different parameters and observe simultaneously the behavior of the other parameters, since all dependencies and characteristics of an analog structure are presented at one glance. As a result, the design tradeoffs are easily found and the circuits can be optimized efficiently.

The analog structures' library relies on a transistor-level calculator and includes the most common basic blocks for the design of analog circuits. For each basic analog structure, the user-friendly graphical interface has the same appearance. All important design parameters are calculated and displayed. Furthermore, the guidelines and the basic design rules are presented to the user in a separate explanation window. The designer can analyze the parameters' dependencies of each basic structure, acquiring in this way an intuitive understanding of the structure's behavior.

The procedural design flow of complex analog structures is based on the partitioning of each complex

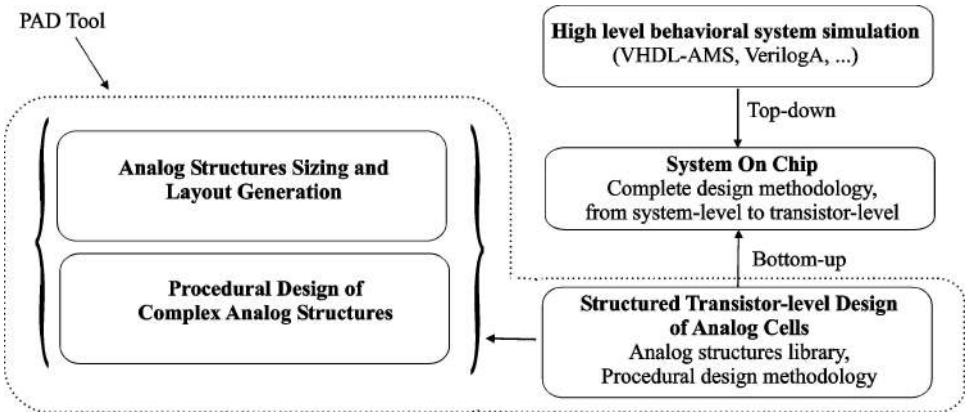

Fig. 2. SOC design methodology.

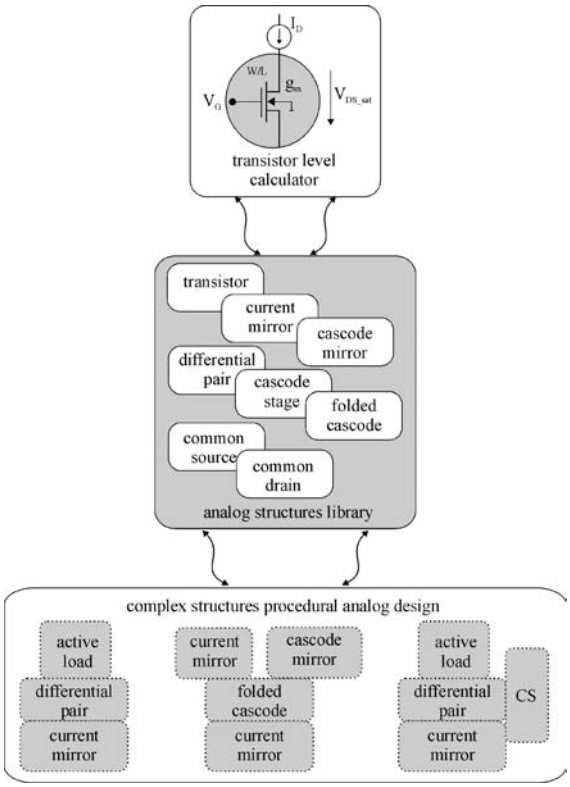

Fig. 3. PAD structure.

structure into basic analog structures. It covers the systematic design of different operational amplifier topologies, as well as the design of OTA followed by a common source/drain stage for power management applications. The design sequence for each analog topology is implemented in the form of a design scenario. The designer can navigate from one point to another through the scenario in order to modify the design at transistor level and reach the optimum cell performance.

3. Analog Structures Library

The analog structures library, embedded in PAD, includes basic analog structures such as: current mirror, differential pair, cascode stage, cascode current mirror, common source/common drain stage. This tool also allows the analysis of a single transistor (NMOS, PMOS) as a basic analog structure.

For each structure a set of general parameters (such as: small signal model parameters, DC biasing values, parasitic capacitances, equivalent noise, speed) is displayed. Some specific parameters are also shown (such as: maximum DC offset for differential pair, current mismatch for current mirror, input capacitance, output resistance, sum of parasitic capacitances in some specific nodes). This enables to analyze the basic structure's behavior in the environment of a given circuit, and to observe the parameters that are important for the design tradeoffs.

The proposed design procedure includes the choice of the g_m/I_D ratio as a measure of the translation of current into transconductance (g_m efficiency and consumption efficiency) [3, 4]. At the same time, the ratio indicating the device operating region (strong, moderate or weak) is shown. The first step is to set the priority targets (gain, noise, speed). According to this, the bias current is determined and the g_m/I_D ratio is chosen. As a result, the only variables to change are: transistor width W and transistor length L. Simultaneously, the changes of all other parameters can be observed. This methodology can be used for sizing, as well as for optimization and resizing of circuit blocks.

After successful sizing of a given analog structure, the tool helps the designer to automatically generate a matched layout (based on existing layout rules) in CIF format.

The snapshots of charts for basic analog structures sizing are shown in Fig. 4.

4. Complex Analog Structures Procedural Design

The current PAD tool version enables systematic design of operational transconductance amplifiers, such as: simple OTA, folded cascode OTA and different operational amplifier structures, such as Miller Op Amp.

The procedural analog design flow consists of: circuit partitioning into basic analog structures, chart-based basic analog structures sizing and circuit level design. The proposed design sequence guides the user through the design revealing the parameters' dependencies and the role of every basic analog structure in the circuit. During and after the design of every basic analog structure, the circuit performance parameters can be checked. The final circuit-level summary provides a complete documentation of the electrical behavior of the designed cell. At the end, an optimized design is ready for simulation.

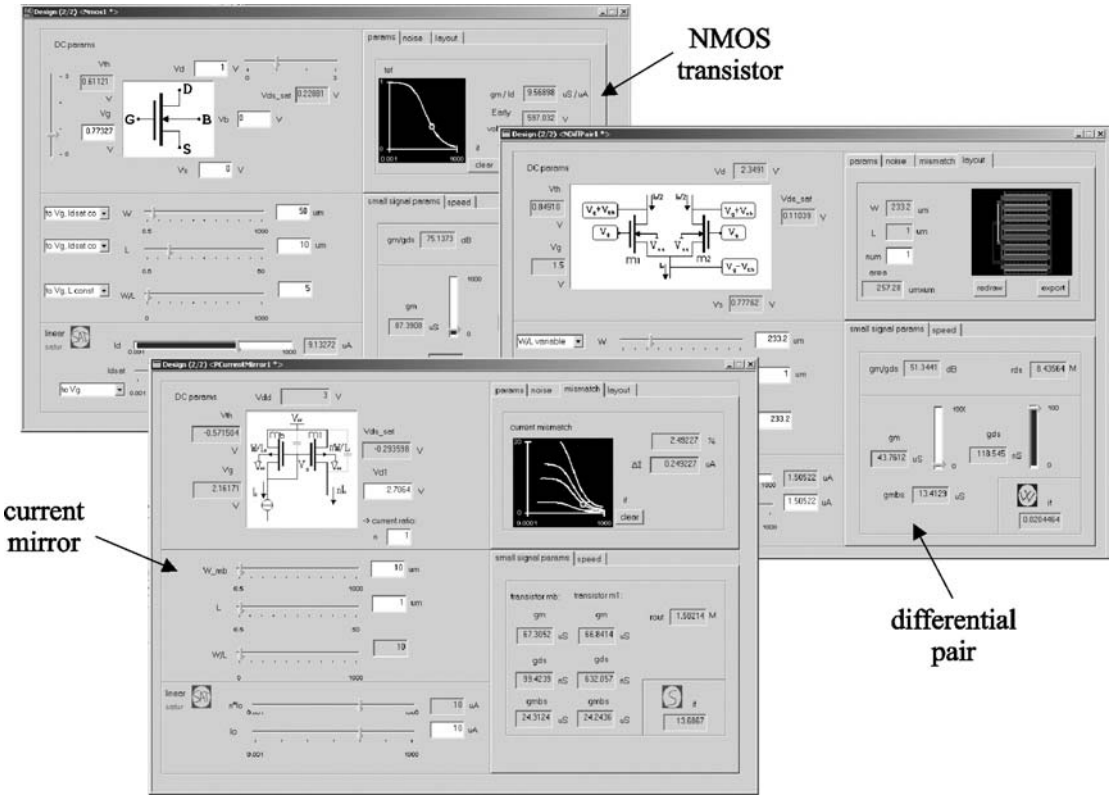

Fig. 4. Basic analog structure sizing.

The procedural analog design steps, together with the examples of user's interface snapshots, are illustrated in Fig. 5. The design initialization consists of the EKV model parameters, initial design requirements, supply voltages, bias currents and compensation and/or load capacitance input. On the basis of input parameters, the circuit currents and the input pair transconductance are proposed. The minimum or maximum values of some parameters are also determined. However, there are no imposed values, and the design of every analog structure depends on user's decisions.

At circuit level, the design sequence and the partitioning into basic analog blocks are predefined. The design scenario guides the user presenting, at each step, the necessary theoretical guidelines and tips from an experienced designer in a separate window. The basic analog structures are sized one after another in a specific order and all dependent circuit parameters are calculated or approximated in order to find trade-offs. The user has a great degree of freedom, which enables exploring the design space and the limits of basic structure parameters' changes. Furthermore, the user can move backward/forward through the scenario to reconsider the taken decisions or to check the proposed guidelines and the design rules. In addition, the dependency analysis of parameters at circuit level is implemented as a separate design step. It also includes the frequency analysis, the equivalent noise and input offset calculation. As a final step, all circuit parameters are calculated and presented in a circuit performance summary. At the end, several simulation runs can be performed for the verification and fine-tuning of the design parameters.

5. Example of Procedural Design of Folded Cascode OTA Using PAD

As an example, the procedural design flow for the folded cascode OTA is illustrated here. The

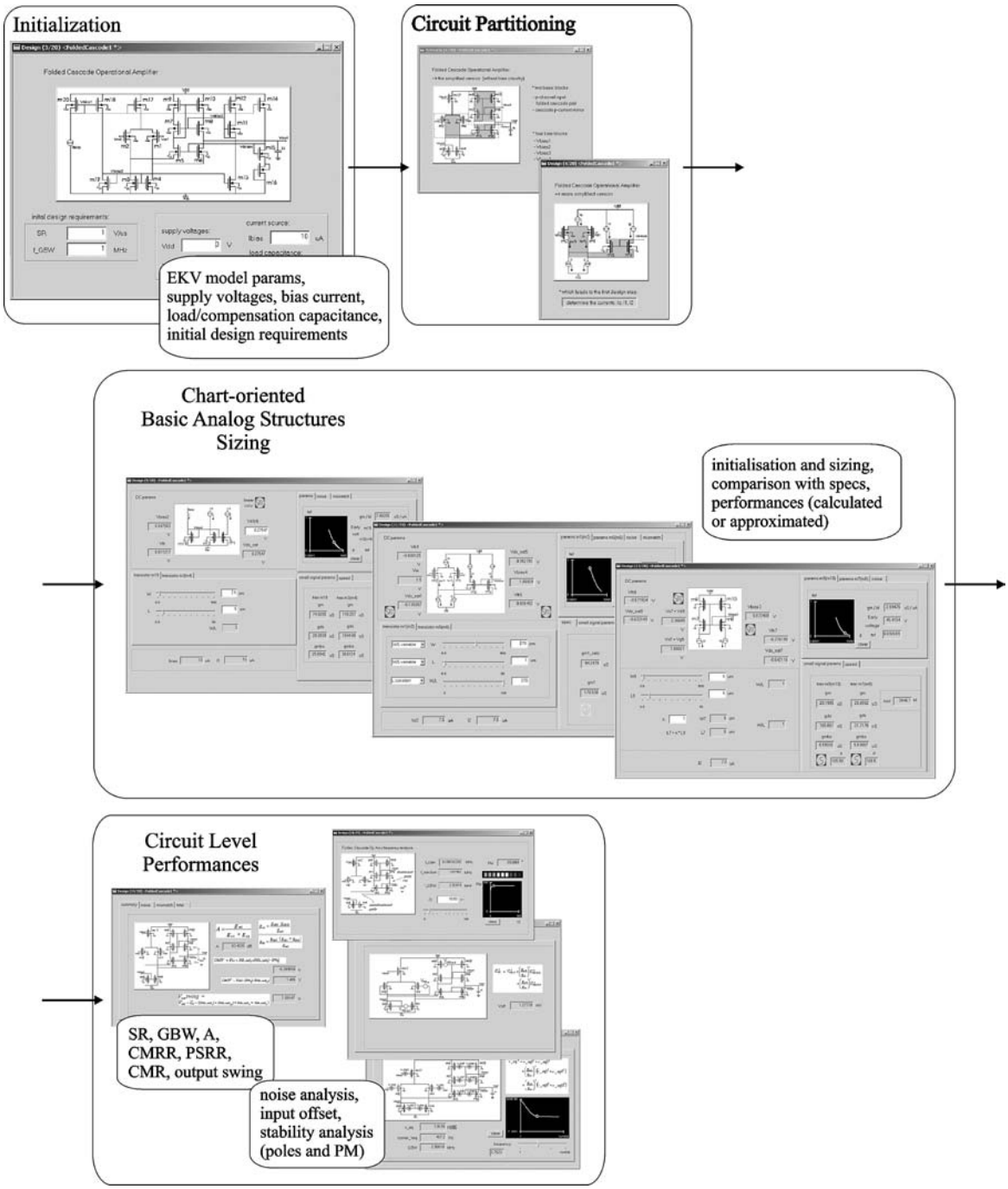

Fig. 5. PAD design flow.

well-known schematic frequently used by analog designers is shown in Fig. 6.

The usual procedure performed by analog designers is to divide the circuit into basic analog blocks and to derive a set of equations that describe the circuit behavior. The folded cascode OTA can be divided into the following basic analog structures (Fig. 6):

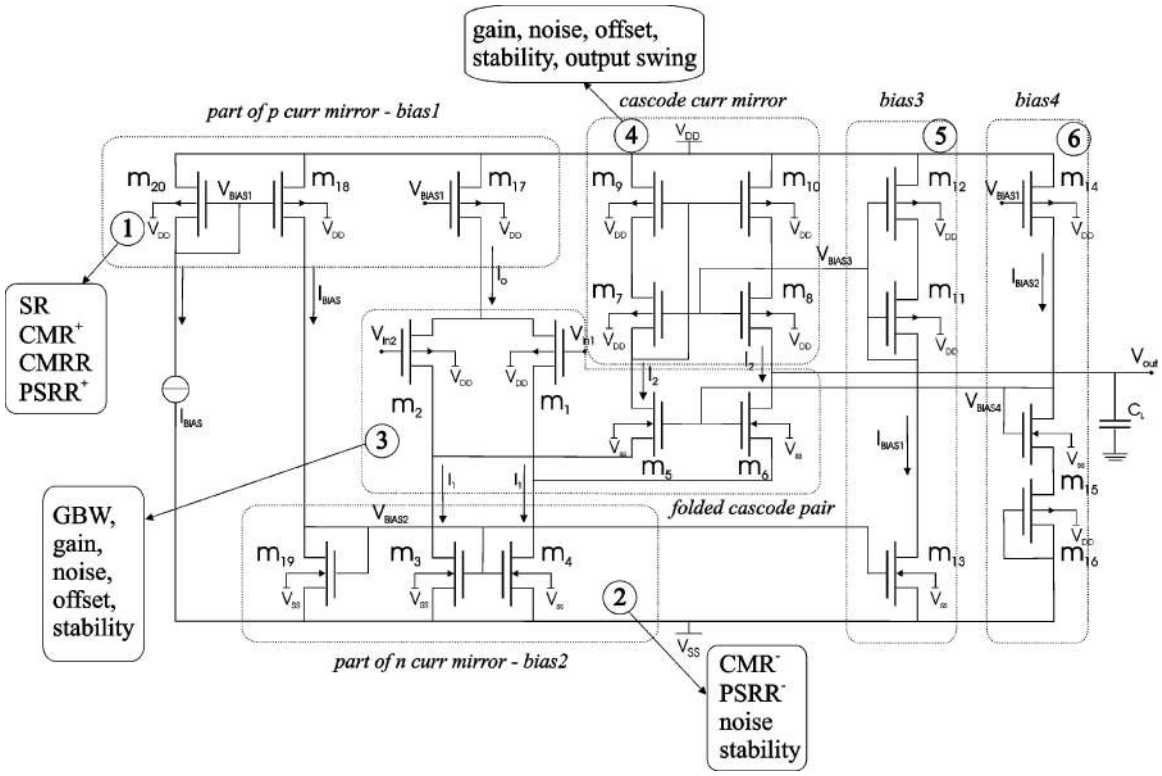

Fig. 6. Folded cascode OTA divided into basic analog structures.

1. bias 1—*p* current mirror
2. bias 2—*n* current mirror
3. folded cascode pair
4. cascode current mirror
5. bias 3—bias for cascode current mirror
6. bias 4—bias for cascode pair

Circuit-level design equations are given in Table 1. Using this equation set and running simulation cycles, the designer discovers tradeoffs and achieves given circuit specifications. This standard design procedure can be time-consuming, it strongly depends on designer's expertise and knowledge and usually a very large number of simulation runs is needed firstly for the design, and then for the optimization and circuit verification.

For the folded cascode OTA structure, the PAD design sequence is as follows:

- initialization
- circuit partitioning
- determination of the currents I_o, I_1, I_2
- sizing of the basic analog structures
- frequency analysis, circuit summary, noise and offset analysis
- simulation runs for fine tuning

Initialization—The user is asked to enter:

- the EKV model parameters
- the initial design requirements: slew rate *SR*, gain bandwidth *f_GBW*
- the bias current I_{BIAS}, the supply voltages $V_{\mathrm{SS}}/V_{\mathrm{DD}}$, the load capacitance C_L

Circuit partitioning—The folded cascode OTA is divided into 6 basic analog structures as depicted in Fig. 6. The corresponding set of equations in PAD is the same as in Table 1.

Basic analog structures sizing—From the initial design requirements two values are proposed:

$$Io\_calc = SR \cdot C_L$$
$$g_{m1}\_calc = 2\pi f\_GBW \cdot C_L$$

Table 1. The equations for the folded cascode OTA design.

Slew rate	$SR = \frac{I_O}{C_L}$
Gain bandwidth frequency	$f\_\text{GBW} = \frac{g_{m1}}{2\pi C_L}$
Power dissipation gain	$PowDisip = (V_\text{DD} - V_\text{SS}) \cdot (2 \cdot I_1 + 2 \cdot I_\text{BIAS} + I_\text{BIAS1} + I_\text{BIAS2})$ $A = \frac{g_{m1}}{g_{ox}+g_{oy}}, g_{ox} = \frac{g_{ds8} \cdot g_{ds10}}{g_{m8}}, g_{oy} = \frac{g_{ds6} \cdot (g_{ds1}+g_{ds4})}{g_{m6}}$
Positive/negative CMR	$\text{CMR}+ = V_\text{DD} - \lvert V_\text{DS\_sat17}\rvert - \lvert V_\text{TH1}\rvert$ $\text{CMR}- = V_\text{SS} + V_\text{DS\_sat4} + \lvert V_\text{DS\_sat1}\rvert - \lvert V_\text{TH1}\rvert$
Output swing	$V_\text{out\_swing} = V_\text{DD} - V_\text{SS} - (\lvert V_\text{DS\_sat8}\rvert + \lvert V_\text{DS\_sat10}\rvert + V_\text{DS\_sat6} + V_\text{DS\_sat4})$
Equivalent noise	$v\_eq^2 = v\_eq_1^2 + v\_eq_2^2 + \left(\frac{g_{m4}}{g_{m1}}\right)^2 \left(v\_eq_3^2 + v\_eq_4^2\right) + \left(\frac{g_{m9}}{g_{m1}}\right)^2 \left(v\_eq_9^2 + v\_eq_{10}^2\right)$
Input offset	$V_\text{off}^2 = (\sigma(\delta V_{G1}))^2 + \left(\frac{g_{m4}}{g_{m1}}\right)^2 (\sigma(\delta V_{G4}))^2 + \left(\frac{g_{m9}}{g_{m1}}\right)^2 (\sigma(\delta V_{G9}))^2 (\sigma(\delta V_G))^2$ $= \sigma_T^2 + \left(\frac{I_D}{g_m}\right)^2 \cdot \sigma_\beta^2 \sigma_T = \frac{A_{Vt}}{\sqrt{WL}}, \sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$
Pole estimations and phase margin	$f\_p_1 = \frac{g_{ox}+g_{oy}}{C_L}, f\_p_2 = \frac{g_{m6}}{C_{S6}+C_{D4}+C_{D1}} PM = 180^\circ - arctg\left(\frac{f\_\text{GBW}}{f\_p_1}\right) - arctg\left(\frac{f\_\text{GBW}}{f\_p_2}\right)$

From then on, the designer follows the given design procedure for every analog block sizing, as described above. For each block the designer can modify the set of independent parameters and observe the impact of his decisions on circuit parameters. The most important point is to determine the circuit currents according to the imposed *SR* value, as well as the g_m for every transistor according to circuit performances. For each basic analog structure, Fig. 6. shows a list of dependent circuit parameters.

Circuit level design—During the sizing of each block, the circuit performance parameters can be checked. After having designed all building blocks, circuit-level behavior is summarized and interface to a simulator is proposed. The simulation runs are needed here only for the verification and fine-tuning.

This design procedure can be repeated several times in interaction with the simulator, if necessary. Not only the number of simulation runs is reduced to minimum, but transistor sizing and (at the same time) circuit optimization are also achieved.

6. BSIM Model Library File Input (BSIM to EKV Conversion)

As described previously, the transistor level calculator implemented in PAD is based on the EKV MOS model. This implies that PAD requires the EKV model parameters (or the EKV model library file) as input. On the other hand, as over past years BSIM family of models were widely used for the design of analog circuits and the BSIM Version 3.3 became an industrial standard, there are some foundries that do not provide EKV model library files. However, the EKV model is indispensable for the transistor level design of analog cells in the procedural design flow implemented in PAD. In order to make it possible to use PAD tool with both BSIM and EKV input library files, a BSIM to EKV model library file converter is developed (Fig. 7).

The BSIM to EKV converter is based on the EKV model parameters extraction procedure described in [5] and implemented as a separate module. It generates the EKV model library file Version 2.6 from the BSIM model library file Version 3.3. This converter requires the BSIM .lib file (for PSpice) and the information about technology such as: voltage range, minimum transistor length and width and parameter *HDIF* (calculated from the design rules as defined in the EKV model).

From then on, it runs the simulator (PSpice) to simulate all required curves and extracts the EKV model parameters by fitting the simulated curves. The fitting algorithm implements a complete extraction method and covers different geometries (wide/long, wide/short, narrow/long devices). At the end, an EKV model .lib file is generated with the following parameters set: all intrinsic model parameters, temperature parameters, series resistance, $1/f$ noise parameters, gate overlap

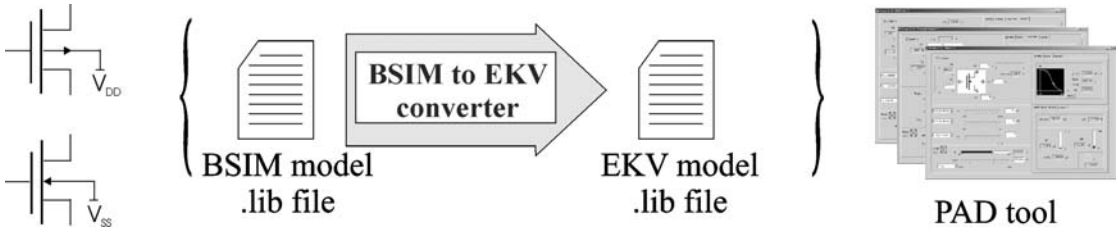

Fig. 7. BSIM/EKV model library file as an input.

capacitances and junction capacitance parameters. For each parameter set, a fitting error is calculated and written to the conversion report file. Furthermore, a set of test bench simulations is provided.

One conversion run takes less than 5 minutes on an Intel Pentium 4 machine clocked at 2.4 GHz and extracts parameters with fitting errors within the range of 5 percents.

7. Conclusion

This paper presents a new chart-based Procedural Analog Design (PAD) tool and a new knowledge based analog design methodology. The PAD tool allows to encapsulate design knowledge and experience into a CAD tool and to hand them on to other designers.

This interactive tool enables design and re-design of a wide range of circuits. The present version covers the most commonly used analog topologies. The proposed procedural design enables transistor sizing and circuit optimization at the same time. Simulation runs are required only for the verification and fine-tuning and therefore reduced to minimum. For the design of other (more specific or more complicated) circuit topologies, the basic analog structures library can be used for separate blocks sizing. The simulator is then used interactively with PAD after sizing of each block. In this way, a great improvement in the quality of analog design can be achieved.

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