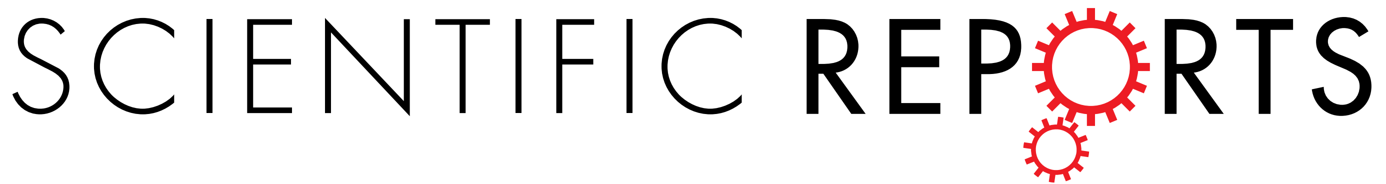

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Palladium gates for reproducible quantum dots in silicon

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We replace the established aluminium gates for the formation of quantum dots in silicon with gates made from palladium. We study the morphology of both aluminium and palladium gates with transmission electron microscopy. The native aluminium oxide is found to be formed all around the aluminium gates, which could lead to the formation of unintentional dots. Therefore, we report on a novel fabrication route that replaces aluminium and its native oxide by palladium with atomic-layer-deposition-grown aluminium oxide. Using this approach, we show the formation of low-disorder gate-defined quantum dots, which are reproducibly fabricated. Furthermore, palladium enables us to further shrink the gate design, allowing us to perform electron transport measurements in the few-electron regime in devices comprising only two gate layers, a major technological advancement. It remains to be seen, whether the introduction of palladium gates can improve the excellent results on electron and nuclear spin qubits defined with an aluminium gate stack.

The realization of a quantum computer using spins in a solid-state system[1,2] has made impressive progress over the last decades. In recent years, group-IV materials like silicon[3] and carbon[4] have attracted a lot of attention, since they can be isotopically purified to only consist of spin-zero nuclei. Metal-oxide-semiconductor devices inspired by classical transistors have proven to be highly suitable for the realization of quantum bits both in intrinsic silicon and silicon-germanium heterostructures[3,5]. Their very flexible design has enabled single and double quantum dots[6–9], spin read-out via Pauli spin blockade[10–15], charge sensing experiments with a quantum point contact[16] and dispersive read-out[17], single qubits[10,18–21] and two-qubit logic gates[22] in quick succession. With the demonstration of these building blocks, the reproducible fabrication of fully gate-tuneable devices receives increased attention[23,24]. The formation of unintentional quantum dots[25–27] poses a substantial problem, since they can capacitively couple to the intended quantum dot and disturb both transport and charge sensing measurements. The choice of the gate material plays a central role here, since e.g. different thermal expansion coefficients within the device lead to mechanical strain leading to fluctuations in the electrochemical potential[27,28]. Also chemical reactions with surrounding dielectric layers have to be taken into account due to the possible formation of charge traps. Finally, also the morphology of the gate material dictates reachable feature sizes and gate design. Due to its high-quality native oxide that renders the deposition of inter-gate dielectric layers unnecessary, aluminium was, in recent years, the most commonly used gate material for accumulation-mode quantum dots in silicon, introduced by Angus *et al.* in 2007[6]. The device design reported there has been the workhorse for the impressive follow-up experiments performed at the University of New South Wales[18,22,29–34], and was also successfully implemented by other research groups[26,35–40]. Besides aluminium, also poly silicon has been employed as a gate material[9,41]. Noble metals, like palladium[7], were so far only used for depletion-type quantum dots that do not require multi-layer gate stacks. For such depletion-type dots with palladium gates, also the role of mechanical stress induced by the electrode for the formation of unintentional quantum dots has been studied and found to be non-negligible[28]. This situation is hard to compare to our accumulation-mode devices with several gate layers, and our devices show no pronounced signature of stress-induced quantum dots.

In this Report, we propose the use of palladium as a gate material for accumulation gates, and compare its performance to the commonly used aluminium. In a first part, we characterize the suitability of the two materials as nanoscale gates by means of transmission electron microscopy (TEM). Subsequently, we assess the usability of devices fabricated with Pd gates for the formation of electrostatically defined quantum dots.

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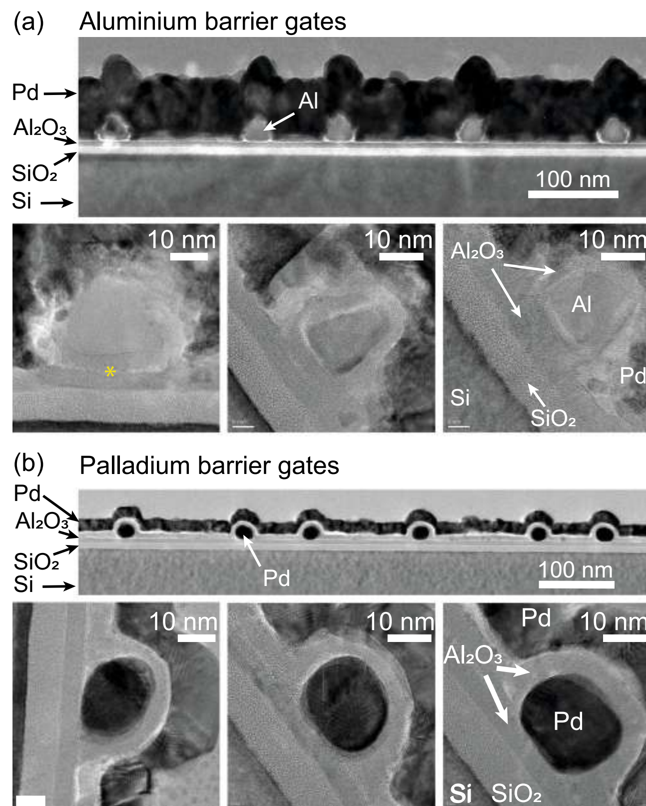

Figure 1. Transmission electron microscopy cross sections of (**a**) aluminium and (**b**) palladium gates on top of a Si-SiO_2-Al_2O_3 layer stack capped by Al_2O_3 and palladium.

Transmission Electron Microscopy

The structures used for the TEM studies are displayed in Fig. 1. The sample layout follows the pioneering device design of Angus *et al.*[6]. A quasi-intrinsic Si wafer is thermally oxidized to form approximately 8 nm of high-quality silicon oxide. In contrast to the original Angus design, we grow an additional dielectric layer of 5 nm aluminium oxide by atomic layer deposition (ALD) at 250 °C with tetramethylammonium hydroxide and H_2O as precursors. In the aluminium gate samples, this layer protects the SiO_2 from partially being reduced to SiO_x with $x < 2$. This reduction due to the stronger oxidation affinity of aluminium otherwise leads to defects directly underneath the gates. The gate structures are then formed by patterning a PMMA layer with electron-beam lithography at an acceleration voltage of 28 kV and subsequent electron-beam evaporation of the gate metal followed by lift-off. At least two layers of gates are required for quantum dot definition. We thermally oxidize the aluminium samples at 180 °C under ambient conditions on a hot plate to form a 5 nm layer of Al_2O_3 around the Al gates in Fig. 1(a). Since palladium is a noble metal, this is not possible in these samples, and we therefore use another ALD step at a reduced temperature of 150 °C to achieve 5 nm of Al_2O_3 for the samples in Fig. 1(b). For the TEM samples, a thick layer of Pd (thick dark layer in Fig. 1(a)) is deposited on top to protect the sample during preparation of the thin cross section.

The gates in Fig. 1 have a nominal width of 20–30 nm. The effective width of the gate is decreased by approximately 10 nm in the case of Al due to the partial oxidation of the metal. In Fig. 1(a) the different materials are labelled as confirmed by energy-dispersed X-ray (EDX) spectroscopy. In the upper overview panel, we can clearly observe the light SiO_2 on top of the Si substrate followed by the grey Al_2O_3, on top of which the Al gates give a similar contrast to the Al_2O_3. For more clarity three higher-resolution zooms of single barriers are shown in the lower panel of Fig. 1(a). Two distinct Al_2O_3 layers are visible, with a very thin interfacial layer (see asterisk in the left single-gate image of Fig. 1(a)) inbetween. Deducing from the fabrication protocol, we identify the two layers as the ALD-grown lower layer, and the thermal-oxidation layer around the gate. Note here that he oxidation process takes place all around the gate, i.e. not only at the aluminium surface directly subjected to air, but also at the interface between the aluminium and the ALD-grown Al_2O_3 (marked by an asterisk in the lower-left panel of Fig. 1(a)). Here, the oxidation of the aluminium includes the diffusion and subsequent incorporation of oxygen atoms into the material. We speculate that this volumetric increase can generate compressive stress on the underlying layers. The associated band structure modulations can then lead to localization of charges at low temperatures, in analogy to quantum dot formation due to different thermal expansion coefficients[27]. Within the scope of this Report, it is difficult to distinguish these two mechanisms, although we note that the difference in the thermal expansion coefficients with silicon and silicon oxide is very large for aluminium, two times larger than for palladium, while the difference is almost zero for poly-silicon[27,42]. This leads to a reduced risk of charge localization by stress-induced potential fluctuations.

Lim *et al.*[8] observed a similar aluminium oxide formation at the Al-SiO_2 interface in their devices. Quantum dots formed below a single gate have been successfully used to demonstrate single-hole tunneling[37,43] and electron quantum bits[18]. For individual control over the electrochemical potential of the quantum dot as well as the tunnel barriers, however, these strain-induced quantum dots are detrimental.

The Pd gates in Fig. 1(b) do not oxidize, so the second Al_2O_3 layer grown by ALD is here only visible at the top part of the Pd gates, not all around them. The zoom-in micrographs in the lower panel of Fig. 1(b) exhibit a more uniform shape and width-to-height ratio than their Al counterparts. We can assign this to an interesting difference between the Al and Pd films deposited for lift-off in the same electron-beam evaporator under the same conditions: while the Pd film morphology looks identical on the substrate and on top of the PMMA layer, the Al grains are substantially larger on top of the PMMA layer (see Supplementary Figure 1), leading to the characteristic triangular cross-sections for narrow Al gates. The increased grain size on top of the polymer resist layer suggests a substantial surface diffusion of Al. This limits the structure size achievable with Al compared to Pd under otherwise identical conditions and leads to overall more uniform gate structures for Pd gates in our metal evaporation system. Apart from the grain size, also the Al gate oxidation itself limits the reduction of the device feature size, since 10 nm of the oxide have to be taken into account in the quantum dot design. Center-to-center gate pitches of 40 nm or less are thus hard to reach with aluminium in a lift-off process, but achievable with palladium, and desirable for reaching the few-electron regime (see e.g. the following section).

In conclusion, the TEM study suggests that gate structures similar to the Angus design made from palladium instead of aluminium can achieve smaller feature sizes and fewer unintentional dots in the formation of quantum dots with individual control over the tunnel barriers and dot potential by means of several gates.

Reproducible quantum dot devices

In Fig. 2(a), a typical device used for studying the fabrication reproducibility of tuneable quantum dot devices made with Pd gates is displayed. 25 nm wide Pd barrier gates with a center-to-center distance of 60 nm are covered by a 5 nm thick Al_2O_3 dielectric layer, followed by a lead gate also made of Pd with a width of 30 nm between the barrier gates. An additional 5 nm Al_2O_3 is grown on top of the whole gate structure before the devices are annealed for 30 min at 400 C in a hydrogen atmosphere. The quantum dot formed under the lead gate between the barrier gates thus has a size of approximately 35 by 30 nm.

In Fig. 2(b) we show data of palladium devices from three separate chips, i.e. apart from the SiO_2 and lowest Al_2O_3 layer, they have been fabricated in three separate fabrication runs in order to demonstrate chip-to-chip reproducibility of the current-voltage measurements. For comparison we also added data from a device with Al gates. All measurements shown in Fig. 2 have been performed at 4.2 K. A constant bias voltage of $V_{SD} = 1$ mV was applied to the ohmic contact overlapping with the lead gate on the left as indicated in the sketch in Fig. 2(a), and the current flowing from the drain to ground was measured. The left column in Fig. 2(b) contains current versus gate voltage curves for all three devices. We will call the green curves in Fig. 2(b), where the voltage is applied to the lead gate and both barrier gates simultaneously, turn-on curves. The measurements for the blue (orange) curves in the palladium devices were performed by applying a constant voltage of 4 V to the lead gate and the right (left) barrier gate to ensure electron accumulation between them, and changing the voltage on the left (right) barrier from 4 V to 0 V. We will refer to them as pinch-off curves for the left (right) barrier gate. Measurements on the aluminium device were performed in the same way, except that the constant voltage on the gates not used for pinch-off was 3.5 V.

While all Pd devices turn on at voltages between 2 and 3 V, the pinch-off curves show a significantly lower and much steeper threshold voltage for pinching off the conductance channel, very much like Angus *et al.*[6] observed. In all three devices the pinch-off curves exhibit only very few or even no resonance around the threshold voltage. Such resonances are commonly attributed to resonant tunneling via localized states within the created tunnel barrier, as discussed in the previous section. We first compare these pinch-off curves to those measured on Al gate devices fabricated in the same cleanroom. Data of one such device is plotted in the lowest panel of Fig. 2(b). Mueller *et al.* recently reported on a second device, with pinch-off curves in Fig. 2a of their publication[38]. For both Al devices, the pinch-off curves are taken at a $V_{SD} = 1$ mV (same as for the Pd devices), and show multiple resonances each. Multiple kinks and resonances are also visible in the high-bias pinch-off curves in Fig. 2b of Mueller *et al.*[38]. None of the Al barrier gates displays a clean, resonance-free pinch-off as is the case for barrier 2 of Device C in this Report. We acknowledge the limited statistics of this comparison, but also note that the Al devices reported here and in Mueller's manuscript already represent a significant improvement compared to another report by the same authors[26] (see Fig. 3a there). Data similar to what Mueller *et al.* reported have also been published by Betz *et al.*[36], where turn-on as well as pinch-off curves exhibit multiple, irregular resonances, indicating the formation of more than one unintentional quantum dot.

A clearer picture of the device physics can be drawn based on the data shown next to the respective current vs. gate voltage curves in Fig. 2(b). Here, the voltages on the barriers V_{b1} and V_{b2} are varied while a constant voltage $V_{lead} = 4$ V is applied to the lead gate. All three charge stability diagrams of the Pd devices reveal diagonal lines, indicating the formation of a single quantum dot with equal capacitive coupling to both barriers. For Device A, a single instability around $V_{b1} = 1780$ mV is visible. Device B also mainly exhibits one resonance below one of the barriers at $V_{b2} = 1320$ mV, which leads to deviations from the ideal single quantum dot picture indicating the formation of a strongly coupled double quantum dot consisting of the quantum dot between the barriers and one unintentional dot below barrier 2[44]. Finally, Device C is completely free of deviations from the ideal single quantum dot behaviour across many charge transitions, suggesting a defect-free electrostatic environment of the quantum dot. Again, we compare these data to the lowest panel of Fig. 2(b) and those reported by Mueller *et al.* in Fig. 4b of the publication[38]. In both cases, the data show diagonal Coulomb peaks as a clear indication of the formation of a quantum dot defined by both barrier gates. Additionally, multiple resonances capacitively coupled

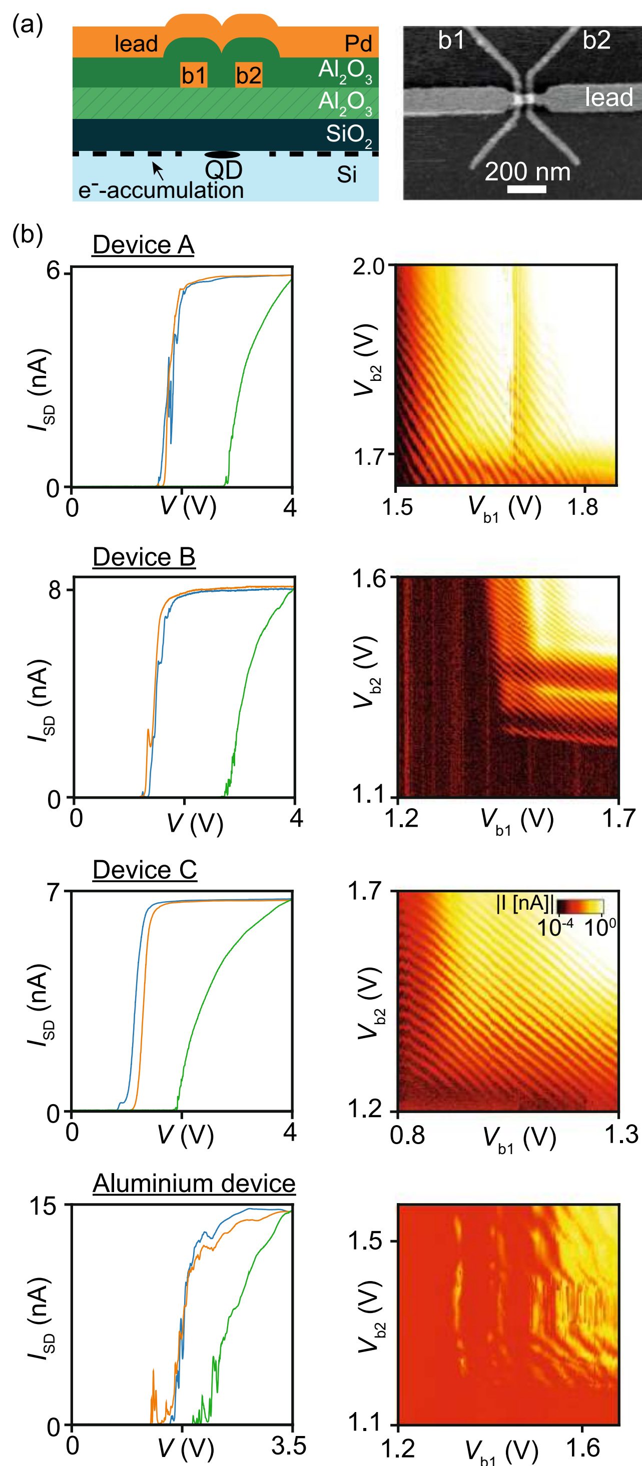

Figure 2. (**a**) Schematic cross-section and atomic-force microscopy top-view of a typical Pd device. (**b**) Measurements taken at 4.2 K for three Pd devices on three different chips, and one device with aluminium gates. Left column: current vs gate voltage applied to all three gates simultaneously (green curve), and applied to barrier gate b1 (b2) [blue (orange) curve] while keeping the voltage on the other two gates at 4 V for the Pd devices, and 3.5 V for the Al device. Right column: current versus voltages on b1 and b2 with $V_{lead} = 4\ V$ for the Pd devices, and $V_{lead} = 3.5\ V$ for the Al device.

to only one barrier are visible for both barriers, an indication for more than one unintentional dot. Furthermore, the diagonal Coulomb peaks display 'switchy' behavior as a result of charge noise.

We want to stress one thought: while comparing data for Pd and Al devices fabricated in the same cleanroom minimizes the effect of using different equipment (e.g. contamination of the evaporation chamber), it also limits the generalizability of the conclusions drawn. We acknowledge that, while the Pd devices seem to exhibit fewer

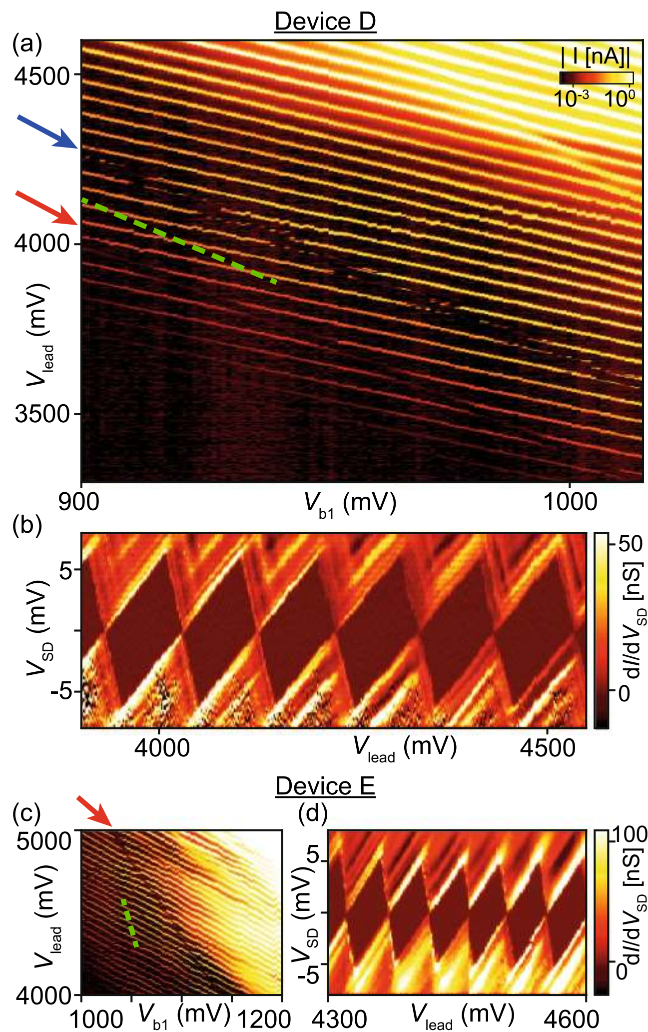

Figure 3. Measurements performed on Pd devices at 25 mK. Current versus voltage on the lead gate and the barrier gates at $V_{SD} = 1$ mV in Device D (**a**) and Device E (**c**). In (**a**), V_{b1} and V_{b2} are linked by $V_{b2} = V_{b1} + 300$ mV. In (**c**), $V_{b2} = V_{b1} - 250$ mV, and the colour scale is the same as in (**a**). The arrows indicate deviations from the single quantum dot picture. (**b**) and (**d**) are bias spectroscopy plots along the dashed lines in (**a**) and (**c**), respectively.

unintentional dots than the Al devices, these findings are not hard proof yet, but more an intriguing hint, that hopefully encourages other research groups to confirm our results.

Further evidence for the findings from the barrier 1 versus barrier 2 plots is provided by measuring Devices D and E from the same chip as Device A in a dilution refrigerator with an electron temperature of approximately 25 mK. In Fig. 3(a) and (c) we plot charge stability diagrams, where we change V_{lead} versus V_{b1} and V_{b2}, with a fixed offset of $V_{b2} = V_{b1} + 300$ mV. Again, parallel, equally spaced current peaks indicate the formation of a single quantum dot. These Coulomb oscillations are only disturbed along two parallel lines marked by a red and a blue arrow in (a), and a single line marked by a red arrow in (c). These disturbances are most likely caused by a defect capacitively coupled to our quantum dot, varying the electrostatic environment by changing its own charge state. Since these two charging events follow parallel lines in gate space in Fig. 3(a), they most likely have the same origin.

Bias spectroscopy measurements are displayed for both devices in Fig. 3(b) and (d), where we plot the numerical differential conductance dI/dV_{SD} while changing V_{SD} and the gate voltages on all three gates simultaneously to follow the dashed lines in Fig. 3(a) and (c). In both cases, the measurements reveal Coulomb diamonds of constant height and shape, indicating a stable electrostatic environment and quantum dot shape and size. The charging energy is approximately 6 meV in both cases. The additonal lines of increased conductance at finite bias can be explained by, e.g., orbital excited states[45,46].

In conclusion, our experiments show that, by using palladium gates, electrostatic definition of quantum dots can be reproducibly achieved and the data suggest a possible reduction of unintentional quantum dots under single barriers compared to Al gate devices. Further evidence under different fabrications conditions is needed to make a general statement.

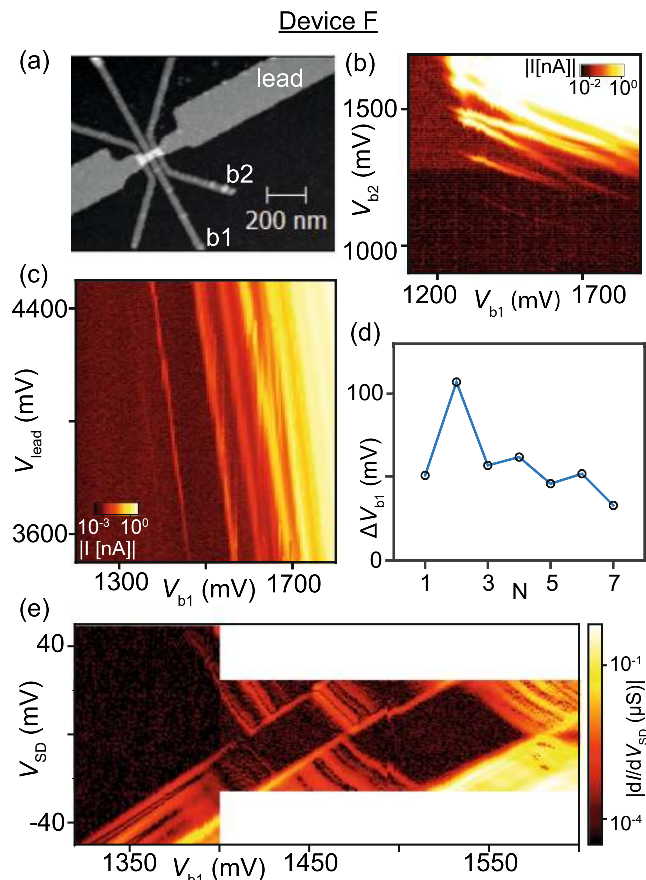

Figure 4. (**a**) AFM image of Device F with a gate pitch of 40 nm. The leftmost barrier gate was not connected. (**b**) plot of I versus the voltages on the barrier gates b1 and b2 with fixed $V_{\mathrm{lead}} = 4000$ mV and $V_{\mathrm{SD}} = 1$ mV. (**c**) I plotted versus $V_{\mathrm{lead}} = 4000$ mV and $V_{\mathrm{b1}} = V_{\mathrm{b2}} + 300$ mV at $V_{\mathrm{SD}} = 1$ mV. (**d**) The Coulomb peak distance ΔV_{b1} between adjacent Coulomb peaks at $V_{\mathrm{lead}} = 3500$ mV. (**e**) Differential conductance dI/dV_{SD} versus V_{b1} at $V_{\mathrm{lead}} = 3500$ mV. All measurements taken at 4.2 K.

Few-electron quantum dots with two-layer devices

Reaching the few-electron regime in gate-defined quantum dots in silicon has proven to be very difficult due to the comparably high effective mass of the electrons[3], a problem that has successfully been circumvented by employing a more complex gate stack with a third layer comprising a dedicated plunger gate[47].

Palladium as a gate metal provides us with an opportunity to reach the few-electron regime without complicating the device design: shrinking the size of the quantum dot to hold fewer electrons to start with. Since they do not oxidize, we can shrink the width of the barrier gates as well as their thickness to approximately 10–15 nm without risking broken gates due to oxidation. This allows us to scale down the barrier gate pitch to 40 nm in Device F (Fig. 4(a)). The charge stability diagram in Fig. 4(b), where we change V_{b1} and V_{b2}, displays again diagonal Coulomb oscillation, but far fewer than in the 60 nm pitch devices in Fig. 3.

A further signature for the lower number of electrons on this quantum dot is revealed in Fig. 4(c), where we plot I_{SD} versus V_{lead} and V_{b1}, with $V_{\mathrm{b2}} = V_{\mathrm{b1}} - 300$ mV. The Coulomb peaks are parallel, signature for the formation of a single quantum dot, but not equidistant. The peak spacing ΔV_{b1} in Fig. 4(d) shows a clear even-odd effect, as well as a trend towards lower peak spacings for higher numbers of electrons N added to the quantum dot. The latter indicates an increasing gate capacitance and thus a deviation from the constant interaction model[48]. This can be explained by a decreasing quantum dot size with decreasing electron occupation[49]. The current is non-zero between Coulomb peaks for $V_{\mathrm{b1}} \gtrsim 1550$ mV at $V_{\mathrm{lead}} = 4000$ mV, a sign for the tunnel barriers being transparent enough for inelastic processes to become significant[46]. At lower barrier gate voltages, the Coulomb peaks are well-separated by Coulomb blockade, and at $V_{\mathrm{b1}} < 1410$ mV for $V_{\mathrm{lead}} = 3500$ mV, no Coulomb peak is visible any more. There are two possible explanations for this: either the quantum dot is empty at this point, or the tunnel barriers simply have become too opaque to allow for a measurable Coulomb peak even though there are still electron states available.

Since our device does not feature a charge sensor[16], we are restricted to transport measurements, which makes it difficult to distinguish the two scenarios. A signature of a not yet empty quantum dot is a saw-tooth-like pattern at finite bias[43], whereas a clean opening of the Coulomb diamond up to high source-drain bias voltages[47,50–52] is a strong sign for the absence of available charge states, i.e. an empty quantum dot. Figure 4(e) shows a bias

spectroscopy of the first two charge transitions visible in Fig. 4(c). For barrier gate voltages lower than V_{b1} = 1410 mV, the onset of conductance opens up without any disturbance up to the measurement range of V_{SD} = ±50 mV, just as expected for an empty dot. Further evidence for reaching the single-electron regime is provided by the addition energies E_{add} of the first electrons added to the quantum dot: while E_{add} = 17 meV for the second electron entering the dot, the energy needed to add the third electron is significantly higher (E_{add} = 24 meV). This can be explained by a significant orbital energy E_{orb} leading to an even-odd effect for the charging energies[46]. $E_{orb} \approx 7$ meV is consistent with a line of increased conductance visible for positive V_{SD} in the first Coulomb diamond, which could thus represent the first orbital excited state[45]. The even-odd effect due to the additional orbital energy in Fig. 4(d) and (e) becomes weaker for higher numbers of electrons, in accordance with findings in other systems[51,53–55].

The undisturbed high-bias opening of the last Coulomb diamond combined with the even-odd filling of the first electrons onto the quantum dot provides strong evidence for the observation of the single-electron regime in our device with the 40-nm gate pitch.

Conclusion

In conclusion, we have demonstrated the suitability of palladium with ALD-grown aluminium oxide for gate stacks in MOSFET-like quantum dot devices in silicon. They provide very good run-to-run reproducibility for the fabrication of single-quantum dot devices with only few defects, possibly since chemical alterations of the silicon oxide layer below the gate are avoided, and mechanical stress imposed by the gate is minimized. The small grain size and nobility of palladium also allow for device dimensions small enough to reach the few-electron regime even in two-layer gate designs, something very unusual in accumulation-mode devices in silicon. Performing transport measurements through quantum dots down to the last electron is highly desirable in fundamental research, since a direct energy scale is provided by the applied source-drain bias, which makes spectroscopy measurements much more feasible than by using charge sensing techniques. It also facilitates the read-out of single-spin quantum bits via Pauli spin blockade.

Data availability. The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

References

1. Loss, D. & DiVincenzo, D. P. Quantum computation with quantum dots. *Physical Review A* **57**, 120–126 (1998).
2. Kane, B. E. A Silicon-Based Nuclear Spin Quantum Computer. *Nature* **393**, 133–137 (1998).
3. Zwanenburg, F. A. *et al*. Silicon quantum electronics. *Reviews of Modern Physics* **85**, 961–1019 (2013).
4. Laird, E. A. *et al*. Quantum transport in carbon nanotubes. *Reviews of Modern Physics* **87**, 703–764 (2015).
5. Morton, J. J. L., McCamey, D. R., Eriksson, M. A. & Lyon, S. A. Embracing the quantum limit in silicon computing. *Nature* **479**, 345–353 (2011).
6. Angus, S. J., Ferguson, A. J., Dzurak, A. S. & Clark, R. G. Gate-defined quantum dots in intrinsic silicon. *Nano letters* **7**, 2051–5 (2007).
7. Simmons, C. B. *et al*. Charge sensing and controllable tunnel coupling in a Si/SiGe double quantum dot. *Nano letters* **9**, 3234–8 (2009).
8. Lim, W. H. *et al*. Electrostatically defined few-electron double quantum dot in silicon. *Applied Physics Letters* **94**, 173502 (2009).
9. Tracy, L. A. *et al*. Double quantum dot with tunable coupling in an enhancement-mode silicon metal-oxide semiconductor device with lateral geometry. *Applied Physics Letters* **97**, 192110 (2010).
10. Maune, B. M. *et al*. Coherent singlet-triplet oscillations in a silicon-based double quantum dot. *Nature* **481**, 344–347 (2012).
11. Liu, H. *et al*. Pauli-spin-blockade transport through a silicon double quantum dot. *Physical Review B* **77**, 073310 (2008).
12. Lai, N. S. *et al*. Pauli spin blockade in a highly tunable silicon double quantum dot. *Scientific reports* **1**, 110 (2011).
13. Li, R., Hudson, F. E., Dzurak, A. S. & Hamilton, A. R. Pauli Spin Blockade of Heavy Holes in a Silicon Double Quantum Dot. *Nano Letters* **15**, 7314–7318 (2015).
14. Betz, A. C. *et al*. Dispersively Detected Pauli Spin-Blockade in a Silicon Nanowire Field-Effect Transistor. *Nano Letters* **15**, 4622–4627 (2015).
15. Borselli, M. G. *et al*. Pauli spin blockade in undoped Si/SiGe two-electron double quantum dots. *Applied Physics Letters* **99**, 1–4 (2011).
16. Simmons, C. B. *et al*. Single-electron quantum dot in Si/SiGe with integrated charge sensing. *Applied Physics Letters* **91**, 213103 (2007).
17. Gonzalez-Zalba, M. F. *et al*. Gate-Sensing Coherent Charge Oscillations in a Silicon Field-Effect Transistor. *Nano Letters* **16**, 1614–1619 (2016).
18. Veldhorst, M. *et al*. An addressable quantum dot qubit with fault-tolerant control-fidelity. *Nature Nanotechnology* **9**, 981–985 (2014).
19. Kim, D. *et al*. Quantum control and process tomography of a semiconductor quantum dot hybrid qubit. *Nature* **1**, 1–12 (2014).
20. Maurand, R. *et al*. A CMOS silicon spin qubit. *Nature Communications* **7**, 13575 (2016).
21. Takeda, K. *et al*. A fault-tolerant addressable spin qubit in a natural silicon quantum dot. *Science Advances* **2**, e1600694 (2016).
22. Veldhorst, M. *et al*. A two-qubit logic gate in silicon. *Nature* **526**, 410–414 (2015).
23. Zajac, D. M., Hazard, T. M., Mi, X., Nielsen, E. & Petta, J. R. Scalable Gate Architecture for a One-Dimensional Array of Semiconductor Spin Qubits. *Physical Review Applied* **6**, 1–8 (2016).
24. Spruijtenburg, P. C., Amitonov, S. V., Mueller, F., van der Wiel, W. G. & Zwanenburg, F. A. Passivation and characterization of charge defects in ambipolar silicon quantum dots. *Scientific Reports* **6**, 38127 (2016).
25. Ishikuro, H. & Hiramoto, T. On the origin of tunneling barriers in silicon single electron and single hole transistors. *Applied Physics Letters* **74**, 1126–1128 (1999).
26. Mueller, F., Konstantaras, G., Van Der Wiel, W. G. & Zwanenburg, F. A. Single-charge transport in ambipolar silicon nanoscale field-effect transistors. *Applied Physics Letters* **106**, 10–15 (2015).
27. Thorbeck, T. & Zimmerman, N. M. Formation of strain-induced quantum dots in gated semiconductor nanostructures. *AIP Advances* **5**, 087107 (2015).
28. Park, J. *et al*. Electrode-stress-induced nanoscale disorder in Si quantum electronic devices. *APL Materials* **4** (2016).
29. Morello, A. *et al*. Single-shot readout of an electron spin in silicon. *Nature* **467**, 687–691 (2010).
30. Pla, J. J. *et al*. A single-atom electron spin qubit in silicon. *Nature* **489**, 541–5 (2012).
31. Pla, J. J. *et al*. High-fidelity readout and control of a nuclear spin qubit in silicon. *Nature* **496**, 334–338 (2013).

32. Laucht, A. *et al*. High-fidelity adiabatic inversion of a 31 P electron spin qubit in natural silicon. *Applied Physics Letters* **104**, 092115 (2014).
33. Muhonen, J. T. *et al*. Storing quantum information for 30 seconds in a nanoelectronic device. *Nature Nanotechnology* **9**, 986–991 (2014).
34. Laucht, A. *et al*. Electrically controlling single-spin qubits in a continuous microwave field. *Science* 1–5 (2015).
35. Podd, G. J., Angus, S. J., Williams, D. A. & Ferguson, A. J. Charge sensing in intrinsic silicon quantum dots. *Applied Physics Letters* **96**, 082104 (2010).
36. Betz, A. C., Gonzalez-Zalba, M. F., Podd, G. J. & Ferguson, A. J. Ambipolar quantum dots in intrinsic silicon. *Applied Physics Letters* **105**, 153113 (2014).
37. Spruijtenburg, P. C. *et al*. Single-hole tunneling through a two-dimensional hole gas in intrinsic silicon. *Applied Physics Letters* **102**, 192105 (2013).
38. Mueller, F., Konstantaras, G., Spruijtenburg, P. C., van der Wiel, W. G. & Zwanenburg, F. A. Electron-Hole Confinement Symmetry in Silicon Quantum Dots. *Nano Letters* **15**, 5336–5341 (2015).
39. Amitonov, S. V., Spruijtenburg, P. C., Vervoort, M. W. S., van der Wiel, W. G. & Zwanenburg, F. A. Depletion-mode Quantum Dots in Intrinsic Silicon. *Applied Physics Letters* **112**, 023102 (2017).
40. Spruijtenburg, P. C., Amitonov, S. V., Van Der Wiel, W. G. & Zwanenburg, F. A. A fabrication guide for planar silicon quantum dot heterostructures. *Nanotechnology* **29**, 143001 (2018).
41. Lu, T. M. *et al*. Enhancement-mode buried strained silicon channel quantum dot with tunable lateral geometry. *Applied Physics Letters* **99**, 97–100 (2011).
42. Nix, F. & MacNair, D. The Thermal Expansion of Pure Metals. II:Molybdenum, Palladium, Silver, Tantalujm, Tungsten, Platinum, and Lead. *Phys. Rev.* **61**, 74 (1941).
43. Li, R., Hudson, F. E., Dzurak, A. S. & Hamilton, A. R. Single hole transport in a silicon metal-oxide-semiconductor quantum dot. *Applied Physics Letters* **103**, 1–5 (2013).
44. van der Wiel, W. G. *et al*. Electron transport through double quantum dots. *Reviews of Modern Physics* **75**, 1–22 (2003).
45. Escott, C. C., Zwanenburg, F. A. & Morello, A. Resonant tunnelling features in quantum dots. *Nanotechnology* **21**, 274018 (2010).
46. Hanson, R., Petta, J. R., Tarucha, S. & Vandersypen, L. M. K. Spins in few-electron quantum dots. *Reviews of Modern Physics* **79**, 1217–1265 (2007).
47. Lim, W. H. *et al*. Observation of the single-electron regime in a highly tunable silicon quantum dot. *Applied Physics Letters* **95**, 242102 (2009).
48. Kouwenhoven, L. P. *et al*. Electron transport in quantum dots. In Proceedings of the NATO Advanced Study Institute on Mesoscopic Electron Transport, 105–214 (1997).
49. Kouwenhoven, L. P., Austing, D. G. & Tarucha, S. Few-electron quantum dots. *Reports on Progress in Physics* **64**, 701–736 (2001).
50. Kouwenhoven, L. P. *et al*. Excitation spectra of circular, few-electron quantum dots. *Science* **278**, 1788–92 (1997).
51. Jarillo-Herrero, P., Sapmaz, S., Dekker, C., Kouwenhoven, L. P. & Van Der Zant, H. S. J. Electron-hole symmetry in a semiconducting carbon nanotube quantum dot. *Nature* **429**, 389–392 (2004).
52. Zwanenburg, F. A., van Rijmenam, C. E. W. M., Fang, Y., Lieber, C. M. & Kouwenhoven, L. P. Spin states of the first four holes in a silicon nanowire quantum dot. *Nano letters* **9**, 1071–9 (2009).
53. Tarucha, S., Austing, D. G., Honda, T., van der Hage, R. J. & Kouwenhoven, L. P. Shell Filling and Spin Effects in a Few Electron Quantum Dot. *Physical Review Letters* **77**, 3613–3616 (1996).
54. Johnson, A. C., Petta, J. R., Marcus, C. M., Hanson, M. P. & Gossard, A. C. Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot. *Physical Review B* **72**, 165308 (2005).
55. Nilsson, H. A. *et al*. Giant, Level-dependent g factors in InSb nanowire quantum dots. *Nano Letters* **9**, 3151–3156 (2009).

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Author Contributions

M.B., S.V.A. and P.C.S. fabricated the devices. M.B. and P.C.S. performed the measurements. M.B., P.C.S. and F.A.Z. analysed the results. M.B. wrote the manuscript. All authors reviewed the manuscript.

Additional Information

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