

Paradigms of connectivity for computer circuits and networks

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Abstract. We discuss several concepts of connectivity for circuit graphs, including Rent's rule, line length distributions, and separators, all of which we argue are fractal concepts. We provide generalizations for systems for which the Rent exponent is not constant throughout the interconnection hierarchy.

Subject terms: connectivity; Rent's rule; fractals; optical interconnections; wiring models.

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1 Introduction

Essential to the general analysis of interconnection and packaging technologies are models of the connectivity of circuit graphs and computer networks. The importance of so-called wiring models have long been recognized and extensively used.¹⁻⁶ On the other hand, connectedness has always been a central concept in mathematical graph theory.⁷⁻⁹ Extensions of some of these ideas play a central role in graph layout.¹⁰

This paper brings together some concepts used to quantify the communication requirements of computer circuits. More generally, these concepts can serve as paradigms of information transfer among the parts of a cybernetic system.

This paper is not meant as a review or tutorial, but rather aims to provide a unifying viewpoint for hitherto scattered concepts and a guide to some of the literature. The reader is referred to the references for further details. Applications of these concepts to the study of optical interconnection architectures^{11,12} and optoelectronic computing systems can be found in Refs. 13 through 17.

2 Paradigms of Connectivity

2.1 Interconnectivity and Dimensionality

Graph layout involves determining how the nodes and edges of a particular graph will be situated in physical space (Fig. 1). Optimal graph layout¹⁸ is, in general, an NP-complete problem.¹⁹ However, once a hierarchical decomposition of a graph is provided, this graph can be laid out following relatively simple algorithms. A hierarchical decomposition of a graph consisting of N_0 nodes and the associated decomposition function $k(N)$ are obtained as follows.

First, we remove $k(N_0)$ edges to disconnect the graph into two subgraphs, each of approximately $N_0/2$ nodes. Roughly speaking, we try to do this by removing as few edges as possible. We repeat this procedure for the subgraphs thus created. The subgraphs, in general, require differing numbers of edges to be removed from them to be disconnected into subsubgraphs of $\approx N_0/2^2$ nodes each. We denote the largest of these numbers as $k(N_0/2)$. Continuing in this manner until the subgraphs consist of a single node each, we obtain the function $k(N)$, the (worst case) number of edges removed during decomposition of subgraphs of N nodes. Once such a decomposition is found, it is possible to lay out the graph in the intuitively obvious manner by

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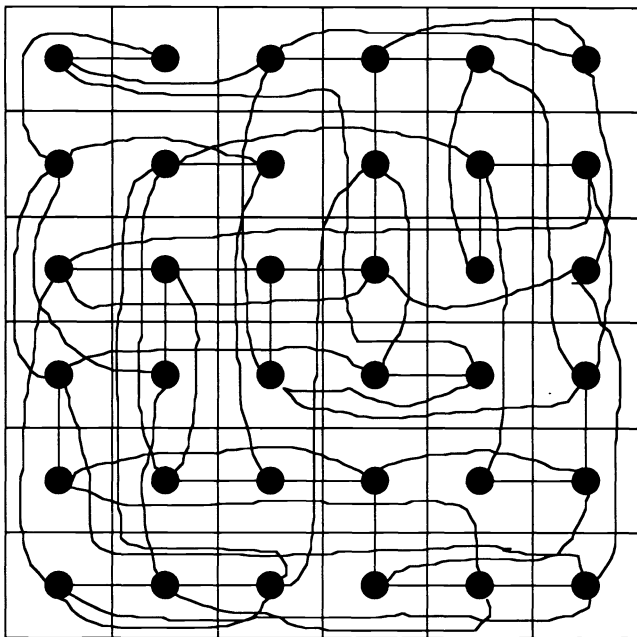


Fig. 1 Graph layout. A particular graph has been laid out in two-dimensional Euclidean space. For convenience, the nodes have been situated on a regular Cartesian grid.

working upward.^{20,10,19} Whereas one can always find some decomposition, finding the decomposition that leads to a layout with some optimal property (such as minimal area) is not a trivial problem. We assume that we agree on a particular decomposition obtained by some heuristic method.

Now, let us define the interconnectivity $p(N)$ and dimensionality $n(N)$ associated with the hierarchical level of a decomposition involving subgraphs of N nodes by*

$$p(N) = \frac{n(N) - 1}{n(N)} = \log_2 \frac{k(N)}{k(N/2)} \quad (1)$$

It is possible to find arbitrarily many examples of graphs for which the values of $k(N)$ and $p(N)$ for different values of N are totally erratic and have no correlation whatsoever. However, both computer circuits and natural systems are observed to exhibit varying degrees of continuity of the functions $k(N)$ and $p(N)$.

Let the geometric derivative \tilde{f} of a function f at the point x be defined analogous to the usual arithmetic derivative

$$\tilde{f}(x) = \lim_{v \rightarrow 1^+} \log_v \frac{f(vx)}{f(x)} \quad (2)$$

If $k(N)$ is slowly varying, we can pretend that it is a continuous function and write

$$p(N) = \frac{n(N) - 1}{n(N)} = \tilde{k}(N) \quad (3)$$

which can be inverted as

$$k(N) = k(1) \exp\left(\int_1^N \frac{p(\bar{N})}{\bar{N}} d\bar{N}\right) \quad (4)$$

where \bar{N} is a dummy variable.

Of course, since $k(N)$ is actually a function of a discrete variable, we cannot actually let $v \rightarrow 1$. The smallest meaningful value of v in our context is 2. Hence, the geometric derivative should be interpreted in the same sense as we interpret the common derivative in the form of a finite difference for discrete functions. Thus, for our definition to make sense, $k(N)$ must be a slowly varying function (which is simply a more physical way of expressing the mathematical condition of continuity). As already noted, this is indeed observed over large variations of N in both computer circuits and natural systems. In fact, in many cases, it is found that $p(N)$ and $n(N)$ are approximately constant over a large range of N . Such systems are said to exhibit self similarity,^{21,22} or scale invariance.

2.2 Rent's Rule

Assuming that $p(N) = p = \text{constant}$, we find from Eq. (4) that $k(N) = k(1)N^p$. This is nothing but the famous Rent's rule,^{†,23,24} which gives the number of graph edges $k(N)$ emanating from partitions of computer circuits containing N nodes (such as the number of pinouts of an integrated circuit package containing N gates). We interpret $k(1)$ as the average number of edges per node. Donath has shown that Rent's rule is a consequence of the hierarchical nature of the logic design process.^{25,26}

2.3 Separators

A graph of N_0 nodes is said to have an $S(N)$ separator [or to be $S(N)$ separable] if the graph can be disconnected into two (roughly equal) subgraphs by removal of $S(N_0)$ edges and if the subgraphs thus created are also $S(N)$ separable.¹⁰ Although we will not go into the details, note that a graph with interconnectivity function $p(N)$ has a separator of the form $S(N) \propto N^{\max[p(N)]}$, where the maximum is taken over the whole domain of N . Separators play a central role in combinatoric approaches to graph layout.^{20,10} (An alternative way of describing the communication requirements of graphs is based on what are called bifurcators.¹⁹)

Thus, we see that both Rent's rule and separators of the form $S(N) \propto N^p$ are special cases of the formalism we have introduced. Apart from minor technicalities involved in their definition, all are equivalent when $p(N) = \text{constant}$. In general, $p(N)$ and $n(N)$ are functions of N .

2.4 Fractal Geometry

The dimensionality $n(N)$ defined in Eq. (3) is a fractal dimension.^{22,27-29} The fractal dimension of a natural system, just as that of computer circuits, can also vary as we ascend or descend the hierarchical structure of that system. In any event, Rent's rule, fractal geometry, and separators are tied together by the notions of self-similarity, scale invariance, and continuity in the relationships between the volume-like

*In general the defined quantities satisfy $0 \leq p(N) \leq 1$ and $1 \leq n(N) \leq \infty$.

†Strictly speaking, for this expression to correspond to Rent's rule, it must be modified by a coefficient of the order of unity. However, we avoid this minor technicality for the purpose of this paper.

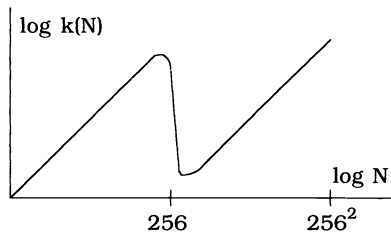


Fig. 2 The decomposition function $k(N)$. The decomposition function for a system of $N=256^2$ nodes (perhaps gates) consisting of 256 processors of 256 nodes each is presented. The number of “pinouts” of the processors bears no relationship to their internal structure. The functional form given in Eq. (4) can be used directly for the range $1 < N < 256$, and with a shift of origin for the range $256 < N < 256^2$.

(number of nodes) and surface-like (number of edges) quantities.

To clarify this point, we offer the following simplified explanation of why the quantity defined as $n = 1/(1-p)$ is being referred to as a “dimension.” The perimeter of a square region is proportional to the $1/2$ power of its area. The surface area of a cube is proportional to the $2/3$ power of its volume. In general, the hyperarea enclosing a hyperregion of e dimensions is proportional to the $(e-1)/e$ power of its hypervolume. Let us now make an analogy between “hyperarea” \Leftrightarrow “number of graph edges emanating from a region,” and “hypervolume” \Leftrightarrow “number of nodes in the region.” According to Rent’s rule, the number of edges emanating from the region is proportional to the p ’th power of the number of nodes in the region. Thus, it makes sense to speak of the quantity n defined by the relation $p = (n-1)/n$ as a dimension. Note that, in general, n need not be an integer.

2.5 Inverse Power Law Distributions

Let us assume that a graph with $n(N) = n = \text{constant}$ is laid out in e -dimensional Euclidean space (in microelectronic circuits, e is often $=2$; in any event, $e \leq 3$) according to the divide-and-conquer layout algorithm^{20,10} (i.e., as intuitively suggested by its decomposition). Such a layout internally satisfies Rent’s rule. Donath³⁰ and Feuer³¹ have shown that such a layout has a probability distribution $g(r)$ of line lengths of the form

$$g(r) \propto r^{-e/n-1} \quad r \leq \sqrt{e}N^{1/e}, \quad (5)$$

where r denotes line lengths in units of node-to-node spacing of the layout. (We assume the nodes are laid out on a regular Cartesian grid, as in Fig. 1.) The relationship between such inverse power law distributions and fractal concepts were discussed by Mandelbrot,³²⁻³⁴ closing the circle. Using the above distribution, or by combinatoric methods, we can show that when $n > e$, the average connection length of such a layout of N elements is given by²¹

$$\bar{r} = \kappa(n, e)N^{1/e-1/n}, \quad (6)$$

where $\kappa(n, e)$ is a coefficient of the order of unity. The accuracy of this expression requires that $N^{1/e-1/n} \gg 1$. This result has a simple interpretation. The average connection length is simply the ratio of the linear extent of the system in e -space ($N^{1/e}$) to that in n -space ($N^{1/n}$). The node-to-node

spacing (Fig. 1) necessary to layout a graph of dimensionality n is given by $\bar{r}^{1/(e-1)} \lambda \sim N^{(n-e)/ne(e-1)} \lambda$, where λ is the line-to-line spacing of whatever interconnection technology is being used.³⁵⁻³⁷ (Essentially equivalent results can be shown to hold also for free-space optical interconnections.³⁸) Thus, when $n > e$, the area (or volume) per node grows with N . This has been referred to as space dilation.³⁹ Examples of graphs exhibiting large values of n are hypercubes, butterfly and shuffle exchange graphs, and neural networks. It is also easily verified that the given definition of dimension is consistent with that for multidimensional meshes.⁴⁰

2.6 Role of Discontinuities

Whereas it is observed that the function $k(N)$ exhibits considerable continuity over large variation of N , it is also observed that it occasionally exhibits sharp discontinuities. In other words, it no longer becomes possible to predict the value of the function $k(N)$ for certain N by knowing its values at nearby N . For instance, in the context of Rent’s rule, it becomes impossible to predict the number of pinouts of a VLSI chip by observing its internal structure, or vice versa.²⁷ However, this does not imply that Rent’s rule [in its generalized form, as given by Eq. (4)] is useless. Consider a multiprocessor computer. Rent’s rule can be used to predict the wiring requirements internal to each of the processors. It can also be used for similar purposes for the interconnection network among the processors. In fact, the Rent exponent may even be similar in both cases. However, the function $k(N)$ may exhibit a steep discontinuity (often downward), as illustrated in Fig. 2. As is usually the case, a finite number of discontinuities in an otherwise smooth function need not inhibit us from piecewise application of our analytical expressions. Such discontinuities are often associated with the self-completeness of a functional unit.^{24,27} Similar examples can also be found in the natural system. For instance, mammalian brains seem to satisfy $n > 3$ (i.e., $p > 2/3$), since the volume per neuron has been found to be greater in species with larger numbers of neurons.⁴¹ The human brain has 10^{11} neurons, each making about 1000 connections.⁴² Thus, we would expect at least $1000 (10^{11})^{2/3} \sim 10^{10}$ “pinouts.” However, we have only about 10^6 fibers in the optic nerve and 10^8 fibers in the corpus callosum.

Why are such discontinuities observed? In the context of microelectronic packaging, a quote from C. A. Neugebauer offers some explanation: “Since the I/O capacity (of the chip carrier) is exceeded, a significant number of chips can be interconnected only if the pin/gate ratio can be drastically reduced, normally well below that predicted by Rent’s rule. Rent’s rule can be broken at any level of integration. The microprocessor chip is an example of the breaking of Rent’s rule in its original form for gate arrays on the chip level. Being able to delay the breaking of Rent’s rule until a much higher level is always an advantage because it preserves many parallel data paths even at very high levels of integration, and thus offers higher systems performance and greater architectural flexibility.”⁴³

Thus, the breaking of Rent’s rule seems to be perceived as a technological necessity, and undesirable from a systems viewpoint. However, the difficulty of maintaining a large fractal dimension throughout the hierarchy extends beyond present implementations, and applies even to idealized free-

space optical layouts.³⁸ Thus, perhaps there is an advantage to constructing processing systems in the form of a hierarchy of functionally complete entities.

3 Open Questions

Fractal concepts have been quite successful in *describing* natural phenomena. However, there has not been so much success in *explaining* why fractal forms come up so often. Why do computer circuits lend to such a description? Perhaps because of the hierarchical nature of the design process. One viewpoint is that there is an inherent dimensionality of information flow related to the application so that a computer circuit/network is not just an arbitrary graph but has an underlying structure.

One suspects that fractal forms may exhibit certain optimal properties. For instance, bitonic (divide-and-conquer) algorithms can be viewed as elementary fractal forms. Is it possible to postulate general principles (such as the principle of least action in mechanics) regarding optimal information flow or computation that would lead to an inverse power law distribution of line lengths (i.e., a constant fractal dimension) or some other distribution? Keyes^{41,44} has shown how the number of distinct ways one can wire up an array of elements increases with average wire length. Mandelbrot has postulated maximum entropy principles to predict the observed inverse power law distribution of word frequencies (linguistics)³³ and monetary income (economics).³⁴ Christie has pursued the idea that the wires in a computing system should obey Fermi-Dirac statistics, based on the observation that the wires are indistinguishable (any two wires of same length can be exchanged) and that they obey an exclusion principle (only one wire need connect two points).⁴⁵

Or, rather than having to do with optimality, are the observed properties of computer circuits or networks merely a result of the way we build them, perhaps similar to the way the fractal structure of some biological objects are a consequence of their growth process?

What is the role of discontinuities in an otherwise smooth decomposition function? Is it beneficial to construct systems in the form of a hierarchy of functionally complete entities?

4 Conclusion

Rent's rule has often been heavily criticized, especially in relation to its inapplicability to VLSI and higher levels of the interconnection hierarchy. We believe this to be mostly a result of the inexistence of a generalization allowing the Rent exponent and dimensionality to vary as we ascend the hierarchy and a failure to recognize discontinuities. It seems that in most cases of practical interest, the decomposition function $k(N)$ is piecewise smooth with a finite number of discontinuities.

With the generalizations and clarification provided, we believe that fractal concepts such as Rent's rule, separators, and dimensionality will be useful not only for the description of the often quasirandom and irregular nature of computer circuits and complex systems, but also as general paradigms of information transfer for natural and cybernetic systems.

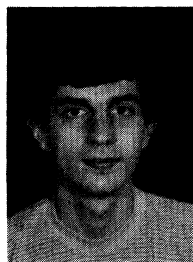
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References

1. R. R. Tummala and E. J. Rymaszewski, Eds., *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York (1989).
2. R. W. Keyes, *The Physics of VLSI Systems*, Addison-Wesley, Reading, Mass. (1987).
3. R. W. Keyes, "Fundamental limits in digital information processing," *Proc. IEEE* **69**, 267-278 (1981).
4. R. W. Keyes, "The evolution of digital electronics towards VLSI," *IEEE Trans. Electron Devices* **26**, 271-279 (1979).
5. H. B. Bakoglu, *Circuits, Interconnections and Packaging for VLSI*, Addison-Wesley, Reading, Mass. (1990).
6. A. Masaki, "Electrical resistance as a limiting factor for high performance computer packaging," *IEEE Circ. Dev. Mag.*, pp. 22-26 (May 1989).
7. B. Bollobas, *Graph Theory: An Introductory Course*, Springer-Verlag, Berlin (1979).
8. G. Strang, *Introduction to Applied Mathematics*, Wellesley-Cambridge Press, Wellesley, Mass. (1986).
9. H. N. V. Temperley, *Graph Theory and Applications*, Ellis Horwood Limited, Chichester (1981).
10. J. D. Ullman, *Computational Aspects of VLSI*, Computer Science Press, Rockville, Md. (1984).
11. H. M. Ozaktas, Y. Amitai, and J. W. Goodman, "Comparison of system size for some optical interconnection architectures and the folded multi-facet architecture," *Opt. Commun.* **82**, 225-228 (1991).
12. H. M. Ozaktas, Y. Amitai, and J. W. Goodman, "A three-dimensional optical interconnection architecture with minimal growth rate of system size," *Opt. Commun.* **85**, 1-4 (1991).
13. H. M. Ozaktas and J. W. Goodman, "The limitations of interconnections in providing communication between an array of points," in S. K. Tewksbury, Ed., pp. 61-124, *Frontiers of Computing Systems Research*, Vol. 2, Plenum Press, New York (1991).
14. H. M. Ozaktas and J. W. Goodman, "Optimal partitioning of very large scale optoelectronic computing systems," in *Opt. Soc. Am. 1990 Annual Meet. Tech. Digest* (1990).
15. H. M. Ozaktas and J. W. Goodman, "Multiplexed hybrid interconnection architectures," in *Tech. Digest of the 1991 OSA Topical Meet. on Opt. Comput.* (1991).
16. H. M. Ozaktas and J. W. Goodman, "Organization of information flow in computation for efficient utilization of high information flux communication media," *Opt. Commun.* **89**, 178-182 (1992).
17. H. M. Ozaktas, "A physical approach to communication limits in computation," PhD Thesis, Stanford University, Stanford, California (1991).
18. T. C. Hu and E. S. Kuh, *VLSI Circuit Layout: Theory and Design*, IEEE Press, New York (1985).
19. S. N. Bhatt and F. Thomson Leighton, "A framework for solving VLSI layout problems," *J. Comput. Sys. Sci.* **28**, 300-343 (1984).
20. C. E. Leiserson, *Area-Efficient VLSI Computation*, The MIT Press, Cambridge, Mass. (1983).
21. W. E. Donath, "Placement and average interconnection lengths of computer logic," *IEEE Trans. Circuits Sys.* **26**, 272-277 (1979).
22. L. Pietronero, "Fractals in physics: introductory concepts," in S. Lundqvist, N. H. March, and M. P. Tosi, Eds., *Order and Chaos in Nonlinear Physical Systems*, Plenum Press, New York (1988).
23. B. S. Landman and R. L. Russo, "On a pin versus block relationship for partitions of logic graphs," *IEEE Trans. Comput.* **20**, 1469-1479 (1971).
24. R. L. Russo, "On the tradeoff between logic performance and circuit-to-pin ratio for LSI," *IEEE Trans. Comput.* **21**, 147-153 (1972).
25. W. E. Donath, "Stochastic model of the computer logic design process," Technical Report RC 3136, IBM Thomas J. Watson Research Center, Yorktown Heights, New York (1970).
26. W. E. Donath, "Equivalence of memory to 'random logic,'" *IBM J. Res. Dev.* **18**, 401-407 (1974).
27. D. K. Ferry, "Interconnection lengths and VLSI," *IEEE Cir. Dev. Mag.*, pp. 39-42 (July 1985).
28. B. B. Mandelbrot, *Fractals: Form, Chance and Dimension*, W. H. Freeman, San Francisco (1977).
29. P. Christie, J. E. Cotter, and A. M. Barrett, "Design and simulation of optically interconnected computer systems," in A. P. DeFonzo, Ed., *Interconnection of High Speed and High Frequency Devices and Systems*, *Proc. SPIE* **947**, 19-24 (1989).
30. W. E. Donath, "Wire length distribution for placements of computer logic," *IBM J. Res. Dev.* **25**, 152-155 (1981).
31. M. Feuer, "Connectivity of random logic," *IEEE Trans. Comput.* **31**, 29-33 (1982).
32. B. B. Mandelbrot, *The Fractal Geometry of Nature*, W. H. Freeman, New York (1983).
33. B. B. Mandelbrot, "Information theory and psycholinguistics: A theory of word frequencies," in P. F. Lazarsfeld and N. W. Henry, Eds., *Readings in Mathematical Social Science*, MIT Press, Cambridge, Mass. (1968).
34. B. B. Mandelbrot, "The Pareto-Levy law and the distribution of income," *Int. Economic Rev.* **1**, 79-106 (1960).

35. I. E. Sutherland and D. Oestreicher, "How big should a printed circuit board be?" *IEEE Trans. Comput.*, **22**, 537-542 (1973).
36. W. R. Heller, W. F. Mikhail, and W. E. Donath, "Prediction of wiring space requirements for LSI," *J. Des. Auto. Fault Tolerant Comput.*, **2**, 117-144 (1978).
37. A. El Gamal, "Two-dimensional stochastic model for interconnections in master slice integrated circuits," *IEEE Trans. Cir. Sys.* **28**, 127-134 (1981).
38. H. M. Ozaktas and J. W. Goodman, "Lower bound for the communication volume required for an optically interconnected array of points," *J. Opt. Soc. Am. A* **7**, 2100-2106 (1990).
39. A. C. Hartmann and J. D. Ullman, "Model categories for theories of parallel systems," in G. J. Lipovski and M. Malek, Eds., *Parallel Computing: Theory and Experience*, John Wiley and Sons (1986).
40. W. J. Dally, *A VLSI Architecture for Concurrent Data Structures*, Kluwer Academic Publishers, Norwell, Mass. (1987).
41. R. W. Keyes, "Communication in computation," *Int. J. Theor. Phys.* **21**, 263-273 (1982).
42. R. F. Thompson, *The Brain*, W. H. Freeman and Company, New York (1985).
43. C. A. Neugebauer, unpublished manuscript.
44. R. W. Keyes, "The wire-limited logic chip," *IEEE J. Solid State Circuits* **17**, 1232-1233 (1982).
45. P. Christie and S. B. Styer, "Fractal description of computer interconnection distributions," in S. K. Tewksbury, Ed., *Microelectronic Interconnects and Packaging: System and Process Integration*, Proc. SPIE **1390**, 359-367 (1990).



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