Parallel connection of single-switch three-phase power-factor correction converters for interleaved switching

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Indexing terms: Converters, Interleaved switching

Abstract: A circuit for the parallel connection of multiple high-frequency three-phase power-factor-correction converters is proposed which enables their input and output current ripple to be interleaved. Such interleaved operation substantially improves the composite power factor, line-current ripple and output-voltage ripple. The improvement is investigated by developing solutions to circuit state equations which allow the high-frequency content of the line current, as well as the low-order line-frequency harmonics, to be computed. Conclusions drawn from the computed results are verified experimentally using a 1kW, two-stage, interleaved converter.

1 Introduction

Three-phase power-factor correction preregulators, when implemented with transistor converters comprising six fast switch/diode pairs [1, 2], give a high level of correction performance similar to that achievable with single-phase circuits. The switches of the three-phase converter are, however, only active for 50% of the line-frequency period, and the line currents are, at any instant, conducted by series/parallel combinations of three switches, rather than the one continually active switch commonly found in single-phase circuits. In consequence, the switch-utilisation-ratio (SUR) is about three times lower (see the Appendix, Section 8.1), and a much higher power-semiconductor silicon-area must be used. The device cost associated with introducing power-factor correction into power-electronic systems with a three-phase input is therefore high.

Other factors further increase the relative cost of three-phase power-factor correction preregulators. For example, more complex line-current sensing and control systems are required since three line currents, rather than one, must be actively shaped and controlled to regulate the converter output voltage. Also, the lower switching frequency potential of the high-voltage (i.e. ≥ 1000V) diodes and switches, increasingly IGBTs, which are required if the converter is to be operated directly from 380 to 480V supplies, generally limits the reduction in reactive component volume to well below that achievable in single-phase circuits. MOSFETs and resonant-switch circuits may be employed in single-phase circuits to allow operation at switching frequencies at least an order of magnitude higher because voltage levels are generally lower and the switch position in the circuit facilitates their application.

If only unidirectional power flow is required, the disadvantages of the six-switch three-phase converter may be substantially overcome at the expense of some reduction in power-factor correction ability, by using the three-phase single-switch power-factor correction circuit highlighted in Fig. 1. In this circuit, the output voltage is regulated at a higher level than the peak input line-to-line voltage by closed-loop control of the switch duty cycle, and, provided the circuit is operated in the discontinuous inductor-current mode (DICM) at the appropriate constant duty cycle for a given input and output voltage combination, it naturally draws correctly phased discontinuous line-current waveforms with phase-voltage envelopes (see Fig. 2) without the need for line-current sensing and closed-loop current control. Therefore, if the phase voltages are relatively well balanced and their distortion is low, power-factor correction above 0.95 is possible.

From a power-semiconductor utilisation standpoint, the main advantages of the single-switch three-phase circuit are a 2 to 3 factor increase in switch SUR, inherent zero-current turn-on switching which eliminates the high turn-on switching loss associated with high-voltage freewheel-diode recovery, and the potential to easily incorporate the resonant-switch circuits developed for single-phase circuits to reduce turn-off switching loss and noise. The increase in SUR over the six-switch converter arises because the three line currents are controlled by a single switch which is continually active throughout the line-frequency period. The SUR lies below that of the single-phase converter, despite the line-frequency related ripple in the switch current being lower, because the high ripple inherent to DICM operation gives a peak switch current, and hence a switch current rating, that is two to three times the fundamental line-current peak (see Figs. 2 and 3). This cannot be reduced by changing switching frequency, or component values, if DICM operation is to

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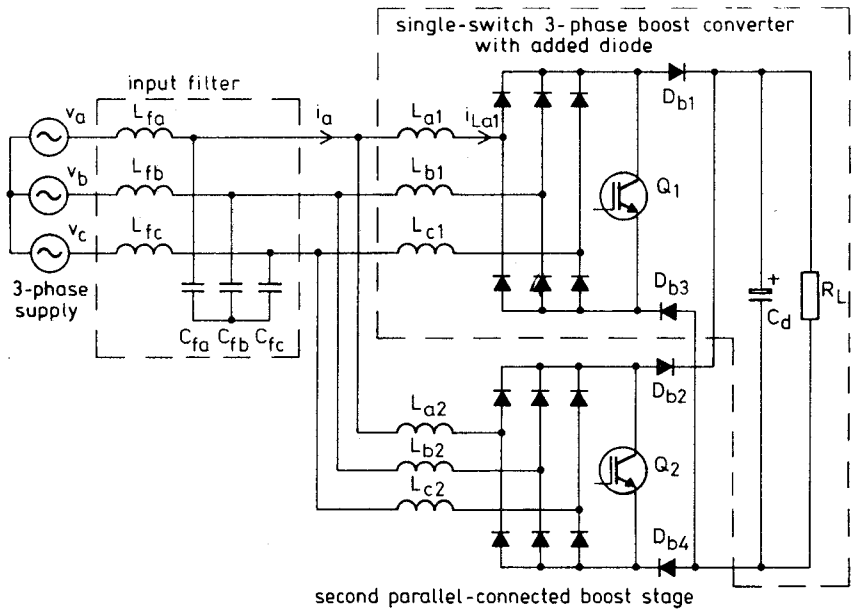

Fig. 1 *Power factor correction preregulator, comprising two parallel-connected single-switch three-phase boost converters for DICM interleaved operation*

be maintained. In contrast, the current ripple in continuous inductor-current mode (CICM) converters can be reduced to negligibly low levels by operating at very high f_{SW} values. Even with the high current ripple, however, a worthwhile reduction in SUR is achievable using the three-phase single-switch circuit.

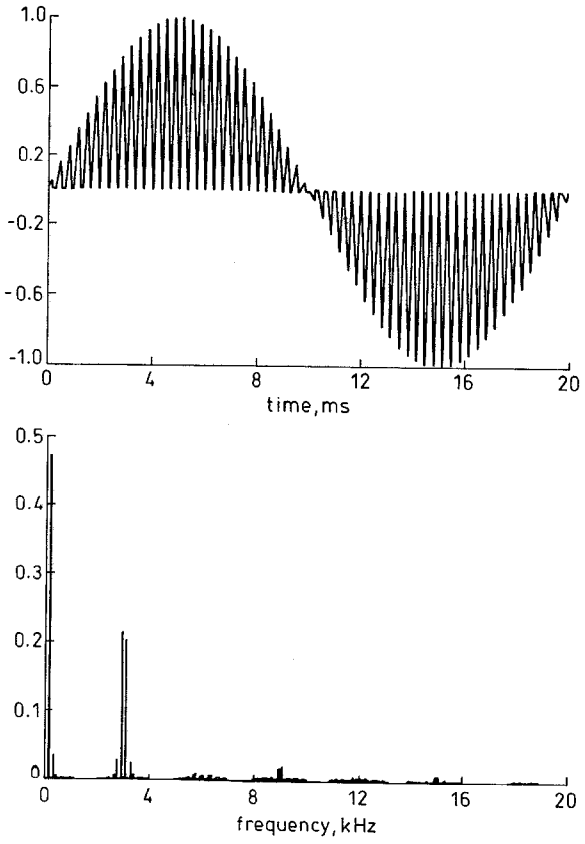

Fig. 2 *Computed phase-a line-current waveform and spectrum for single-stage converter operation, at f_{SW} = 3kHz and D = 0.5*

The advantages of the three-phase single-switch circuit and its potential for cost-effective power-factor correction have been acknowledged in the past, and its analysis and operation have been developed a number of times since it was first proposed [3]. Most recently, a rigorous analysis of harmonic suppression performance and complex data for component sizing have been produced [4], and the small improvement in power-factor correction that is possible using a variable f_{SW} control method, rather than a constant f_{SW} method, has been examined [5]. However, one of the main disadvantages of single-switch three-phase circuits, the high level of peak-to-peak line-current ripple produced as a result of the DICM, has not previously been addressed in

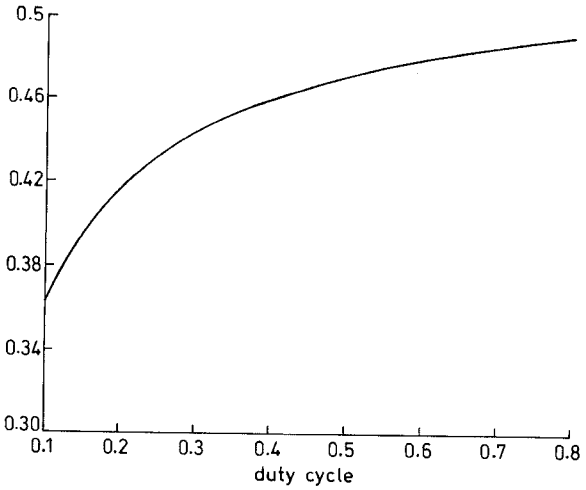

Fig. 3 *Variation in normalised line-current fundamental, $\hat{I}_1/\hat{I}_{L(max)}$, with duty cycle for constant f_{SW}/f_{LINE} at 60*

detail. In previous work, a second-order filter was simply interposed between the AC supply and the converter. The component values required are significantly higher than in CICM converters (i.e. the six-switch type), assuming similar operating conditions, because line-current ripple and salient f_{SW} related frequency components in the line current are more than an order of magnitude higher. An alternative way of addressing the ripple current problem is by operating multiple single-switch converters in parallel (see Fig. 1), and phase-shifting switch conduction so that the composite line-current waveforms comprise the interleaved ripple of the N individual converters. Such interleaved operation has previously been adopted in single-phase DICM

preregulators [6] and multiple-converter active-filtering systems [7], and shown to have several benefits:

(*a*) The composite-current-ripple fundamental frequency is multiplied by N.

(*b*) The input current-ripple amplitude is generally reduced by a factor greater than N, the exact value depending on the duty-cycle.

(*c*) The switch silicon-area remains approximately constant because the line current is naturally shared equally between individual converters.

(*d*) A reduction in the lowest f_{SW}-sideband amplitudes allows some increase in control loop bandwidth because lowpass filters for ripple-amplitude control may be placed at a higher frequency.

The following analysis shows that these benefits may also be exploited in single-switch three-phase converters. However, the direct parallel connection of three-phase converter outputs results in undesirable current circulation, and an additional boost-cell diode must first be added to each converter (see D_{b3} and D_{b4}, Fig. 1) to isolate boost-cell operation and thus make interleaved operation possible.

2 Single-switch three-phase converter circuit

For analysis, a typical sequence of intermediate states for one single-switch converter is first identified by considering pulse-by-pulse circuit operation (see Figs. 4 and 5). Approximate closed-form solutions are then developed for the state equations of these on the assumption that a high, even-integer, carrier-frequency ratio will be used (i.e. $f_{SW}/f_{LINE} \geq 50$), which will normally be the case for MOSFET and IGBT switches. Thus the full line-current spectrum of switching-frequency harmonics and sidebands, as well as line-frequency harmonics, may be computed, whereas previous analysis methods involving per-phase equivalent circuits [3], part cycle-by-cycle analysis [4], or averaged circuit operation [5], generally, only allowed f_{LINE} related effects to be considered.

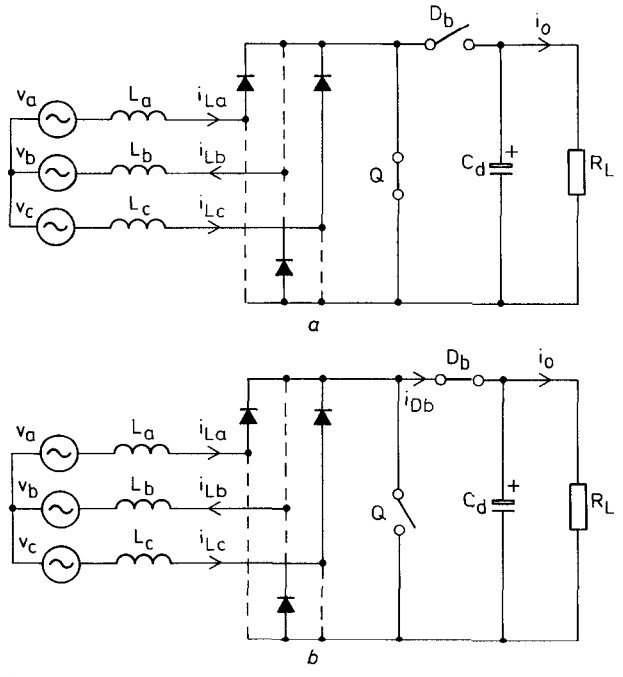

Fig. 4 *Typical sequence of equivalent circuits to model operation within switching periods (continued in Fig. 5)*
a Switch Q is on and boost-diode D_b is off during DT_{SW} period in Fig. 6*a*
b Q is off and D_b is on during period t_{ir1} in Fig. 6*a*

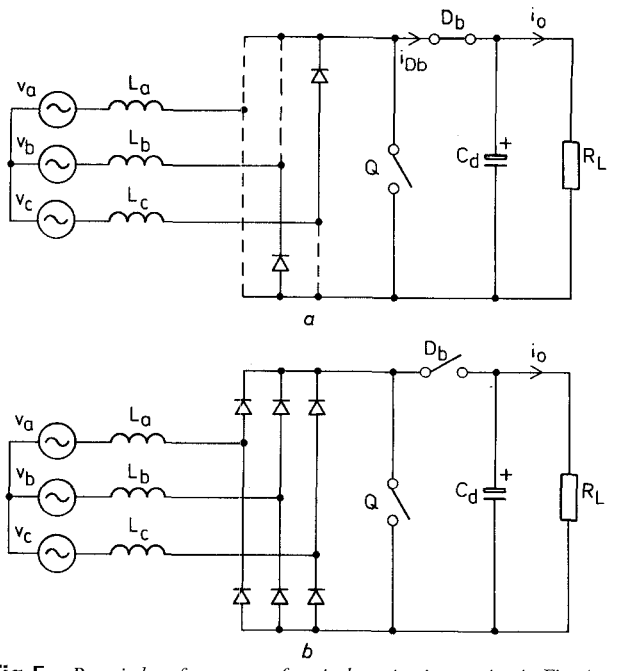

Fig. 5 *Remainder of sequence of equivalent circuits starting in Fig. 4*
a Q is off and D_b is on during period t_{ir2} in Fig. 6*a*
b Both Q and D_b are off after t_{ir2}, when all inductor currents reach zero

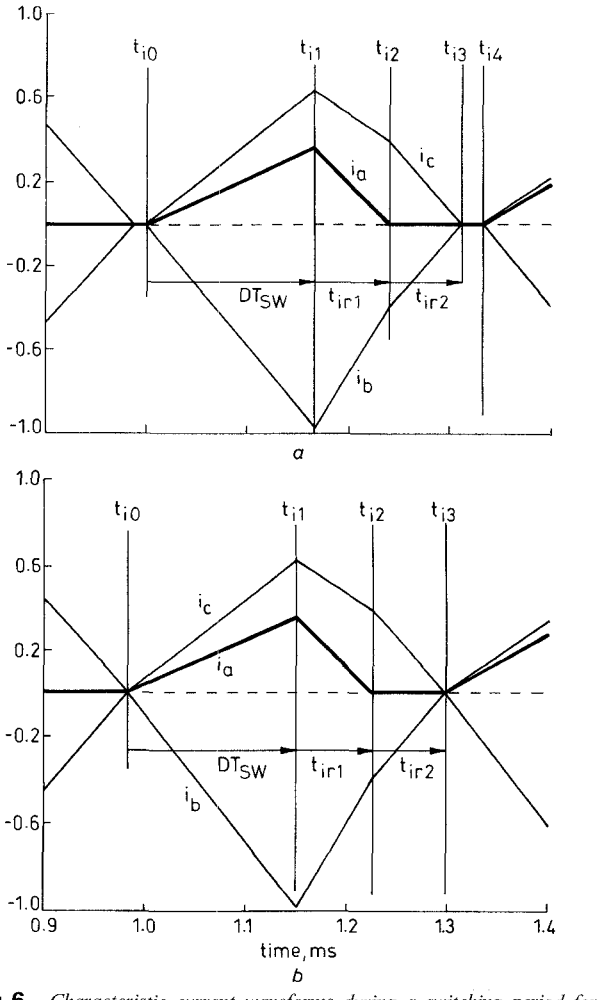

Fig. 6 *Characteristic current waveforms during a switching period for constant switching-frequency and variable switching-frequency control methods*
a Constant
b Variable

The single-stage converter circuit used in Figs. 4 and 5 comprises: a three-phase power-supply system modelled by sinusoidal sources v_a to v_c; a fast-recovery-

diode bridge-rectifier; boost-circuit components L_a to L_c; switch Q; freewheel diode, D_b; sufficient filter capacitance to maintain V_O virtually constant; and an idealised load represented by R_L. Throughout the analysis, steady-state DICM circuit operation at a fixed duty cycle and high switching frequency is assumed, and the power semiconductor devices and passive reactive components are assumed lossless.

During the conduction of Q, boost inductors L_a to L_c are star connected across the balanced 3-phase supply (see Fig. 4*a* and period DT_{SW} in Fig. 6*a*). Consequently, line currents i_a to i_b simultaneously increase at a rate proportional to the instantaneous value of their respective phase voltage. Although the phase voltages vary sinusoidally, they may be assumed constant during a switching period because f_{SW} is far greater than f_{LINE}. Hence, the inductor-current peaks at the instant of each Q turn-off are approximately proportional to their respective phase voltages, and follow three-phase sinusoidal envelopes provided the supply voltage is relatively undistorted (see Fig. 2).

Given the balanced nature of the three-phase supply and fixed duty-cycle operation, a constant value of total energy is thus stored in the line inductors during each Q conduction period. Each time Q is turned off, the inductor currents commutate to D_b and decay to zero since the output voltage is always higher than the peak value of the line-to-line input voltage, e.g. $\hat{V}_{ab}$. During the complete transfer of stored energy to the RC load-cell (a prerequisite for DICM operation), three distinct regions of inductor-current decay are, generally, produced (see t_{i1} to t_{i4} in Fig. 6*a*). A typical set of equivalent circuits used to model the inductor-reset periods is given in Figs. 4*b* and 5*a*.

2.1 Voltage conversion ratio

The voltage conversion ratio M is defined by eqn. 1, where D is the switching duty cycle and V_{LL} the input line-to-line voltage, and is determined by solving a line-inductor volt-second integral over an f_{SW} period. This is best performed when one phase voltage is approximately zero, say at $\omega t = \pi/3$ (i.e. at $t = 3.33$ms if $f_{LINE} = 50$Hz; see Fig. 7*b*), since only two line inductors and phase voltages need be considered. The same conversion ratio must then be obtained at other points in the f_{LINE} period, during steady-state fixed duty-cycle operation, because the energy transferred to C_d from the three line inductors within each f_{SW} period is constant, and the capacitance of C_d is usually chosen to give low output ripple and maintain the output voltage approximately constant at V_O:

$$M = \frac{V_O}{\hat{V}_{LL}} = \frac{1}{1-D} \tag{1}$$

For DICM operation, the minimum permissible duty-cycle value D_{min} is calculated using the maximum peak line voltage and minimum output voltage likely to be experienced during operation.

2.2 Line-current waveforms

Converter line-current waveforms are generated from approximate solutions to sets of generalised state equations. The coefficients of these depend on where operation lies in a phase-*a* f_{LINE} period. For any current-rise period at sampling instants t_i in the f_{LINE} period, Fig. 4*a* applies, and eqns. 2 and 3, alone, model circuit operation. Zero initial conditions apply for i_{Lk}, as DICM operation prevails.

For $t_{i0} \le t \le t_{i1}$,

$$L\frac{di_{Lk}}{dt} = v_k(t_i) \tag{2}$$

$$C_d\frac{dv_o}{dt} = -\frac{V_o}{R_L} \tag{3}$$

$k = a$, b or c, depending on the phase under analysis, and the sampling instants t_i (see Fig. 7) are given by $t_i = (i - 1 + D)T_{SW}$ with $i = 1, 2, ..., p$, where the switching-pulse number p is f_{SW}/f_{LINE}.

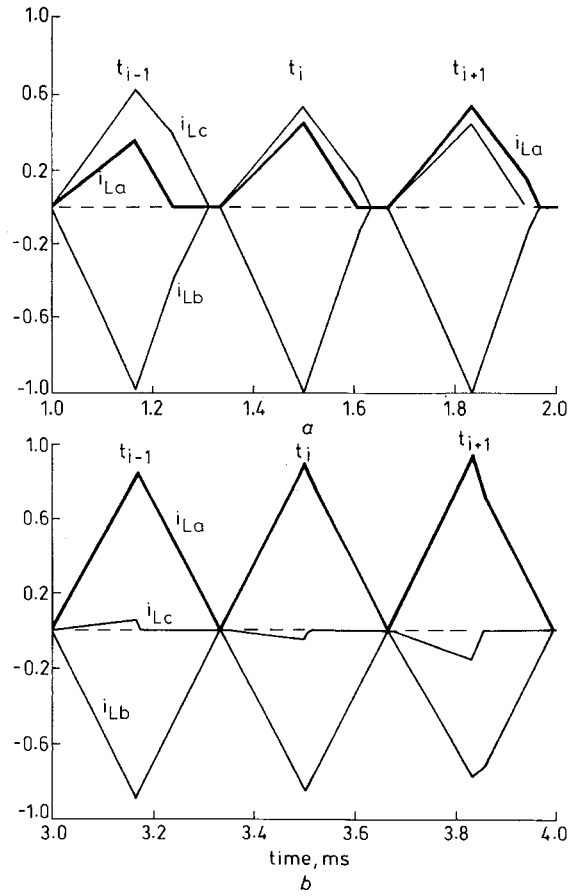

Fig. 7 *Computed current waveforms about π/6 (1.67ms) and π/3 (3.33ms) in a 50Hz line-frequency period for constant switching-frequency control*
a π/6
b π/3

Peak inductor currents at the end of the switch conduction time DT_{SW} are approximated by eqn. 4.

$$i_{Lk}(t_{i1}) = \frac{v_k(t_i)}{L}DT_{SW} \tag{4}$$

assuming $L_a = L_b = L_c = L$. When Q is turned off at t_{i1}, the inductor currents freewheel through D_b, and the RC load cell (Fig. 4*b*) and two periods of inductor current reset generally follow. Initially, all inductors are conducting. The first reset period, t_{ir1}, (Fig. 6*a*) ends when the smallest current reaches zero at t_{i2}. During t_{ir1}, eqns. 5 and 6 apply with initial condition $i_{Lk}(t_{i1})$. In eqn. 5, α_{1k} is a coefficient whose value changes when the phase voltage with the lowest magnitude alters. This is necessary because a different inductor will then reset first and a modified set of equivalent circuits is required. Six sets of α_{1k} values are required to completely model circuit operation, and these are given in the Appendix (Section 8.3).

For $t_{i1} \le t \le t_{i2}$,

$$L\frac{di_{Lk}}{dt} = v_k(t_i) - \alpha_{1k}V_o \tag{5}$$

$$C_d \frac{dv_o}{dt} = i_{Db} - \frac{V_o}{R_L} \quad (6)$$

The second reset period, t_{ir2}, involves the two inductors still conducting (Fig. 5*a*), and persists until all currents have fallen to zero at t_{i3}. Generalised state equations, eqns. 7 and 8, apply for t_{ir2}. The coefficients α_{2k} and X_k change 12 times throughout the f_{LINE} period as the relative values of phase voltage and hence equivalent circuits change. Values are also given in the Appendix (Section 8.3).

For $t_{i2} \leq t \leq t_{i3}$,

$$L \frac{di_{Lk}}{dt} = X_k \left[\sum_{k=a}^{c} \alpha_{2k} v_k(t_i) \right] - \alpha_{2k} V_o \quad (7)$$

$$C_d \frac{dv_o}{dt} = i_{Db} - \frac{V_o}{R_L} \quad (8)$$

For the remainder of T_{SW}, the inductor currents are zero, and eqn. 6, alone, describes operation.

Approximate solutions may be generated for the generalised state equations above and allow normalised inductor-current amplitudes and reset times to be calculated for switching instants throughout the f_{LINE} period. These are given in the Appendix (Section 8.2) for the first f_{LINE} interval, $0 \leq \omega t_i \leq \pi/6$, and must be derived for other intervals to completely describe steady-state circuit operation over an f_{LINE} period [8].

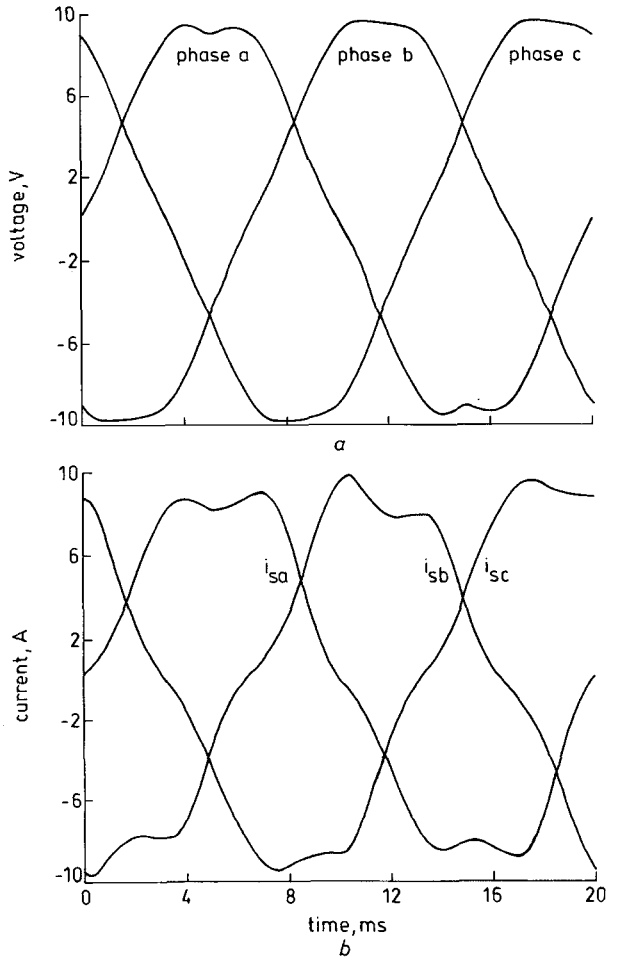

Fig. 8 *Measured three-phase supply-voltage waveforms and filtered line-current waveforms at input of experimental two-stage interleaved converter*
a Measured three-phase waveforms
b Filtered line-current waveforms

A calculated line-current waveform is shown in Fig. 2 for f_{LINE} and f_{SW} values chosen to be 50Hz and 3kHz, respectively, for illustration, and this is expanded at $\pi/6$ and $\pi/3$ (i.e. 1.67ms and 3.33ms) in Figs. 7*a* and 7*b*. In passing through $\pi/6$, the relative magnitudes of v_a and v_c change (see Fig. 8*a*), leading to a change in the relative duration of L_a and L_c reset. Near the second point of interest, $\pi/3$, v_c passes through zero. Hence, with f_{SW} far greater than f_{LINE}, i_C is approximately zero, and current waveforms are virtually determined by L_a, L_b, v_a and v_c, alone. Since the line-to-line voltage v_{ab} reaches a maximum at $\pi/3$, the peaks and widths of the corresponding current pulses are also maximal. Therefore, operating conditions at this point are put into eqns. 1 and 4, to calculate the maximum inductance that is permissible to place operation at the DICM/CICM boundary.

2.3 Line-current frequency spectra

The spectra of the normalised line-current waveforms, computed by the fast Fourier transform algorithm (Fig. 9) [9], show that low levels of f_{LINE} harmonics remain. The observable residual low-order harmonics (i.e. 5th, 7th, 11th, etc.) arise because, unlike for the current-rise periods of the current pulses, the current-time areas associated with inductor reset are determined by factors other than the phase voltages, and are not linearly dependent on phase voltage. Hence, they do not accurately follow a sinusoidal distribution, and nontriplen odd f_{LINE} harmonics are thus introduced.

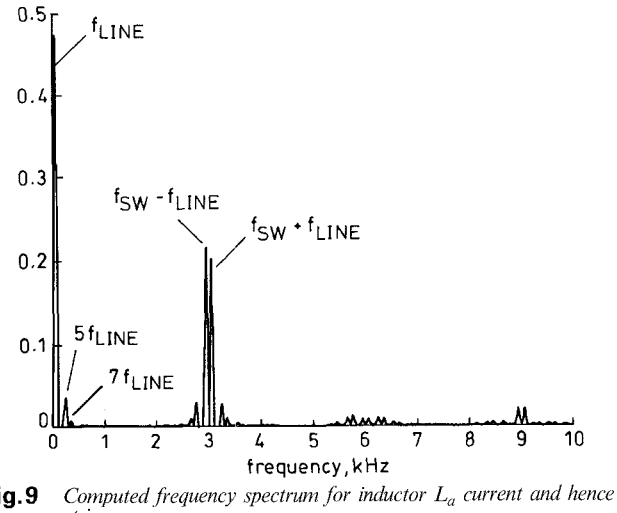

Fig. 9 *Computed frequency spectrum for inductor L_a current and hence line current i_{La}*

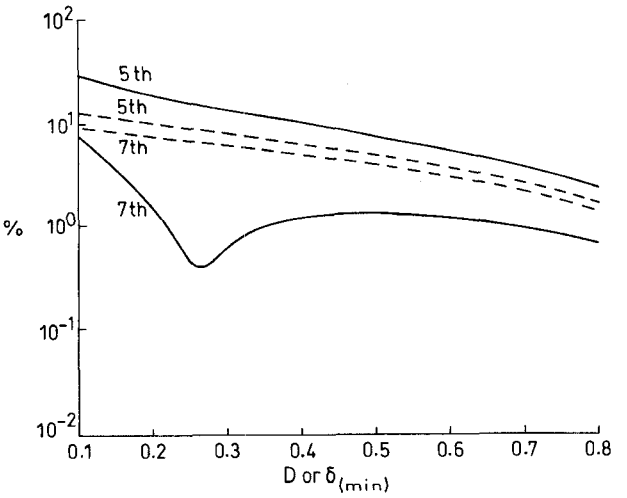

Fig. 10 *Computed variation in lowest-order residual line-current harmonics with duty ratio for both constant f_{SW} control and variable f_{SW} control methods*
——— constant switching frequency
– – – – variable switching frequency

The dominant f_{LINE}-harmonic levels vary with duty cycle as shown in Fig. 10. Since these are virtually independent of f_{SW} values above a certain value (i.e. $f_{SW}/f_{LINE} > 30$) [8], they limit the maximum improvement possible in power-factor correction and also power-converter capacity if the converter is required to comply with harmonic emission standards which set absolute limits. The fundamental f_{LINE} currents are virtually in phase with the three-phase supply voltages, and hence the power-factor values, shown by the constant switching frequency graph in Fig. 11, arise due to line-current distortion alone.

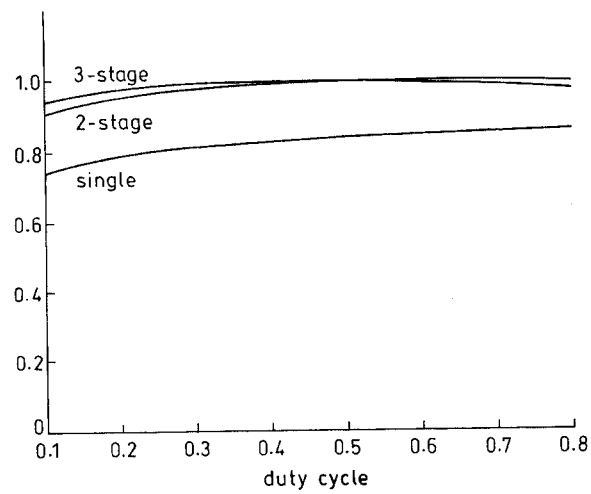

Fig. 11 *Computed variation in input power factor with duty cycle for single-stage, two-stage interleaved and three-stage interleaved three-phase boost converters for* $f_{SW}/f_{LINE} = 60$

3 Variable switching frequency control

The total RMS current associated with residual f_{LINE} harmonics may be reduced somewhat by using variable-frequency rather than constant-frequency control of the boost-cell switch, as proposed in [5]. This involves controlling the converter switch to minimise the zero-current periods in the discontinuous line-current waveforms (see Fig. 6*b*). With this control method, the point at which all line currents reach zero is detected and used to start the next conduction period of Q. Since the blocking time of Q is dependent on the current reset times t_{ir1} and t_{ir2}, which vary over the f_{LINE} period, the switching frequency of Q, i.e. $1/(DT_{SW} + t_{ir1} + t_{ir2})$, now varies. The conduction duty cycle of Q also varies cyclically above a minimum value δ_{min} [8].

Line-current waveforms for variable-frequency control may also be obtained, as previously described for constant f_{SW} operation [8], to allow a more complete analysis of line-current spectra than in previously used methods [5]. The 5th and 7th residual harmonic levels and the input power factor have been computed from the unfiltered line currents and overlaid in Figs. 10 and 12 for comparison with results for fixed f_{SW} control. Although both the low-frequency f_{LINE} and high-frequency f_{SW} related spectral content changes, the improvement in power factor, especially at low duty cycle, arises largely because of less reduction in the fundamental line-current amplitude. Reduction in the total RMS current associated with f_{LINE} harmonics and f_{SW} related components is less marked [8].

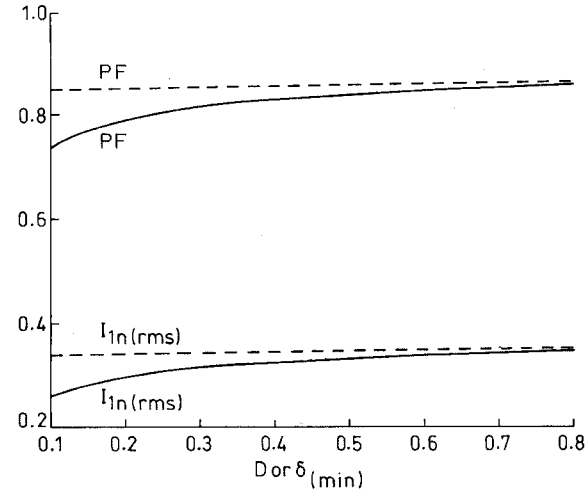

Fig. 12 *Computed variation in power factor assuming no input filtering and normalised fundamental input current* $I_{1n(rms)}$ *against duty cycle for control methods*
$f_{SW}/f_{LINE} = 60$ for constant f_{SW} control
——— constant switching frequency
– – – – variable switching frequency

4 Interleaved operation of converters

The high level of f_{SW} related ripple in the line currents of the single-switch converter, in particular, produces a significant reduction in power factor. This is generally greater than twice the fundamental line-frequency amplitude (see Figs. 2 and 3) and more than an order of magnitude higher than that commonly found in CICM converters. The higher values of input-filter components required compromise the potential passive-component-volume and dynamic-response advantages of the discontinuous converter. With fixed f_{SW} control, however, this problem may be virtually eliminated by parallel connecting two or more converters and interleaving their switching. Ripple cancellation by interleaving variable f_{SW} waveforms gives less reliable results and hence the variable f_{SW} method of control will not be considered further. The advantages of interleaved converter operation have previously been applied to single-phase power-factor preregulators with DICM [6] and CICM [7] operation, and to six-switch converters [10], but not to three-phase single-switch converters.

A two-stage parallel converter is given in Fig. 1. If the control pulses applied to the main switches are synchronous and optimally phase shifted by half an f_{SW} period, the input and output ripple frequency is effectively doubled and the ripple amplitude is reduced by a factor greater than two (cf. Figs. 2 and 13). As well as alleviating the input and output filtering requirements, the line-inductor and output filter capacitor volume are reduced for a given output power because the total peak energy stored in the circuit inductance is halved. The reduced current-pulse amplitudes and increased ripple frequency in the composite output of the boost cells, also, reduce the excess required in the value and rating of the output filter capacitor, above that determined by $6\,f_{LINE}$ ripple-current considerations alone.

For N interleaved converters the optimal phase difference between boost cells is $1/N$ times the f_{SW} period [6], the peak energy stored in the $3N$ line-inductors is reduced by $1/N$, and input and output current ripple frequency and amplitude are increased to $N\,f_{SW}$ and reduced below $\Delta I/N$, respectively. In principle, con-

verter passive component volume or single-cell f_{SW} may therefore be progressively reduced by increasing the number of interleaved cells (cf. Figs. 2, 13 and 14).

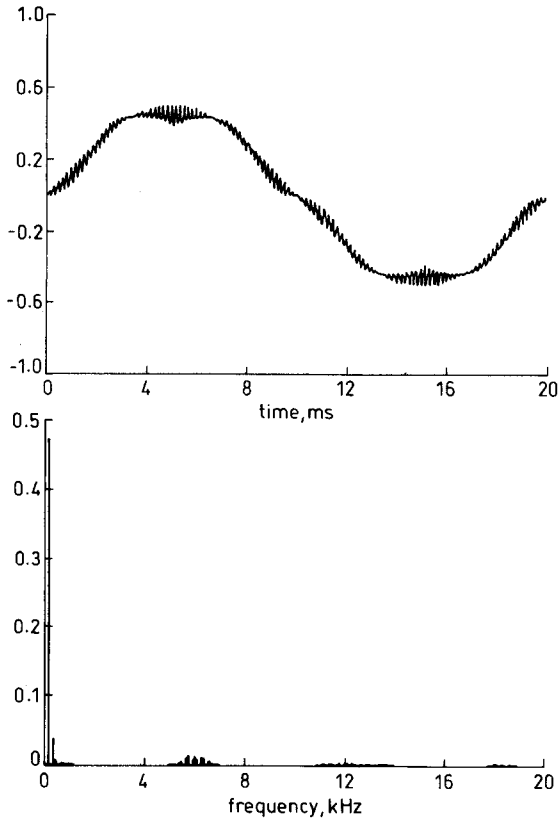

Fig. 13 *Computed composite phase-a line-current waveform and spectrum for interleaved two-stage converter operation, at f_{SW} = 3kHz and D = 0.5, showing ripple-frequency multiplication and ripple-amplitude reduction*

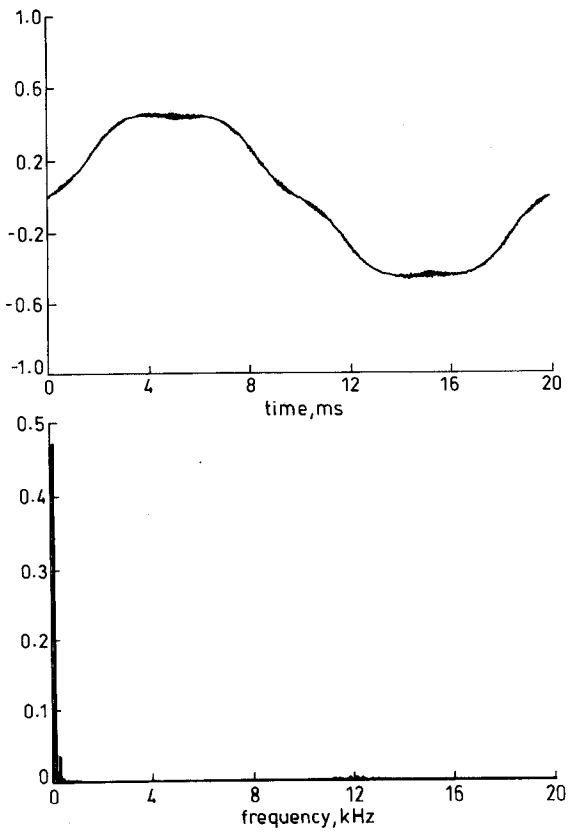

Fig. 14 *Computed composite phase-a line-current waveform and spectrum for interleaved four-stage converter operation, at f_{SW} = 3kHz and D = 0.5, showing ripple-frequency multiplication and ripple-amplitude reduction*

4.1 Interleaved operation of parallel-connected converters

In principle, any number of single-switch three-phase boost-converters may be connected for interleaved switching, provided one additional fast recovery diode per stage is added to prevent undesirable converter interaction, e.g. D_{b3} and D_{b4} in Fig. 1. For without these, when Q_1 is on, a proportion of forward current set up in L_{a1} to L_{c1} may return through L_{a2}, L_{b2} and L_{c2}, and vice versa when Q_2 is on.

Normalised line-current waveforms and their frequency spectra are calculated for multiple interleaved switching converters, as previously outlined for the single-stage converter, and are shown in Figs. 13 and 14. Comparing the normalised current waveforms and spectra for the two- and four-stage interleaved converters with the single-stage converter shows not only the multiplication of effective f_{SW}, but also the reduction in f_{SW} related current. Principal current-ripple frequency components vary with duty cycle. The total ripple cancellation effect and how it varies with duty cycle is best seen from the input power factor calculated from the unfiltered normalised line current (Fig. 11), since this takes into account all frequency components. Phase displacement of the fundamental line current is negligible; as is the variation in f_{LINE} harmonic distortion with f_{SW}, once the carrier frequency ratio is above 30 [8]. Hence, the significant improvement in power factor seen is almost entirely due to the ripple cancellation resulting from interleaved converter operation.

A less marked current ripple and thus power-factor improvement is obtained by adding more than two stages, although the potential to reduce filter and line-inductance volume or decrease the fundamental f_{SW} remain because the ripple frequency to f_{SW} ratio continues to rise. The actual reduction in output-filter-capacitor high-frequency RMS current varies below $1/N$ because of the change in composite ripple shape as well as its amplitude. At duty cycles likely to be used in practical 380–480V three-phase systems, i.e. $D \leq 0.5$, the reduction is generally greater than $1/N$ [8].

4.2 Converter component sizing

The previous results apply at any power level because they are based on normalised waveforms. However, to verify them it is necessary to design converters to operate at specific power levels. Different circuit operating conditions may be simulated using the previous analysis technique to produce relatively uncomplicated design data. For example, the maximum permissible line inductance is readily determined from the precalculated graph of peak fundamental line current $\hat{I}_1$ normalised to a base of peak inductor current $\hat{I}_{L(max)}$, shown in Fig. 3 and eqns. 1 and 4. The relationship between $\hat{I}_1$ and $\hat{I}_{L(max)}$ remains virtually constant once the carrier-frequency ratio exceeds a certain value (e.g. $f_{SW}/f_{LINE} \geq 30$ [8]). A single graph may, therefore, be used to find the maximum allowable line inductance to always give DICM operation. This considerably simplifies the determination of line inductance L_a to L_c values over previously documented methods [3, 4].

For single power-stage circuit design, the maximum duty cycle is obtained by using eqn. 1 with the minimum operating voltage-conversion ratio likely to be experienced. This fixes an abscissa on Fig. 3 and hence the $\hat{I}_1/\hat{I}_{L(max)}$ value. Converter power capacity sets I_1, and hence the absolute value of $\hat{I}_{L(max)}$, and T_{SW} is

fixed by the optimum switching frequency for the power-semiconductor technology used. The maximum value of L is then obtained by solving eqn. 4 at $\omega t_k = \pi/3$, when v_C is zero and a single period of inductor reset occurs (see Fig. 7*b*).

Normalised circuit current waveforms may also be used to produce average and RMS current for the power semiconductors and other passive components, from which component current ratings and power dissipation may be determined [11].

The design procedure and data are equally valid in the design of single-switch converters for parallel connection, since operation is similar except that total power capacity and peak inductor current are divided by N, and line inductance is multiplied by N.

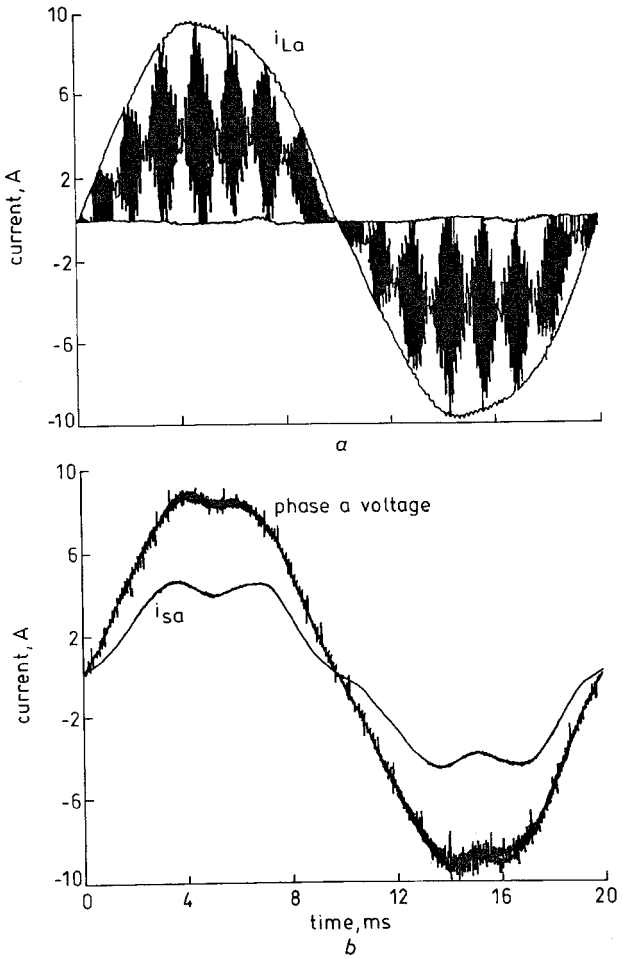

Fig. 15 *Measured phase-a inductor current and filtered line current and phase voltage for experimental single-stage converter*
a Inductor current
b Line current and phase voltage

5 Practical verification of analysis

To validate analytical results and the design methods two single-switch three-phase boost converters were designed for connection and operation as in Fig. 1. Boost-cell components were set at $L_a = L_b = L_c \simeq 170\mu H$, $C_d = 200\mu F$ and $R_L = 60\Omega$ for DICM operation under the following conditions: $V_S = 50V$, $V_O = 245V$, $P_O = 1kW$, $f_{LINE} = 50Hz$ and $f_{SW} = 20kHz$.

The experimental results obtained with these are somewhat marred by distortion and imbalance in the laboratory three-phase supply system used, although this does have the advantage of illustrating the system's vulnerability to supply voltage distortion. Fig. 8*a* shows signals proportional to the synthesised 87V three-phase supply voltages which were derived from a 415V supply system using an isolation transformer and variac.

Examination of the phase-*a* discontinuous line-current waveform i_{La} for a single-stage converter on a 50MHz analogue oscilloscope confirmed that operation is fully discontinuous and the system was properly designed. However, the i_{La} waveform included here in Fig. 15*a* was recorded on a digital oscilloscope, and the crest ripple and apparent incomplete current reset to zero, either side of the sinewave peak, results from the relatively low oscilloscope sampling rate. A second-order input filter effect with $f_B \simeq 5kHz$ is provided by the transformer leakage inductance, and added line-to-line capacitance C_f removes the high-frequency current ripple while producing very little phase shift between line currents and phase voltages, as shown in Fig. 15*b*. The remaining odd line-frequency harmonics, mainly 5th, are largely unaffected by the 5kHz lowpass filter, and their effect is apparent in the filtered line currents (see Fig. 15*b*). Spectral analysis of the practical discontinuous line current gave frequency-component amplitudes which were in good agreement with the results predicted by computation [8].

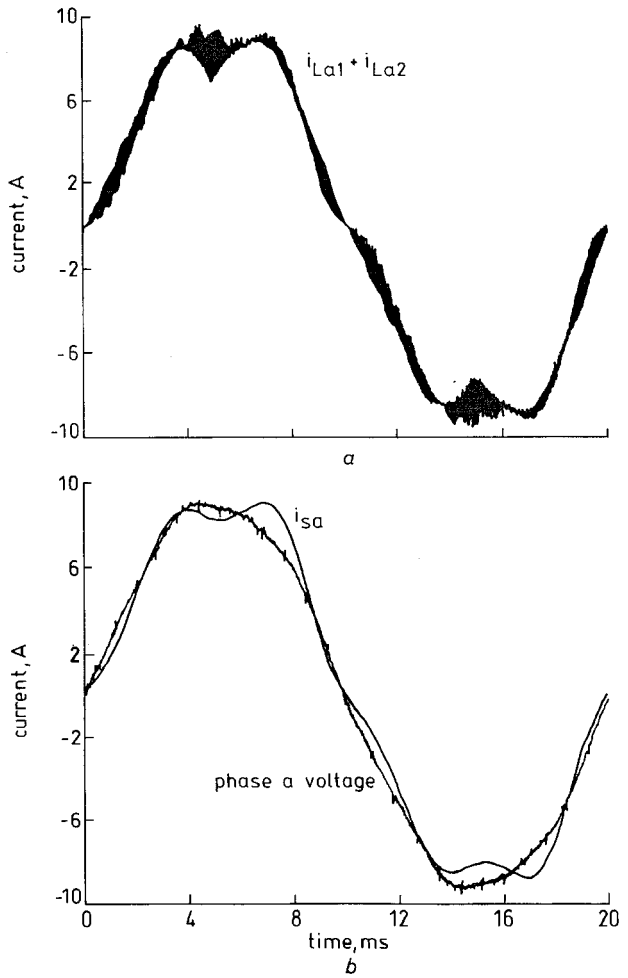

Fig. 16 *Measured phase-a inductor current and filtered line current and phase voltage for experimental two-stage interleaved converter*
a Inductor current
b Line current and phase voltage

5.1 Practical results for interleaved operation

For interleaved operation, the two single-stage circuits were parallel connected and operated open-loop into a resistive load. The constant duty cycle IGBT drives were phase shifted by $f_{SW}/2$. The composite phase-*a*

unfiltered and filtered line currents are shown in Fig. 16 and the three filtered line currents are given in Fig. 8*b* with the corresponding phase voltage waveforms. The line current frequency spectra before and after interleaving are shown in Fig. 17 and confirm that artificial switching frequency multiplication and a high level of ripple reduction is indeed possible in practice. Comparing Figs. 17*a* and 17*b* shows that ripple frequency components at the fundamental converter switching frequency (i.e. ~20kHz) are virtually eliminated, and, although converter power capacity has been doubled as shown by the factor of 2 increase in fundamental f_{LINE} current, the residual line-current ripple at Nf_{SW} (i.e. 40kHz) is low and comparable with levels found in CICM converters. The frequency spectra for the filtered line currents, when expanded, reflect the imbalance in source voltages, impedances and converter per-phase circuits. In consequence, fundamental and harmonic line-current levels differ and low levels of third harmonic are introduced into line currents [8].

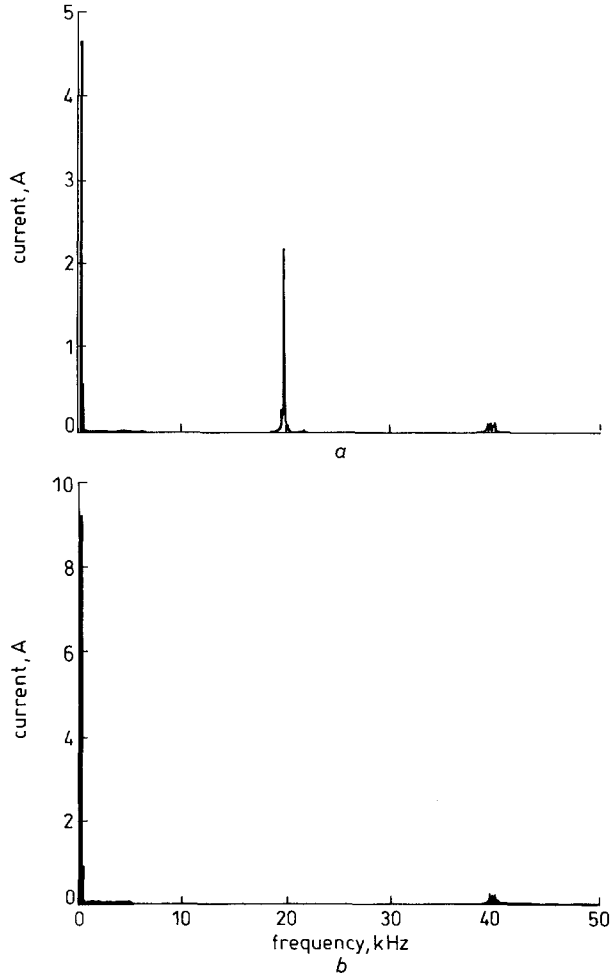

Fig. 17 *Frequency spectra computed from unfiltered phase-a line currents in experimental single-stage and two-stage interleaved converters*
a Single-stage converter
b Two-stage interleaved converter

6 Conclusions

By connecting a single-switch boost converter after a three-phase rectifier, and operating it in the DICM mode at constant switching frequency and duty cycle, pulsed line currents with an approximately sinusoidal average current may be naturally drawn from a three-phase supply. Control circuit requirements are relatively simple and, since the circuit employs small reactive components, it is potentially capable of very fast response to changing operating conditions. The disadvantages of the circuit include: the supply voltage distortion has a direct influence on line-current distortion; residual f_{LINE} harmonics cannot be reduced below a certain level by raising f_{SW} or control-loop bandwidth, as is the case in principle with six-switch CICM power-factor correction preregulators; the circuit draws pulsed line currents under a sinewave envelope greater than twice the fundamental current amplitude, necessitating heavy input filtering below f_{SW}; and circuit analysis and design to ensure proper DICM operation under a range of operating conditions is difficult.

Some of the disadvantages have been addressed here. A method of analysis is presented and verified which allows both f_{LINE} and f_{SW} components of the unfiltered line-current frequency spectra to be computed. As a result, the levels of residual f_{LINE} harmonics and f_{SW} related components may both be studied to assess compliance with standards or to design input filters. Also, normalised design graphs have been produced to considerably simplify boost-cell inductor and capacitor selection for DICM operation. The problems associated with switching and drawing high line-current peaks have been addressed by devising a simple method of parallel connecting a number of boost stages and interleaving their switching. With interleaved converters, an equivalent device silicon area is in principle required, and the main reactive-component volume associated with the boost-cell and input-filter reactive components is reduced. Also, good current sharing between converters is naturally obtained.

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8 Appendixes

8.1 Switch utilisation ratio

The switch utillsation ratio SUR, defined for inverter topologies in [12] and given by eqn. 9, is used here to estimate the relative silicon cost of power-factor correction preregulator topologies:

$$\mathrm{SUR} = \frac{(VA)_1}{qV_T I_T} \tag{9}$$

$(VA)_1$ is the converter volt-ampere capacity at the fundamental line frequency f_{LINE}, and V_T and I_T are the theoretical peak voltage and current ratings, respectively, required by the q converter switches to achieve this, assuming idealised, 100% efficient, converter operation.

$$M = \frac{V_O}{\hat{V}} = \frac{1}{1-D} \tag{10}$$

The power-factor correction preregulators incorporate boost-converter switching cells. Hence, converter output voltage V_O has a direct bearing on switch voltage rating, and the voltage-conversion ratio term M must be incorporated in V_T (see eqn. 10, where $\hat{V}$ is the peak fundamental line-neutral in single-phase systems and the peak fundamental line-to-line voltage in three-phase systems). Converter switch current rating I_T is determined by the peak controlled current, and, since current ripple increases this, a ripple term r may be incorporated in I_T (see eqn. 11, where I_S is the fundamental input line current and ΔI_S is the peak ripple magnitude above this):

$$r = 1 + \frac{\Delta I_S}{\hat{I}_S} \tag{11}$$

The relative SUR values for (i) the CICM, single-phase, power-factor correction preregulator based on the boost converter; (ii) CICM, three-phase, six-switch converter; and (iii) DICM, three-phase, single-switch converter are given in Table 1. In the CICM converters, current ripple may, in principle, be rendered negligible by choosing a very high f_{SW} value. Hence, a unity r value is used for CICM converters which gives the theoretical upper limit for SUR. In the DICM case, because current ripple is very high and is virtually independent of f_{SW} above a certain f_{SW}/f_{LINE} ratio, it must be taken into account. The variation in current-ripple amplitude with duty cycle must also be considered. Normalised peak-current values for a range of D may be calculated from the data in Fig. 3, and are used to calculate the maximum achievable SUR over the duty-cycle range, $0.1 \leq D \leq 0.8$.

Table 2: Coefficients for state eqn. 5 for different intervals of the f_{LINE} period

ωt	0–π/3	π/3–2π/3	2π/3–π	π–4π/3	4π/3–5π/3	5π/3–2π
α_{1a}	1/3	2/3	1/3	−1/3	−2/3	−1/3
α_{1b}	−2/3	−1/3	1/3	2/3	1/3	−1/3
α_{1c}	1/3	−1/3	−2/3	−1/3	1/3	2/3

8.2 State equation solutions

Normalisation bases:

$i_{Lkn} = i_{Lk}/\hat{I}_L$ where $\hat{I}_L = (\hat{V}/L)DT_{SW}$, assuming $L_k = L$, $\hat{V} = \hat{V}_{phk}$ and $k = a$, b or c.

$t_n = t/DT_{SW}$, $\omega = 2\pi f_{LINE}$

During the first interval, $0 \leq \omega t_i < \pi/6$, the absolute value of phase voltage v_a is the smallest and v_b is the highest, and Fig. 4*a* applies. During the switch on-time DT_{SW}, inductor currents increase to peak values given by eqns. 12–14, at rates determined by eqn. 2. The peak values occur at times t_{i1} within the switching periods (see Fig. 6*a*) and are given by eqns. 15–17.

$$i_{Lan}(t_{i1}) = \sin(\omega t_i) \quad t_i = (i-1+D)T_{SW},\ i = 1, 2, \ldots, p \tag{12}$$

$$i_{Lbn}(t_{i1}) = \sin\left(\omega t_i - \frac{2\pi}{3}\right) \tag{13}$$

$$i_{Lcn}(t_{i1}) = \sin\left(\omega t_i - \frac{4\pi}{3}\right) \tag{14}$$

When the switch is turned off, the first inductor reset period, t_{ir1}, starts, and the inductor currents decrease over $t_{i1} < t < t_{i2}$ at rates given by eqn. 5 and the appropriate coefficient values from Table 2. Eqns. 15–17 give these for the first interval of the f_{LINE} period:

$$\left(\frac{di_{Lan}}{dt_n}\right)_{i12} = \sin(\omega t_i) - \frac{M}{\sqrt{3}} \quad \text{since } \alpha_{1a} = 1/3 \tag{15}$$

$$\left(\frac{di_{Lbn}}{dt_n}\right)_{i12} = \sin\left(\omega t_i - \frac{2\pi}{3}\right) + \frac{2M}{\sqrt{3}} \quad \text{since } \alpha_{1b} = -2/3 \tag{16}$$

$$\left(\frac{di_{Lcn}}{dt_n}\right)_{i12} = \sin\left(\omega t_i - \frac{4\pi}{3}\right) - \frac{M}{\sqrt{3}} \quad \text{since } \alpha_{1c} = 1/3 \tag{17}$$

These apply until the lowest inductor current reaches zero; for example, see i_a at t_{i2} in Fig. 6*a*. This marks the end of the first inductor reset period, t_{ir1}. Now, putting eqns. 12 and 15 into eqn. 18 gives t_{ir1n} values for sampling instants within the first $\pi/6$ interval of the line-current waveforms:

$$i_{Lan}(t_{i1}) + \left(\frac{di_{Lan}}{dt_n}\right)_{i12} t_{ir1n} = 0 \tag{18}$$

Table 1: Relative SUR values for correction converters and data used in their evaluation

Converter type	Switch number q	Power capacity $(VA)_1$	Switch voltage rating V_T	Switch current rating I_T	Current ripple factor r	SUR	SUR/SUR$_{1PH}$
CICM Single-phase boost	1	$V_S I_S$	$\sqrt{2}V_S M$	$\sqrt{2}I_S$	1	$1/2M$	1
CICM Six-switch three-phase	6	$3V_S I_S$	$\sqrt{6}V_S M$	$\sqrt{2}I_S$	1	$1/6(2/\sqrt{3})M$	0.29
DICM Single-switch three-phase boost	1	$3V_S I_S$	$\sqrt{6}V_S M$	$\sqrt{2}rI_S$	$0.1 \leq D \leq 0.8$ 2.76–2.04	$1/(2/\sqrt{3})rM$	$0.1 \leq D \leq 0.8$ 0.63–0.85

Table 3: Coefficients for state eqn. 7 for different intervals of the f_{LINE} period

ωt	0–π/6	π/6–π/3	π/3–π/2	π/2–2π/3	2π/3–5π/6	5π/6–π
α_{2a}	0	1/2	1/2	1/2	1/2	0
α_{2b}	−1/2	−1/2	−1/2	0	−1/2	1/2
α_{2c}	1/2	0	0	−1/2	0	−1/2
X_a	0	1	1	1	1	0
X_b	−1	−1	−1	0	−1	0
X_c	1	0	0	−1	0	−1
ωt	π–7π/6	7π/6–4π/3	4π/3–3π/2	3π/2–5π/3	5π/3–11π/6	11π/6–2π
α_{2a}	0	−1/2	−1/2	−1/2	−1/2	0
α_{2b}	1/2	1/2	1/2	0	0	−1/2
α_{2c}	−1/2	0	0	1/2	1/2	1/2
X_a	0	−1	−1	−1	−1	0
X_b	1	1	1	0	0	−1
X_c	−1	0	0	1	1	1

$$\Rightarrow \sin(\omega t_i) + \left[\sin(\omega t_i) - \frac{M}{\sqrt{3}}\right] \cdot t_{ir1n} = 0 \quad (19)$$

$$\Rightarrow t_{ir1n} = -\frac{\sin \omega t_i}{\sin \omega t_i - \frac{M}{\sqrt{3}}} \quad (20)$$

To determine the duration of the second inductor reset period, inductor currents $i_{Lbn}(t_{i2})$ and $i_{Lcn}(t_{i2})$ are first estimated using eqns. 21–24:

$$i_{Lbn}(t_{i2}) = i_{Lbn}(t_{i1}) + \left(\frac{di_{Lbn}}{dt_n}\right)_{i12} t_{ir1n} \quad (21)$$

$$\Rightarrow i_{Lbn}(t_{i2}) = \sin\left(\omega t_i - \frac{2\pi}{3}\right) + t_{ir1n}\left[\sin\left(\omega t_i - \frac{2\pi}{3}\right) + \frac{2M}{\sqrt{3}}\right] \quad (22)$$

Similarly,

$$i_{Lcn}(t_{i2}) = i_{Lbn}(t_{i1}) + \left(\frac{di_{Lbn}}{dt_n}\right)_{i12} t_{ir1n} \quad (23)$$

$$\Rightarrow i_{Lcn}(t_{i2}) = \sin\left(\omega t_i - \frac{4\pi}{3}\right) + t_{ir1n}\left[\sin\left(\omega t_i - \frac{4\pi}{3}\right) - \frac{M}{\sqrt{3}}\right] \quad (24)$$

At the end of t_{ir1}, i_{La} is zero, and hence i_{Lbn} and i_{Lcn} are equal in magnitude but opposite in sign (see Figs. 5*a* and 6*a*). During the second inductor reset period, t_{ir2}, i_{Lbn} and i_{Lcn} fall at the new rates given by eqn. 7 and the coefficients in Table 3. These are given for each phase in eqns. 25 and 26:

$$\left(\frac{di_{Lbn}}{dt_n}\right)_{i23} = \frac{\sqrt{3}}{2}\left[\sin\left(\omega t_i - \frac{\pi}{2}\right) + M\right] \quad (25)$$

$$\left(\frac{di_{Lcn}}{dt_n}\right)_{i23} = \frac{\sqrt{3}}{2}\left[\sin\left(\omega t_i + \frac{\pi}{2}\right) - M\right] \quad (26)$$

To estimate t_{ir2n}, phase-*b* inductor current, i_{Lbn}, is considered further. At the end of t_{ir2}, i_{Lbn} falls to zero and eqn. 27 applies:

$$i_{Lbn}(t_{i2}) + \left(\frac{di_{Lbn}}{dt_n}\right)_{i23} t_{ir2n} = 0 \quad (27)$$

Substituting eqns. 22 and 25 into eqn. 27 gives eqn. 28:

$$t_{ir2n} = -\frac{\left\{\sin\left(\omega t_i - \frac{2\pi}{3}\right) + t_{ir1n}\left[\sin\left(\omega t_i - \frac{2\pi}{3}\right) + \frac{2M}{\sqrt{3}}\right]\right\}}{\frac{\sqrt{3}}{2}\left[M + \sin\left(\omega t_i - \frac{\pi}{2}\right)\right]} \quad (28)$$

Using eqn. 28, values for the second inductor reset period, t_{ir2n}, may be estimated at any sampling instant within the first f_{LINE} interval. Equations for all salient amplitudes and periods are now available, and solving these allows line-current waveforms and other circuit waveforms to be constructed for the first π/6 interval. To fully compute the line-current waveforms over an entire f_{LINE} period as shown in Fig. 2, 12 such sets of equations must be derived and solved [8].

8.3 Generalised state equation coefficients

The values of coefficients α_{1k}, α_{2k} and X_k in the generalised state eqns. 10–16 are dependent on the interval in the f_{LINE} period in which operation is taking place, as shown in Tables 2 and 3.