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**PARALLEL FABRICATION AND TRANSPORT PROPERTIES OF
CARBON NANOTUBE SINGLE ELECTRON TRANSISTORS**

by

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M.S. University of Central Florida, 2011

A dissertation submitted in partial fulfillment of requirements
for the degree of Doctor of Philosophy
in the Department of Physics
in the College of Sciences
at the University of Central Florida
Orlando, Florida

Spring Term
2015

Major Professor: Saiful I. Khondaker

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ABSTRACT

Single electron transistors (SET) have attracted significant attention as a potential building block for post CMOS nanoelectronic devices. However, lack of reproducible and parallel fabrication approach and room temperature operation are the two major bottlenecks for practical realization of SET based devices. In this thesis, I demonstrate large scale single electron transistors fabrication techniques using solution processed single wall carbon nanotubes (SWNTs) and studied their electron transport properties. The approach is based on the assembly of individual SWNTs via dielectrophoresis (DEP) at the selected position of the circuit and formation of tunnel barriers on SWNT. Two different techniques: i) metal-SWNT Schottky contact, and ii) mechanical templating of SWNTs were used for tunnel barrier creation.

Low temperature (4.2K) transport measurement of 100 nm long metal-SWNT Schottky contact devices show that 93% of the devices with contact resistance (R_T) $> 100 \text{ K}\Omega$ show SET behavior. Majority (90%) of the devices with $100 \text{ K}\Omega < R_T < 1 \text{ M}\Omega$, show periodic, well-defined Coulomb diamonds with a charging energy $\sim 15 \text{ meV}$, represents single electron tunnelling through a single quantum dot (QD), defined by the top contact. For high R_T ($> 1 \text{ M}\Omega$), devices show multiple QDs behaviors, while QD was not formed for low R_T ($< 100 \text{ K}\Omega$) devices. From the transport study of 50 SWNT devices, a total of 38 devices show SET behavior giving an yield of 76%.

I also demonstrate room temperature operating SET by using mechanical template technique. In mechanical template method individual SWNT is placed on top of a Al/Al₂O₃ local gate which bends the SWNT at the edge and tunnel barriers are created. SET devices fabricated

with a template width of ~ 20 nm shows room temperature operation with a charging energy of ~ 150 meV. I also discussed the detailed transport spectroscopy of the devices.

To my wife and parents

ACKNOWLEDGMENTS

I would like to express my sincere gratitude my supervisor, mentor, and guide, Dr. Saiful Khondaker, for encouraging me to pursue a topic of my choice and helping me in every possible way. His constructive comments, wisdom and commitment to the highest standards inspired and motivated me. Without his active help and support this thesis could not have been written. Dr. Lee Chow, Dr. Sergei Stolbov, and Dr. Lei Zhai thank you for the encouragement, time and attention.

I would like to thank my fellow coworkers. In particular, I would like to acknowledge Dr. Paul Stokes who taught me the low temperature measurement for SET. I would also like to thank Dr. Daeha Joung for teaching me the device fabrication as soon as I join this group, as well as working together on many research projects. Thanks to Dr. Biddut Sarker, Dr. Feras Alzubi, Narae Kang, Udai Bhanu, Kristy Kormondy, Eliot Silbar, Dr. Shashank Shekhar, Dr. Mohammad Arif, Dr. Surajit Ghosh, Dr. Tanusri Pal, for sharing their enthusiasm and comments on my work.

I have many friends who have encouraged and supported me during the five years of graduate school. I would like to thanks Alamgir Kabir, Abrar Quadery, Rizvi, and Satez for their warmth and generosity.

I would like to thank my parents for their persistent support and sacrifice for my education and research, I cannot thank you enough. Last but not the least; I would like thank Zareen, my wife, for enduring my irregular working hours as a graduate student. Her emotional support was of immense help. This thesis is dedicated to you.

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
CB	Coulomb Blockade
CO	Coulomb Oscillation
CD	Coulomb Diamond
CMOS	Complementary Metals Oxide Semiconductor
CNT	Carbon Nanotube
CVD	Chemical Vapor Deposition
DEP	Dielectrophoreis
DI	Deionized
EBL	Electron Beam Lithography
FET	Field Effect Transistor
IPA	Isopropyl-alcohol Methyl-isobutyl-ketone
LOR	Lift-off-Resist
MIBK	Methyl-isobutyl-ketone
MOS	Metals Oxide Semiconductor
m-SWNT	Metallic single walled carbon nanotube
MWNT	Multiwalled cabon nanotube
NPGS	Nano-Patterned- Generation-System
NPs	Nanoparticles
QD	Quantum Dot

SET	Single electron transistor
SWNT	Single walled carbon nanotube
s-SWNT	Semiconducting single walled carbon nanotube
SB	Schottky Barrier
SEM	Scanning Electron Microscopy

CHAPTER 1: INTRODUCTION

1.1 Motivation

The origin of modern electronics traces back to the innovation of transistor by Bardeen, Brattain and Shockley in 1947. This leads to the discovery of integrated circuit (IC) in 1958-59, which provides a means of logic and computation. Shortly after that Metal oxide semiconductor (MOS) transistor and Complimentary MOS (CMOS) (1963) were demonstrated which lead to a revolution in the field of electronics. Since then progress has made for scaling down the size of the transistors to increase the density of logic and memory in the chip. The number of transistor per chip is doubling roughly in every 18 month as devised by Moore's law [1] leading to the device fabrication upto submicron level (figure 1.1). The miniaturization of transistor size together with the ease of fabrication made Si-based CMOS technology as workhorse for modern electronics. However, scaling down of transistor below sub 100 nm generates several fundamental challenges including short channel effects, gate oxide leakage, increased off state current, high field mobility degradation, and high power dissipation etc [2-4]. By introducing new gate oxide materials, and innovative circuit design, researches are able to overcome those problems and thus transistor size as small as 14 nm is expected to be available by the end of 2014. If the Moore's law continues unabated and the miniaturization of transistor continues at this rate, by 2030 the size of transistor would reach atomic dimension. At such small device geometry, the quantum nature of electron will play significant role in the device operation and classical laws would no longer be applicable [5]. With the miniaturization of transistor, high

speed operation is achieved by increasing the density of components; however it leads to an increased generation of heat.

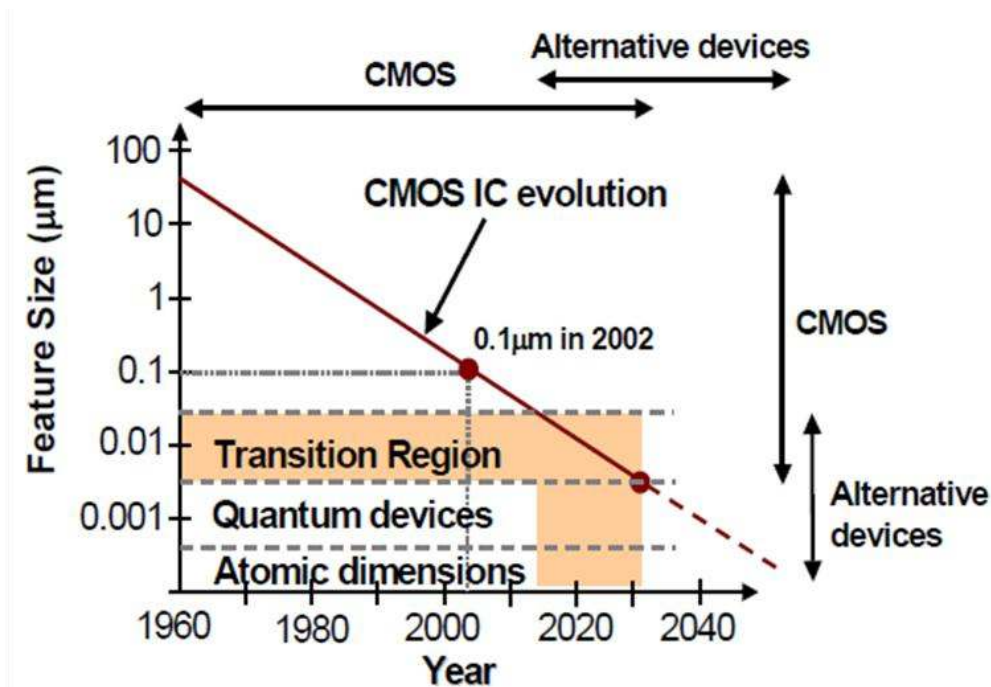


Figure 1.1 History and future of CMOS scaling. Image taken from ref [6].

Figure 1.2 shows the amount of power dissipated per unit area, with successive technology nodes. The reliability and performance of the devices are greatly affected by the increased amount of heat generation. With reduction of device size, electron tunnel through the barriers leading to an unexpectedly high leakage current. In addition, fabrication of such minuscule devices require complex design, high resolution lithography, and tight process controls which increases the manufacturing cost of the devices.

Thus, in the near future Moore's law will reach a dead end and the CMOS technology will lose its dominance in modern semiconductor industry. An innovative approach with new device

physics and promising device architecture is required which could replace the conventional CMOS technology.

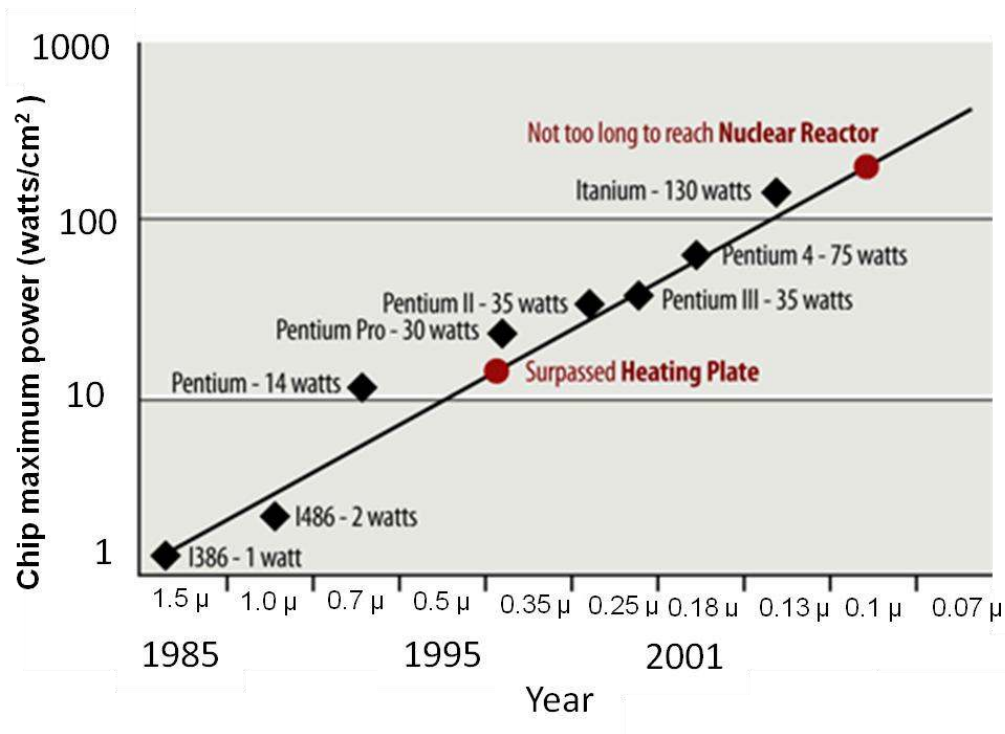


Figure 1.2 Power dissipation with technology node. Images are taken from ref [7]

The device operation should implement the quantum mechanical phenomena that arise during nanoscale dimensions. A number of emerging technologies and devices including, single electron transistors (SET), resonance tunnel diodes (RTD), spin transistor, molecular devices have been proposed for memory and logic operation as a replacement of current CMOS technology [8]. Among them SETs are considered as most promising replacement for the post CMOS era electronic devices. In an SET the electron transport is controlled by quantum tunneling [9, 10].

SET has several advantages over the conventional Si technology which includes ultra-low power consumption, scalability down to the sub-nanometer range, and ability to detect an

extremely small amount of charge (single electron) [5, 10]. SET has shown potential for different device application including logic circuits, memory devices, and sensors [11-20]. Therefore, those advantages make SET a potential candidate as the basic element for quantum information processing system.

Although SETs have shown great potential, practical implementation of SET based devices is still in its infancy and face several challenges. The major challenge in the fabrication involves controlled fabrication of reproducible quantum dot (QD), the basic component of SET. So far different techniques has been developed to fabricate SET which includes lithographically defined QD in a GaAs/AlGaAs heterojunctions, direct etching of Si substrate, silicon on insulator (SOI) with pattern dependent oxidation, metallic grains in nanopore, and chemically synthesized colloidal nanocrystals [21-27]. However, such techniques involve complex fabrication steps, lack of reproducibility, low temperature operation, and inability for large scale fabrication, which have made those techniques unsuitable for practical application of SET based devices. For the practical realization of SET based devices several issues need to be addressed : i) the fabrication method need to be controllable and should give reproducible results, ii) the fabrication technique should be compatible with the conventional large-scale integration techniques, and iii) the SET devices should work at room temperature. In particular, parallel and controllable SET fabrication technique together with reproducible size of QD is also necessary to meet those challenges.

A possible route for the scalable and CMOS-compatible fabrication of SET is to use single wall carbon nanotubes (SWNTs) as QD. SWNTs, atomically thin layer of graphite (graphene) rolled up into a cylinder, is a true 1D material, show unique electronic, mechanical, and optical properties [28-34]. The very small dimension (diameter \sim 1-2 nm) of SWNT makes them a

suitable choice for SET as such a small feature is unattainable by conventional lithography techniques. Although SWNTs have shown potential as a QD, for the practical realization of SWNT based SET devices several issues need to be resolved. One of the major challenges is to find out reliable techniques for the assembly of individual SWNT which is compatible with the conventional CMOS technologies. Besides, absence of scaled up and reliable tunnel barrier fabrication technique is another major concern. Different techniques including AFM manipulation, deposition of top gate, FIB or ion induced damage etc. had been used to create tunnel barrier on SWNT to fabricate SET.[35-38] However in those technique SWNTs are assembled either by the chemical vapor deposition (CVD) growth or by random dispersion. During CVD process SWNTs grows at a high temperature (~ 900 °C) and hence is not CMOS-compatible. On the other hand, a large scale assembly is not possible using random dispersion as the alignment of individual SWNT depends on luck. Besides, their complicated design and lack of controllability on QD size make them only useful for proof-of-concept fabrication techniques and is unsuitable for parallel fabrication of SET based device.

In this thesis, I will demonstrate scalable, CMOS-compatible fabrication of SET using SWNT. We will use AC-dielectrophoresis, a large scale assembly technique to align individual SWNT between prefabricated source, and drain electrodes. I will use two different techniques to create tunnel barrier on SWNT: *i*) metal-SWNT Schottky contact, and *ii*) mechanical template. Subsequently, the low temperature transport measurement demonstrates that large scale assembly of SWNT based SET is possible using those techniques. Furthermore, I will demonstrate fabrication of SET that works even at room temperature by scaling down of the size of QD using the mechanical template technique.

1.2 Outline of the thesis

Chapter 2 provides the background and basic theoretical concepts. I will begin with a detailed discussion on the electronic structure and properties of carbon nanotubes: the active material used for the fabrication of SET in our research. Subsequently, a short description of the components of SET including the concept of Coulomb blockade and the basic theory of single-electron tunneling will be introduced. Since high yield SET fabrication depends on the successful assembly of individual SWNT, the chapter will end with a discussion of different types of SWNT assembly techniques.

In chapter 3, I will discuss the device fabrication processes and electron transport measurement setups. In particular, I will discuss different steps of the fabrication of electrode patterns for the device integration using optical and electron beam lithography. This will be followed by the dielectrophoresis (DEP) assembly set-up used for the integration of the individual SWNT. Subsequently, the measurement setup will be discussed, including measurements needed for the electronic transport properties at cryogenic temperatures using ^4He cryostat.

In Chapter 4, I will demonstrate a technique for large scale assembly of SWNT devices. I use DEP to assemble SWNT between prefabricated contacts. By optimizing the DEP parameters it is possible obtain highest assembly yield. I will discuss the detailed electron transport properties of the SWNT devices.

In Chapter 5, I will discuss an approach for scalable and CMOS-compatible technique for the fabrication of SET. The approach includes assembly of individual SWNT via DEP followed by deposition of metal top contact. Details about the design, fabrication steps will be discussed in this chapter. The detailed electron transport properties of the top contact SET device at low temperature will also be discussed.

In chapter 6, we will present another novel technique for the scalable fabrication of SWNT SET by the mechanical template technique. Using this method large scale fabrication of SET is possible by aligning SWNT on mechanical template via DEP. We will explore the effect chirality on the mechanical templating of the SWNT by studying their transport properties at low temperature.

Technique for the fabrication of room temperature operating SET will be discussed in chapter 7. This can be achieved by scaling down the size of carbon nanotube to sub-40 nm. We scale down the width of mechanical template to reduce and control the size of QD.

In Chapter 8, I will suggest future research directions related to my work and also discuss possible experiments.

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CHAPTER 2: BACKGROUND¹

2.1 Carbon nanotubes

Carbon, a remarkable element, offers the extraordinary opportunity to investigate a material in all possible dimensionalities. It has many different stable forms ranging from 0D fullerenes, to 1D nanotubes, to 2D graphene, and finally 3D diamond and graphite. The different forms of carbon are presented in Fig. 2.1.

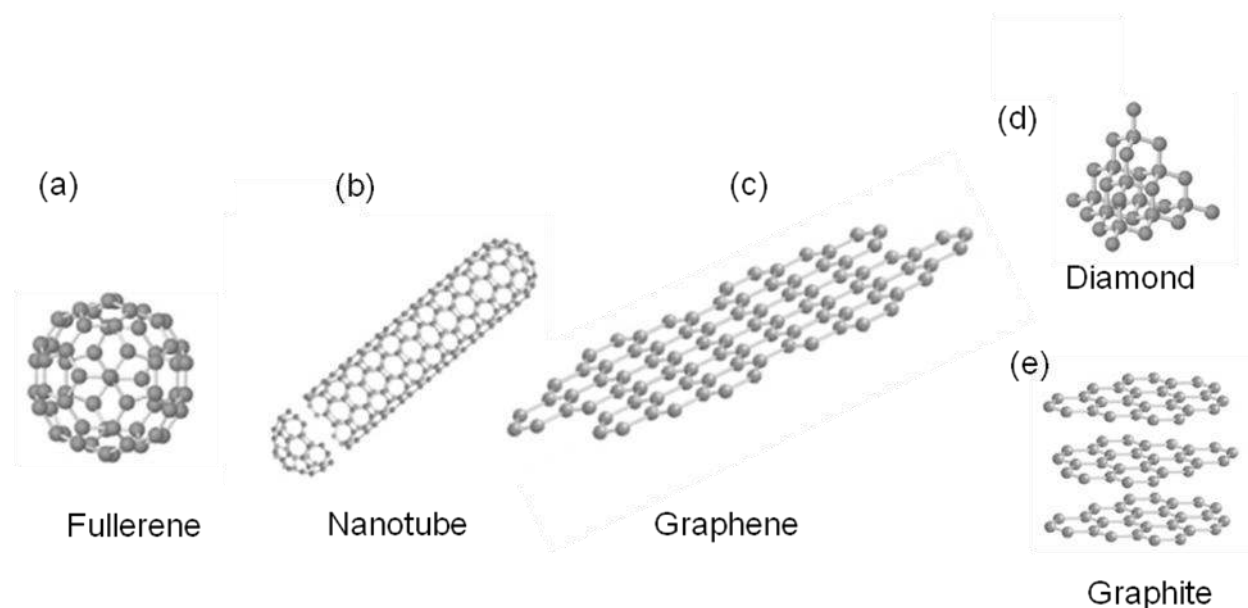


Figure 2.1 A few examples of the stable forms of carbon with the different dimensionalities and various forms. They range from (a) 0D fullerene to (b) 1D nanotube to (c) 2D graphene to 3D (d) diamond and (e) graphite. Images are taken from ref [1].

¹ Part of the work presented in this chapter are extensions of Muhammad R. Islam and Saiful I. Khondaker, Recent progress in parallel fabrication of individual single walled carbon nanotube devices using dielectrophoresis. *Materials Express* 4, 263 (2014) (Cover article).

The history of carbon nanotube (CNT) begins with the discovery of first carbon based nanostructure, fullerene. The first fullerene molecule named, buckyball (C_{60}), shown in Fig. 2.1 (a) was discovered in 1985 [2]. It is a hollow sphere made of carbon atoms in the form of soccer ball. The discovery of fullerenes greatly influenced the carbon nanostructure based research.

CNTs was discovered in 1991 by Iijima during synthesis of fullerenes by electric arc discharge technique [3]. CNTs observed by Iijima were called multi-walled carbon nanotubes (MWNTs). In an MWNT several concentric cylinders made of graphene are placed with an interlayer spacing of 3.4 \AA and a diameter of varying between 10 to 20 nm. Two years later, researchers from NEC [4] and IBM [5] independently synthesized single-walled carbon nanotubes (SWNTs) as shown in Fig. 2.1b. In contrast to MWNT, a SWNT consist of a single sheet of graphene rolled up into a seamless hollow cylinder. Since its discovery, SWNT have created huge interest in different areas of science and technology because of their exceptional electronic, optical and mechanical properties. In short SWNT is a unique material providing a combination of superlative electronic, optical, mechanical and thermal properties. In this their will discuss the fabrication and electron transport measurements of SWNT based SETs.

2.1.1 Structure of carbon nanotubes

The basic configuration of a carbon nanotube can be described as a seamless cylinder made by rolling a graphene sheet with fullerene cap at ends [6]. Graphene is a single atomic layer of SP^2 bonded carbon atoms arranged into a honeycomb lattice [7]. The graphene sheet can be rolled in different way to give different type of SWNT. Depending on the rolling of the graphene sheets, the SWNTs give different geometrical and electrical properties which are known as chirality. Figure 2.3(a) presents an arbitrary way to construct a SWNT from a graphene sheets. A nanotube

is uniquely described by the vector (chiral vector) $\vec{c} = n\vec{a}_1 + m\vec{a}_2$ where, \vec{a}_1 and \vec{a}_2 are primitive translation lattice vectors and n and m are integers. The circumference of tube can be expressed by the vector \vec{c} and radius r , of the tube [8]:

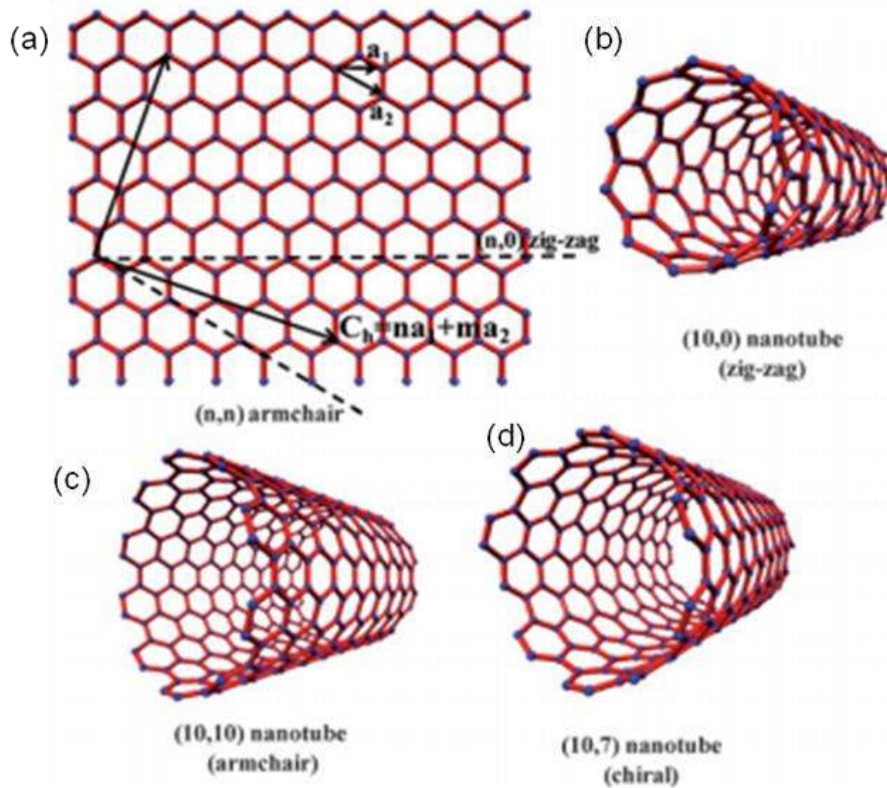


Figure 2.2 (a) A graphene sheet that can be folded into a seamless cylinder by cutting out the sheet along the dashed lines and rolling it up along vector \vec{C}_h . a_1 and a_2 are the unit vectors of the hexagonal graphene sheet (b) Example of a “zig-zag” nanotube. (c) Example of a “armchair” nanotube. (d) Example of a “armchair” nanotube. Adpated from ref [9].

$$r = \frac{|\vec{c}|}{2\pi} = \frac{a}{2\pi} \sqrt{n^2 + m^2 + nm} \quad (2.1)$$

Here a is the lattice constant defined by, $a = \sqrt{3}a_{cc}$, a_{cc} is the C-C bond length. Also the chiral angle φ , which is the tilt angle between the hexagon and the nanotube axis can be described using the chiral vector:

$$\varphi = \arccos\left(\frac{\sqrt{3}(n+m)}{2\sqrt{n^2+m^2+nm}}\right) \quad (2.2)$$

Because of the hexagonal symmetry of graphene structure φ lies in the range between 0 to 30°.

Nanotubes are generally labeled using the (m,n) indices. For example, $(n, 0)$ nanotubes have carbon-carbon bond along the axial direction of nanotube giving a chiral angle $\varphi = 0^\circ$. These nanotubes are called zigzag nanotube (Fig 2.2(b)). For nanotubes labeled (n,n) , the chiral angle is $\varphi = 30^\circ$ with the carbon-carbon bond normal to the length of the nanotube, and is called armchair nanotube shown in Fig 2.2 (c) [8]. All the remaining configurations $(n, m \neq n \neq 0)$ are called chiral nanotube shown in figure 2.2(d).

2.1.2 Electronic properties of carbon nanotubes

Since rolling of graphene gives single wall carbon nanotube, we can obtain the band structure of nanotube from the band structure graphene. By applying proper boundary conditions on the momentum wave vectors of graphene structure it is possible to derive the band structure of SWNT. For an infinite long nanotube the wavevector along the tube axis, \vec{k}_\parallel is continuous and the wavevector perpendicular to \vec{k}_\parallel , \vec{k}_\perp follow the periodic boundary condition $\vec{k}_\perp \cdot \vec{c} = 2\pi q$, where $q = 0, 1, 2, \dots, n$. This boundary condition leads to a quantized value allowed for the \vec{k}_\perp , which satisfy the relation, $d\vec{k}_\perp = 2/d$ where d is diameter of SWNT. We can obtain the 1D subband of nanotube by cutting of the graphene band structure along the cross-sectional

direction with the allowed \vec{k}_\perp values (fig 2.3(a)). Under certain conditions the allowed \vec{k}_\perp states pass through the centre of the dispersion cone.

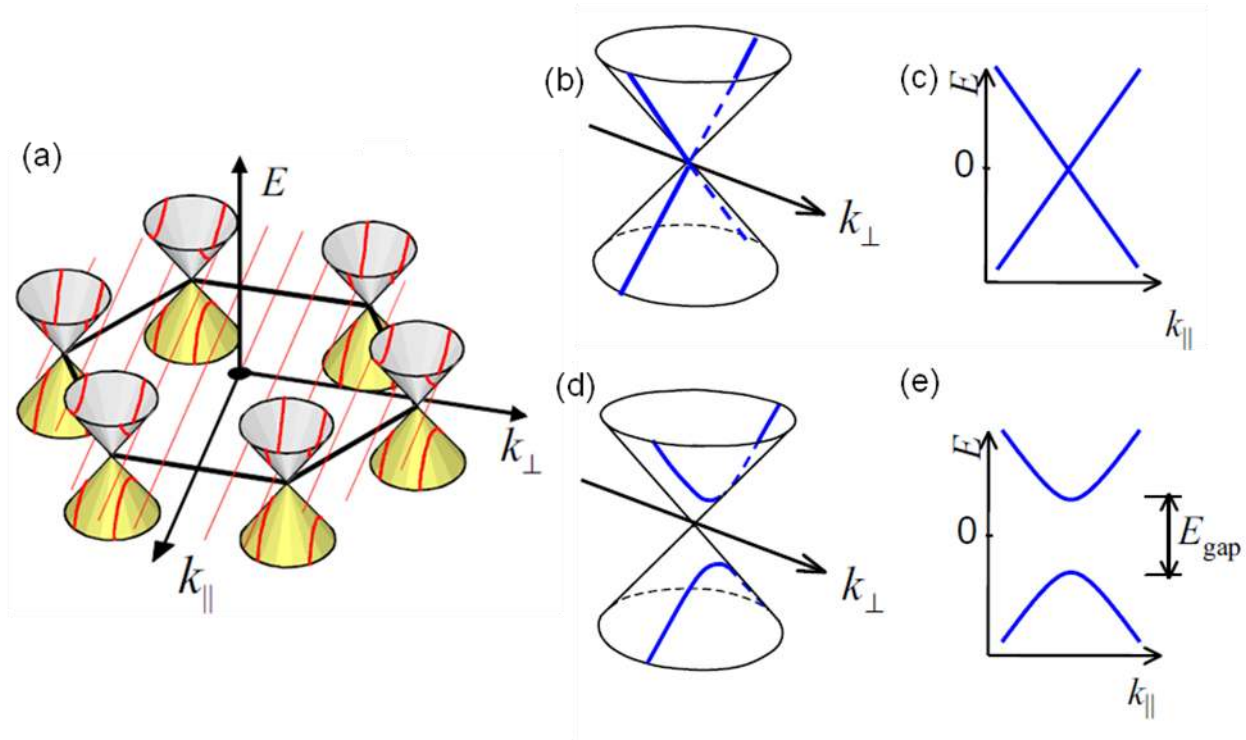


Figure 2.3 (a) Band structure of graphene. It shows that the one dimensional subbands of nanotubes can be determined by applying boundary conditions. Low energy band structure of carbon nanotube: (b) For $p = 0$, there is an allowed value of \vec{k}_\perp whose subband passes through the middle of the dispersion cone which results in a metallic nanotube. (c) Energy dispersion for a metallic nanotube. (d) For $p \neq 0$, there is an allowed value of \vec{k}_\perp whose subband misses the middle of the dispersion cone which results in a semiconducting nanotube. (e) Energy dispersion for a semiconducting nanotube. Figure adopted from ref [10].

In this case the energy dispersions show bands crossing the Fermi level without any band gap and hence the nanotube (Fig 2.3 (b)) shows metallic behavior. If the \vec{k}_\perp states miss the middle of dispersion cone (Fig 2.3 (d)) then there are two parabolic bands resulting in a bandgap near Fermi level giving a semiconducting nanotube [11-13]. Thus depending on the quantization of \vec{k}_\perp either semiconducting or metallic transport can be obtained.

In fact the wrapping indices (m, n) of the nanotube determines the electronic properties of SWNT. For any arbitrary (m, n) nanotube, $n-m = 3a+b$, where a is an integer and b is -1, 0, or 1 [14]. If $b=0$ then the allowed \vec{k}_\perp is such that it pass through the middle of the dispersion zone and the nanotube is metallic. The slope of the dispersion cone, for metallic SWNT, depends on the Fermi velocity, $dE/dK = \hbar v_F$, where $v_F \sim 8 \times 10^5$ m/s [15]. If $b= +1$ or -1 then the \vec{k}_\perp states miss the middle of dispersion cone, gives semiconducting nanotube. For a semiconducting nanotube the \vec{k}_\perp vector misses the middle of dispersion cone by, $\Delta \vec{k}_\perp = \pm \frac{2}{3d}$. Therefore the bandgap of the semiconducting nanotube is given by,

$$E_g = 2 \times \left(\frac{dE}{dK} \right) \times \frac{2}{3d} = 2\hbar v_F \left(\frac{2}{3d} \right) \approx 0.7 eV/d(nm) \quad (2.3)$$

Therefore the bandgap of the semiconducting nanotube ($d = 0.8-3$ nm) varies between 0.2 eV to 0.9 eV and is proportional to the reciprocal of the diameter. For a more detailed description of the structural and electronic properties of carbon nanotube including the band structure calculation reader can explore the review article [16-19].

2.2 Single electron transistor

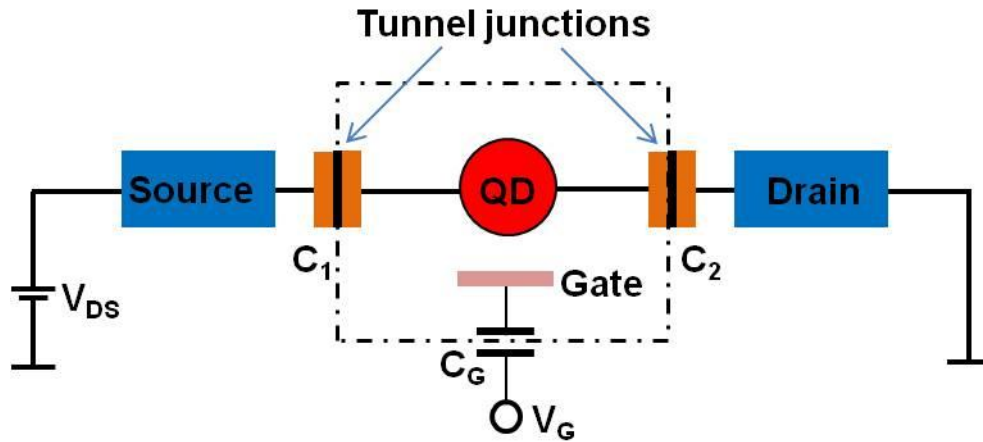


Figure 2.4 Schematic of a single electron transistor with the electrical connection. A conducting island often called quantum dot (QD) coupled to the source and drain leads via tunnel barriers and capacitively connected to a gate.

Figure 2.4 describes the schematic diagram of a single electron transistor (SET) with all its important components and parameters. An SET consists of a small conducting island often called quantum dot (QD) which is resistively attached to the source and drain reservoirs, through which charge particle transfer takes place. QD is capacitively coupled to nearby gate electrodes. The gate voltage tune the entire ladder of electrochemical potential of the QD up and down with respect to the bias voltage [20-22]. There exist tunnel coupling between the QD and the reservoir that allows electrons to flow between the QD and electrodes via single electron tunneling. If N is the number of electrons in the QD then the charges on the island are quantized and equal to Ne . If an electron tunnel through the QD the number of electrons, N in the QD is adjusted to minimize the energy in the circuit.

During tunneling the charges of QD is change by ne ($n = 1, 2, \dots$). This changes the electrostatic potential energy of the QD by, $Ec = e^2/C_{\Sigma}$, where capacitance $C_{\Sigma} = C_1 + C_2 + C_3$,

is the total capacitance of the SET. In order to observe single electron tunneling this charging energy E_C needs to be greater than the thermal energy ($K_B T$). Also the tunnel barrier needs to be sufficiently opaque so that the electrons are located either in the source, drain or on the QD [20, 21, 23]. This means that the quantum fluctuation in the number N of electron tunnel through the island must be much smaller than the inverse of time. This criterion sets a lower limit for the tunnel resistance R_t , which can be found from the uncertainty principle. The charging or discharging time for the QD is $\Delta t = R_t C$. Applying uncertainty principle we get, $\Delta E \Delta t = (e^2 / C) R_t C > h$. This implies R_t should be much larger than the quantum resistance $h/e^2 = 25.81 \text{ K}\Omega$ in order to minimize the energy uncertainty. Therefore the two conditions for observing single electron tunneling are:

$$R_t \gg h/e^2 = 25.81 \text{ K}\Omega \quad (2.4)$$

$$E_c = e^2 / C_\Sigma \gg k_B T \quad (2.5)$$

By weakly coupling the island to the source and drain leads, the first condition can be met. The second condition can be met by making the QD very small since the capacitance of any object scales with its dimension. Typically the size of QD ranges between few nanometer to few micron which yields capacitance of the order of aF. Therefore in order to satisfy the second condition and observe the single electron tunneling, measurements need to be performed at cryogenic temperatures.

2.2.1 Electron transport through single electron transistor

The electronic transport through a single electron transistor can be usually described by the constant interaction (CI) model [24, 25]. This model is based on two assumptions: (1) the

E_{add} is called addition energy. Coulomb interaction among the electrons inside the dot and between the electrons in the dot and somewhere else in the circuit are parameterize by a capacitance C . Here $C = C_S + C_D + C_G$, is the total capacitance where C_S , C_D , and C_G are the capacitance of the source, drain and gate respectively. (2) The quantum energy levels and C are independent of the number of electrons on the QD. The total energy of a N -electron dot using CI model is given by

$$U_n = \frac{[-|e|(N - N_0) + C_S V_s + C_D V_D + C_G V_G]^2}{2C} + \sum_{n=1}^N E_n(B) \quad (2.6)$$

Where, $|e|$ is the charge of electron and N_0 is the number of electrons in the QD at $V_G=0$, and V_s , V_D , and V_G are the voltage applied to the source, drain, and gate, respectively. The term $C_S V_s$, $C_D V_D$, and $C_G V_G$ represent the induced charge and electrostatic potential on the dot. And the last term of Eq. 2.6 is the sum over the occupied single-particle energy levels $E_n(B)$, and it depend on the characteristics of the confinement potential.

The transport of QD can be more conveniently described using the idea of electrochemical potential, μ which is the minimum energy needed to populate the QD with an additional carrier:

$$\mu(N) = U(N) - U(N-1) = (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|} (C_S V_s + C_D V_D + C_G V_G) + E_N \quad (2.7)$$

Where, $E_C = e^2/C$ is the charging energy. Here, $\mu(N)$ is the potential when the number of electron in the minimum energy state changes from $N-1$ to N . Spacing between two consecutive energy states are given by:

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E \quad (2.8)$$

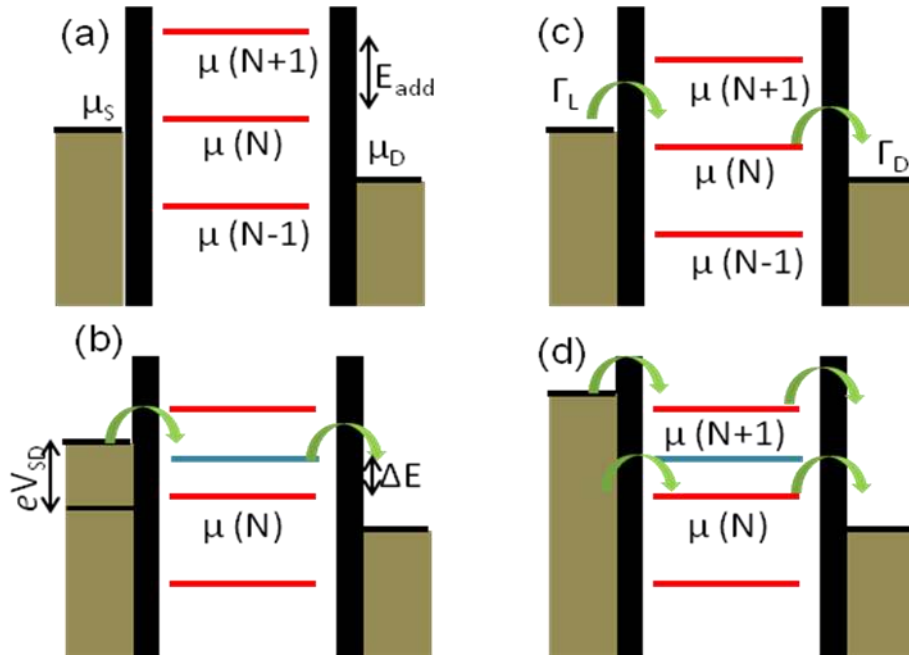


Figure 2.5 Cartoon for the electrochemical potential of the SET at different voltage configuration. (a) The electrochemical potential of QD does not falls inside the bias window - which cuses current blockade. (b) The electrochemical potential of the QD is drag inside bias window by sweeping gate voltage and electron tunneling occurs. (c) Application of bias voltage rises the electrochemical potential of the drain and electron tunneling occur once the electrochemical potential of the QD fall inside dias window. (d) Excited energy levels are obtained for application of large bias voltage.

The addition energy is defined as $E_{add} = E_C + \Delta E$. Where ΔE is separation between two quantized energy levels and is zero if the energy levels are degenerate. Single electron tunneling through a QD depends on the relative position of electrochemical potentials of dot, source, and drain. When voltage is applied at source then a “bias window” is open up. The energy in the bias window is between μ_S and μ_D ($\mu_S \geq \mu \geq \mu_D$), and $\mu_S - \mu_D = -|e|V_{SD}$. When the electrochemical potential of QD lies in the bias window, electrons can tunnel from the source to the drain. If this condition does not met then no electron can flow through the island and is known as Coulomb blockade (fig 2.5 (a)).

Single electron tunneling can also be observed by sweeping the gate voltage. This shifts the energy levels of QD up or down. When the electrochemical potential of QD fall inside the bias window single electron tunneling occur and the number of electrons by one as shown in Fig. 2.5 (b). By measuring the current while sweeping the gate voltage, we obtain a trace as presented in Fig 2.6 (b), which is known as Coulomb oscillation. Coulomb oscillation gives aluable information about SET. The distance between the peaks gives $E_C + \Delta E$. The space between two peaks represents Coulomb blockade and electron transfer does not occur here. Thus by tuning the gate voltage, it is possible to control the electron tunneling through the QD.

Coulomb blockade can also be lifted by applying bias V_{SD} (see Fig. 2.5 (c)). Bias voltage changes the electrochemical potential the source and drain. When the electrochemical potential of the QD is between the bias windows an electron tunneling occurs. By increasing V_{SD} further it is possible to observe excited state of QD (Fig. 2.5 (d)).

A plot of the conductance versus source- drains voltage, and gate voltage is shown in fig 2.6 (c). This is known as “stability plot”. The blue outlined diamond structures are known as Coulomb diamonds. Inside the coulomb diamond no current flows due to Coulomb blockade. Outside the diamonds, single-electron tunneling take place and Coulomb blockade is lifted. The stability plot contains all the information of the SET and the SET parameters can be extracted from this plot. For example the gate capacitance can be obtained using the relation $C_G = e / \Delta V_G$ where, ΔV_G is separation between two diamond. The source and drain capacitances can be derived from the slopes of the Coulomb diamonds using the relation, $\alpha_S = -C_G / C_S$ and $\alpha_D = C_G / (C_G + C_D)$. The charging energy defined as $U_C = e^2 / C_\Sigma$ can be obtained once we know all different capacitances. Also the height of Coulomb diamond gives the charging energy of the QD.

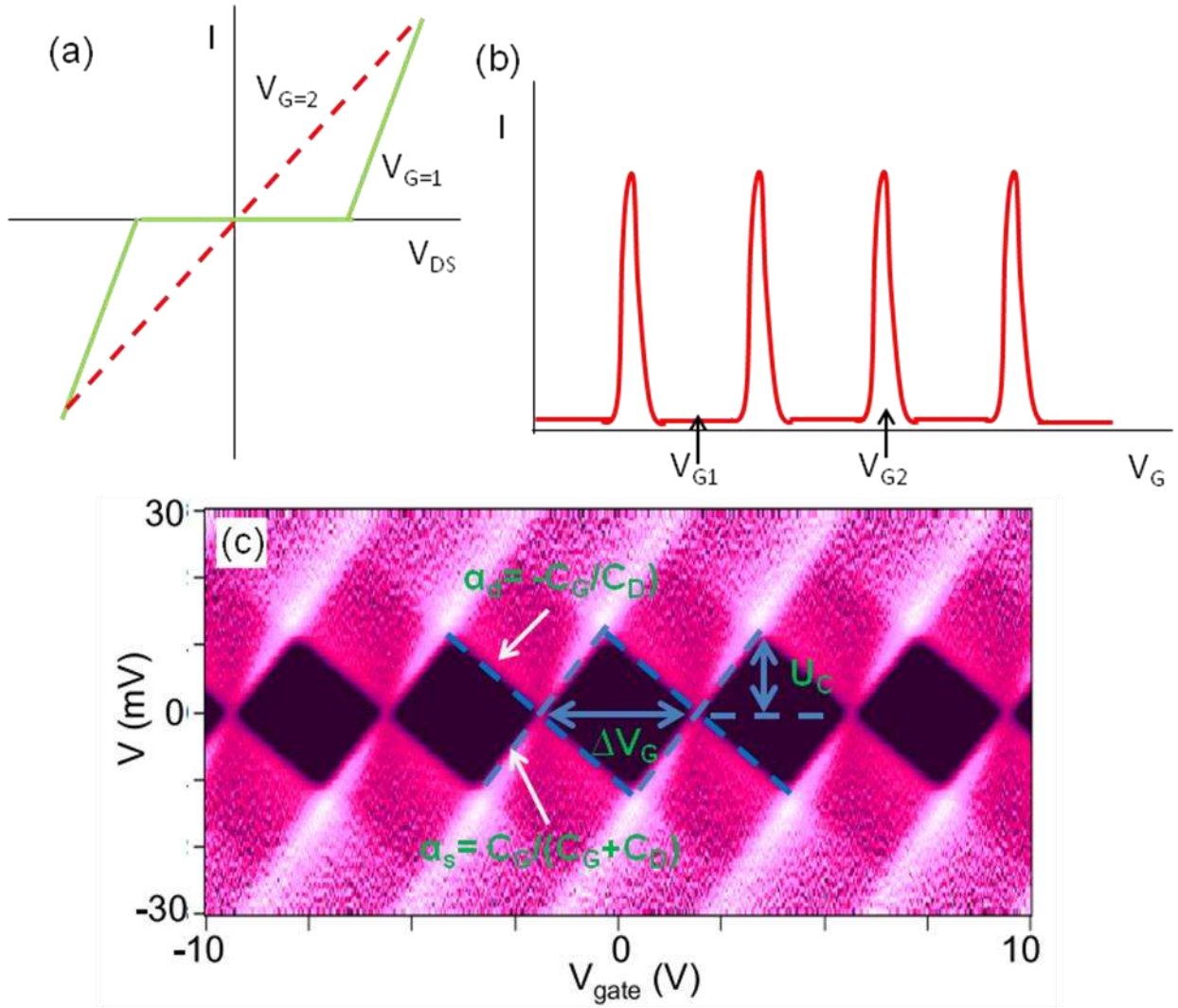


Figure 2.6 Typical low temperature electron transport behavior of SET (a) at gate voltage, V_{G1} , current is suppressed and is called Coulomb blockade (CB). Electron tunneling occur when a gate voltage to V_{G2} is applied. (b) Tuning the gate voltage gives current oscillation known as Coulomb Oscillation (CO) (c) Stability plot, where conductance vs source-drain voltage vs gate voltage is plotted.

2.2.2 Fabrication of different type of single electron transistors

Single electron tunneling was first observed about sixty years ago in extremely thin film consist of discontinuous grain. High resistance observed in these films at low temperature was

explained by Gorter et al. in 1951 [26]. The field and temperature dependent resistance was considered to be an effect of the separation of positive and negative charge. Similar effect was observed in discontinuous gold film by Neugebauer et. al. in 1962 [27]. They derived a conductivity based on the creation of charge and field dependent tunneling between islands. Charge transport through a layer of tin particles in embedded oxide was investigated by Giaever et. al. several years later [28]. They explain the high resistance behavior at low bias using a capacitor-charging model.

Several decades later, innovations in nanolithography and thin film processing enabled better-controlled fabrication of artificial structures small enough to demonstrate single electron effects at cryogenic temperatures. The first experimental demonstration of an SET was done by Fulton and Dolan in 1987 [29]. In their work tunnel junctions were formed in overlapping layer of aluminum thin film by controlling the shadow evaporation angle.

Coulomb oscillations in semiconductors were first observed in 1989 [30]. Current oscillations was observed in narrow 1D channel on dual gated Si MOSFET. The upper gate forms an inversion channel in the Si and a narrow gap is created by the other gate create a horizontal confinement, for the electron gas to move in only one direction. Electrostatic potential originating from the random charges at the Si/SiO₂ interface create tunnel barrier. In 1990 SET was fabricated in a GaAs/AlGaAs 2-DEG by Meirav et. al.[31]. They patterned a constriction in a channel which creates the potential barriers for electrons moving down the channel using a gate potential. The potential barriers in this case were defined lithographically.

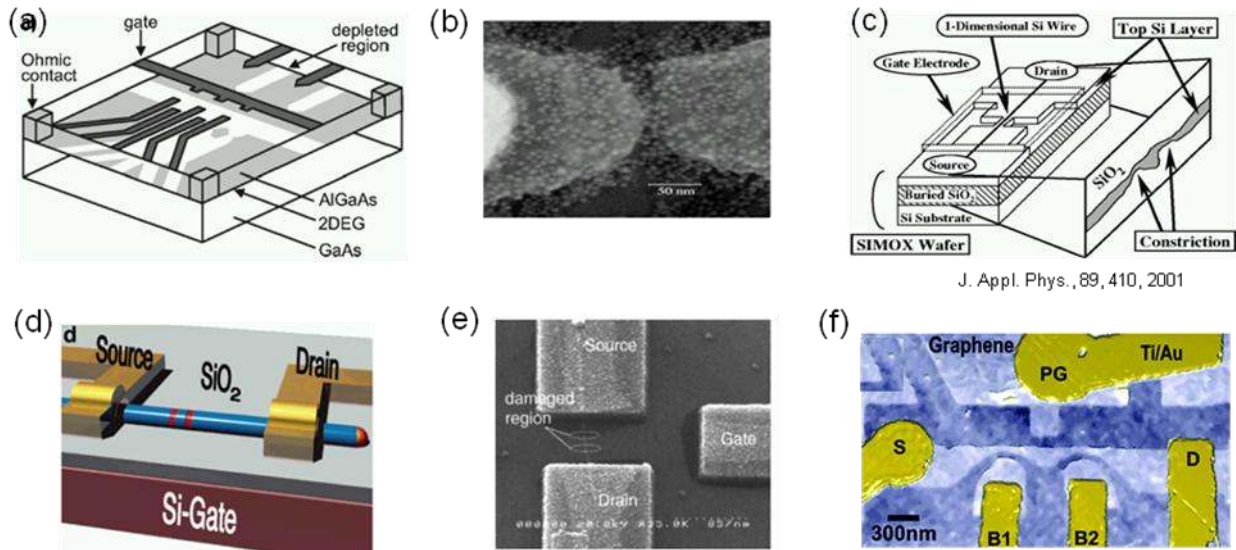


Figure 2.7 Popular SET fabrication techniques: (a) surface patterning of 2DEG heterostructure [31] (b) self assembly of CdSe colloidal nanocrystal [32] (c) Etching Si substrate [34] (d) patterning of InAs nanowire with InP barriers.[42] (e) Nanotube SET defined by metal contacts[48] (f) Graphene SET [64].

Several other techniques including metallic grains or particle in nanopore [32, 33], direct etching of Si substrate [34], colloidal nanocrystals [35-38], focused ion beam [39-41] had been used for the fabrication of SET. Lithography defined dots in 2DEG or Si MOSFETs typically require ultra-low (sub-Kelvin) temperatures for operation. Higher operating temperature (~100 K) and reproducible SET behavior can be obtained by metallic grains and colloidal nanocrystals. However it is very difficult to place nanoparticles or metallic grains inside the nanopore.

Recently, nanowires [42-45] and carbon nanotubes including both MWNT [46, 47] and SWNT [48-63] are considered as promising candidates for the QD of SETs because of their ultra-small diameters (~ 1nm) along with the unique one dimensional nature. Besides 2D graphene are also used as active materials for fabrication of SET very recently [64-67].

Fabrication of SWNT based SET relies on the creation of tunnel barriers along the axial direction of the tube, which will be discussed in more detail in the next section.

2.2.3 Carbon nanotube quantum dots

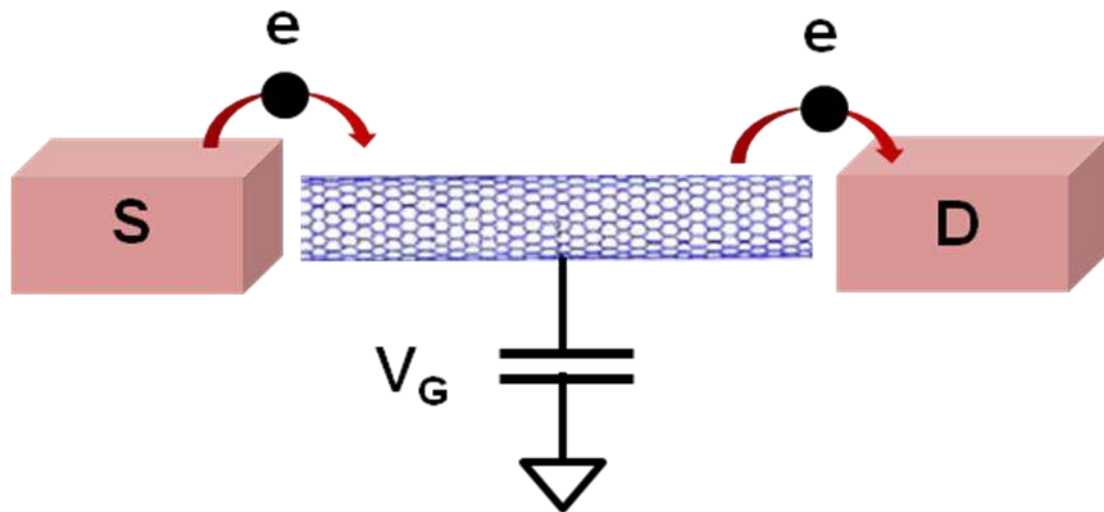


Figure 2.8 Schematic diagram of a carbon nanotube quantum dot which can be formed by depositing metal electrodes, source (S) and drain (D), on top of the tube separated by a distance L . The nanotube is capacitively coupled to the gate, (usually the back gate plane of the silicon substrate). The QD is formed in the segment of nanotube in between the electrodes.

We described the basic electronic properties of SWNT in section 2.1. Due to the momentum quantization along traverse direction nanotubes are considered as one dimensional object. At low temperatures for the nanotubes with short lengths, discrete energy levels originating from the zero-dimensional nature of the nanotubes electronic states manifest itself and nanotubes behave as quantum dots [68].

In SWNT tunnel barriers can be created by depositing metal electrodes. The size of the QD is defined by the separation between two such barriers (metal contact), L , (Fig. 2.8). This

results in quantized energy levels in the longitudinal direction, with an energy level separation Δ . The strength of the tunnel barriers determines the degree of confinement of electrons in the nanotube QD.

For very strong (opaque) barriers, the tunnel rate between the QD and the reservoirs (Γ) is very small which results in a large lifetime of the electrons in the QD. If the barriers become more transparent, the energy levels get ' Γ -broadened'. Depending on the ratio between the lifetime broadening and the charging energy E_C , there are three different types of QD regimes (with different typical phenomena associated with them):

1. Closed QD regime: ($\hbar\Gamma \ll E_C$): Charging effects dominate transport (Coulomb blockade). Single electron transistors operates in the Coulomb blockade regime.
2. Intermediate transparency regime: ($\hbar\Gamma \leq E_C$): Charging effects are important in this regime (co-tunneling and Kondo effect).
3. Open QD regime: ($\hbar\Gamma \gg E_C$): Quantum interference of non-interacting electrons dominates in this regime (Fabry-Perot like interference).

Metal-SWNT coupling depends on the metal contact, diameter and type of the nanotube (metallic/semiconducting). In general metals such as Au or Pd [69-71] make good contact to nanotubes. Whereas Al or Cr make bad contact to nanotubes. It has also been demonstrated that the nanotubes with larger diameter give very small contact resistance [69, 72]. Also the metallic nanotube gives better contact (lower contact resistance) compare to the semiconducting ones. Usually Schottky barriers are created at the nanotube-metal interface for semiconducting SWNT.

Charging energy E_C of the SWNT quantum dots are generally high, and is inversely proportional to the capacitance, C of the device. For a nanotube QD, of length L the capacitance can be expressed by considering the formula of a coaxial cable,

$$C = \frac{2\pi\epsilon_0\epsilon_r}{\ln(2h/r)} L \quad (2.9)$$

where $\epsilon_r = 3.9$ is the average dielectric constant of Si [73], h is the thickness of gate oxide and r is the radius of the nanotube.

We can approximate the charging energy of a nanotube between two leads by a simple model,

$$E_C = \frac{e^2}{C} \approx \frac{e^2}{\epsilon_0\epsilon_r L} \approx \frac{5meV}{L(nm)} \quad (2.10)$$

Using the particle in a box model we can also approximate the single particle energy levels by,

$$\Delta E = \frac{h v_F}{2L} \approx \frac{1meV}{L(\mu m)} \quad (2.11)$$

Where L is the length of the QD, h is planks constant and v_F is the Fermi velocity[73].

2.2.4 Fabrication of carbon nanotube quantum dots

In order to fabricate carbon nanotube single electron transistor using we have to create quantum dot in the nanotube. In a nanotube quantum dot can be created by creating tunnel barrier along the nanotube. Tunnel barrier are usually created by crating defects in the nanotube. Carbon nanotube single electron transistors have been demonstrated by several techniques by creating tunnel barrier.

The first attempt to fabricate nanotube based single electron transistor was performed using multiwall carbon nanotube. In 1999, L Roscheir et. al. had employed scanning probe

manipulation for the fabrication of single electron transistor using semiconducting multiwall nanotube [46]. AFM tip was used to drag MWNT on metal electrode and the portion of MWNT between the electrodes act as QD. For those devices SET behavior was observed at 15 mK and it shows a charging energy of 15 meV. SET was also fabricated by placing MWNT on top of another MWNT [47].

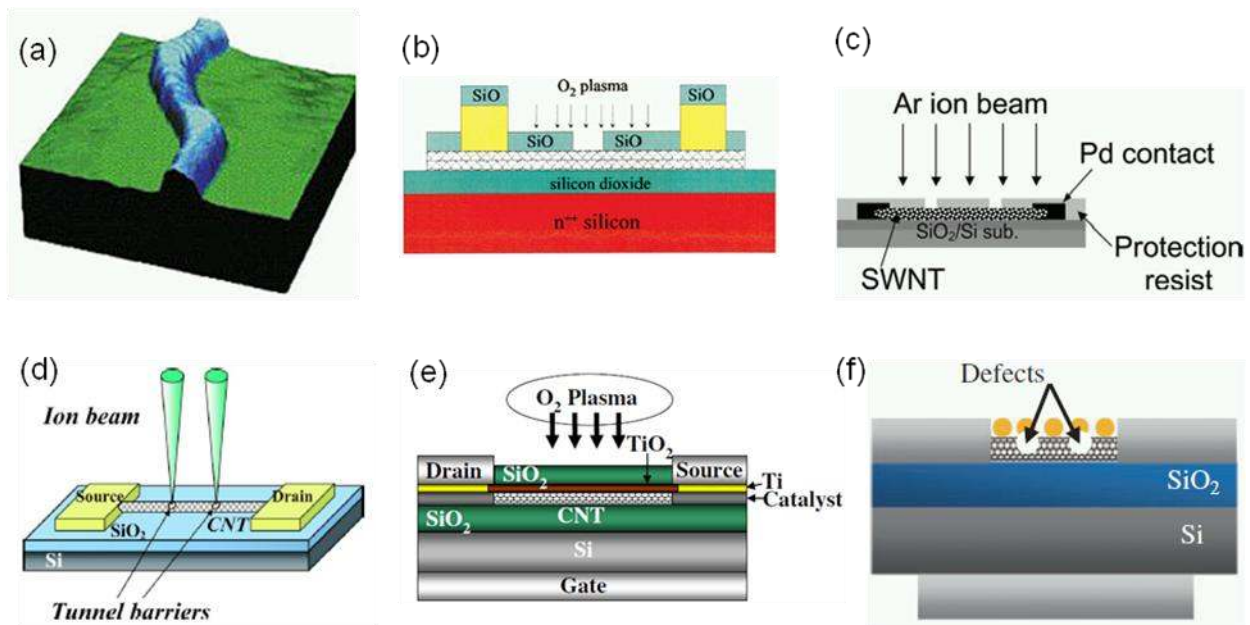


Figure 2.9 Carbon nanotube single electron transistors fabrication techniques. (a) Bending carbon nanotube by AFM tip [48] (b) Modification of nanotube by oxygen (O₂) plasma [49] (c) Bombardment of nanotube by Ar ion beam [57] (d) Fabrication of tunnel barrier by focused ion beam (FIB) defects by Ar ion [75] (e) Creation of defects by O₂ plasma [56] (f) Introducing defects by ion La particles [58].

In 2001 AFM manipulation technique was used to create SWNT based SET [48]. AFM tip was used to bend the SWNT at selected position as shown in figure 2.9 (a). The bend act as tunnel barrier and two such barriers define a QD and the device show SET characteristics at room temperature. A QD of size 25nm was created by this technique which gives a charging energy of 120 meV which is higher than room temperature thermal energy (~26 meV). It is

possible to fabricate single QD using this technique, however creating bend in SWNT using AFM tip is difficult and controlling the size of QD is also challenging.

QD was also defined by modifying the SWNT locally via chemical treatment [49]. In this technique QD is defined by placing a nanowire on top of a SWNT. The entire substrate is then coated with polymer and a gap is created on top of the SWNT by removing the nanowire as shown in figure 2.9 (b). The open window is plasma etched to create QD. The device shows room temperature SET operation.

Tunnel barrier in SWNT can also be created by making defects via ion irradiation [55, 56, 58, 59, 74]. SWNT are bombarded by low energy particle or gas ion (La, Ar, N₂) as shown in figure 2.9 (c)-2.9 (f). Generally MQD are created in this techniques and the size of the device cannot be controlled. Focused ion beam (FIB) was also used for the creation of tunnel barrier in nanotube [75]. The devices show SET behavior with high charging energy. Mostly multiple QD are created in this technique and due to the high energy processing nanotube got damaged.

2.3 Assembly of SWNTs

Assembly of SWNT is one of the most important parts to fabricate nanotube based devices. Fabrication of SET using SWNT has two major steps: 1) assembly of individual SWNT to the circuit, and 2) creation of tunnel barrier to the SWNT. In particular large scale assembly of individual SWNT is required for the assembly of individual SWNT. Here in this section we will discuss techniques for the assembly of SWNT.

2.3.1 Find 'em and wire 'em technique

Find 'em and wire 'em technique is technique is oldest and widely used methods for the integration of SWNT. Many novel physics associated with individual SWNT has been observed with devices fabricated using this approach [76-79]. In this technique SWNT are randomly dispersed on silicon substrate containing marker. The SWNT on which the device needs to be fabricate is located by scanning electron microscopy (SEM) or atomic force microscopy (AFM). Once the position of the SWNT is located electrode pattern are defined by electron beam or optical lithography. Different electronic and optical devices were made using this approach. Figure 2.10 (a) shows the images of SWNT device fabricated by placing individual SWNT the metal electrodes [80]. The advantage of the find 'em and wire 'em technique is that it can customized the devices.

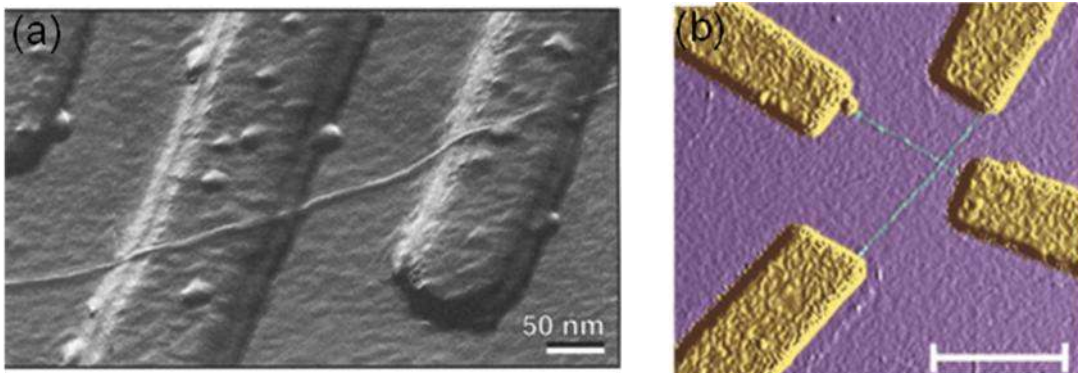


Figure 2.10 (a) Field effect transistor fabricated where SWNT was randomly placed between metal electrodes by the 'find' em and 'wire' technique[80]. (b) Complex SWNT structure (crossing of two SWNT) assembled by 'find' em and 'wire' technique[79]

Figure 2.10 (b) shows an AFM image of device with customized design where, crossed SWNTs are contacted between two metal (Au) contacts using the "find 'em and wire 'em" technique in order to study interaction between two SWNT [79]. The disadvantages of the find 'em and wire

'em technique is that only a limited number of devices can be made using this techniques. Besides, this technique is not scalable, and it is time consuming. Therefore in order to obtain industrial applications for SWNT based devices scalable assembly techniques need to be developed.

2.3.2 Chemical vapor deposition (CVD) growth of SWNTs

Chemical vapor deposition (CVD) is one of the most popular and widely used method to obtain assembled SWNTs [81-83]. In CVD photolithography or electron beam lithography are used to pattern small catalyst island at the desired position on the substrate (fig 2.11(a)). After defining the catalysts particle appropriate carbon containing feedstock gases are introduced into a furnace at high temperature ($700\text{ }^{\circ}\text{C} < T < 900\text{ }^{\circ}\text{C}$). Then SWNT are growing from the catalytic particle. The catalytic particles are typically composed of a transition metal or alloy of transition metal (e.g. iron or iron/molybdenum). The catalyst can be obtained by immersing the silicon chip into a solution of catalyst particle. The feedstock gas typically consists of methane. By controlling the density of catalyst particle it is possible to grow individual SWNT (fig 5.11)[84].

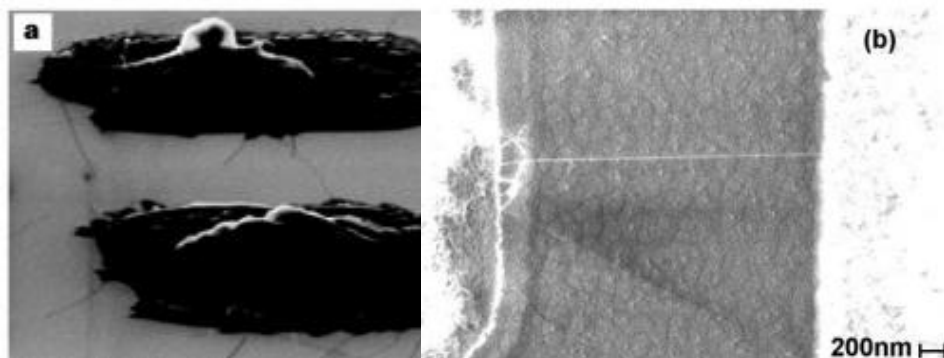


Figure 2.11 a) CVD growth of individual SWNT from Patterned catalytic[81] (b) Zoom in image of CVD grown single SWNT [84]

Besides, the band gap and diameter of the SWNT can be controlled by controlling the gas flow rate and temperature. Using different growth condition it is possible to grow ultra-long nanotube or ultra-dense nanotube. Figure 2.11 (b) shows a long individual SWNT grown via CVD.

The most significant advantage of CVD is that it allows SWNT to grow in different forms. For example CVD can grow both individual or thick films of nanotube. The as grown nanotube can be straight, aligned, or entangled. SWNT growth by CVD techniques are defects free and the device fabricated from CVD grown SWNT gives superior device performance [71, 85-88]. Even though large scale assembly of SWNT is possible using CVD, the high growth temperature (900 °C) required for this technique make it incompatible with current complementary metal-oxide-silicon (CMOS) fabrication technology [89].

2.3.3 Post growth techniques

2.3.3.1 Dielectrophoresis

Dielectrophoresis (DEP) is the phenomena wherein a polarized particle experiences a force and gains translational motion when it is placed in a non-uniform electric field [22-24]. This force was first recognized and described by Pohl in 1951 [25]. When an alternating (AC) electric field is applied to a suspension of polarizable elements, surface charge of different polarity are induced on either side of the particle resulting in the formation of a dipole moment and causes the particle to experience a net force. As a result, the particle undergoes a translational motion and aligns along the direction of electric field lines. When the field is uniform, no net charge is induced on the particle and it does not experience any force

2.3.3.2 Theory of Dielectrophoresis

When a polarized object is subject to an electric field, surface charges are induced at the particle resulting in the formation of induced dipole moment. For uniform electric field, the equal and opposite charges are induced on the SWNTs. So the net Coulomb force experienced by the particle is zero and the particle does not undergo translational motion.

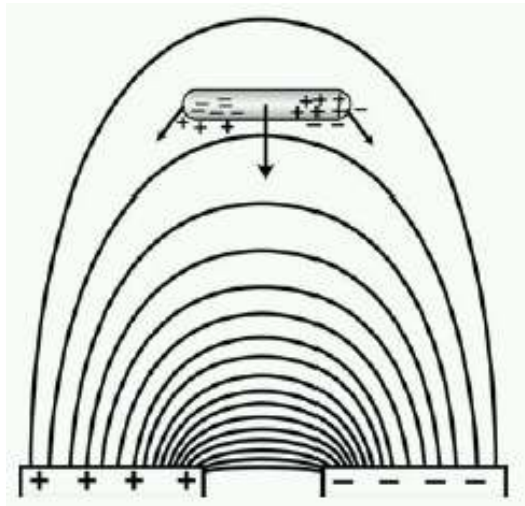


Figure 2.12 Schematic for the nanotube assembly via DEP. In a non-uniform electric field opposite charges are induced at the opposite end of the SWNT and a dipole moment is created and the resulting DEP force causes the SWNT to move towards the electrode[90]

When the electric field is not uniform then the Coulomb force on different side of the object are different and a net force is exerted on the object which causes the particle to move. In addition, the resulting torque aligns the object towards the field lines. The phenomena is observed for both alternating current (AC) and direct current (DC) electric field. When an AC electric field is applied to nanotubes induced dipole moment are created and the it experience a DEP force which align the tube between the electrodes. The principle of DEP for a SWNT is shown schematically in fig 2.12. Because of their anisotropic shape nanotube induce the strongest dipole moment along the axis of the tube.

If p is the dipole moment induced by a polarized particle when placed in an AC electric field E , then the DEP force experienced by a polarized particle can be expressed by

$$F = (p \bullet \nabla E) \quad (2.12)$$

The AC electric field E can be expressed as

$$E = E_x \hat{i} + E_y \hat{j} + E_z \hat{k}$$

Where E_x , E_y , and E_z are x , y , and z components of electric field. The x -component can be described in terms of frequency ω and phase φ of the AC current by:

$$E_x = E_{x0}(x, y, z) \cos[\omega t + \varphi_x(x, y, z)]$$

Similar expression can be obtained for the other orthogonal components of the electric field.

Similarly dipole moment has components, p_x , p_y , and p_z along the orthogonal directions and can be expressed as

$$p = p_x \hat{i} + p_y \hat{j} + p_z \hat{k}$$

Where the x component:

$$p_x = 2\Gamma \bullet \varepsilon_m [\text{Re}(K_{CM}) \cos(\omega t + \varphi_x) - \text{Im}(K_{CM}) \sin(\omega t + \varphi_x)] E_{x0}$$

Where Γ is a prefactor depends on the geometry of the object, ε_m is the dielectric constant of the suspending medium and K_{CM} is the Clausius-Mossotti (CM) factor. Similar expression can be obtained for the other components p .

The DEP force similarly can be described as

$$F = F_x \hat{i} + F_y \hat{j} + F_z \hat{k}$$

The x -component F_x can be expressed as

$$F_x = m_x \frac{\partial E_x}{\partial x} + m_y \frac{\partial E_y}{\partial y} + m_z \frac{\partial E_z}{\partial z}$$

By averaging F_x over time we got

$$\bar{F}_x = \Gamma \bullet \varepsilon_m \left[\frac{1}{2} \text{Re}(K_{CM}) \nabla (E_{x0}^2 + E_{y0}^2 + E_{z0}^2) + \text{Im}(K_{CM}) (E_{x0}^2 \nabla \varphi_x + E_{y0}^2 \nabla \varphi_y + E_{z0}^2 \nabla \varphi_z) \right]$$

From the above equation we can write the real part of the DEP force as

$$\bar{F}_{C,DEP} = \frac{1}{2} \Gamma \bullet \varepsilon_m \frac{1}{2} \text{Re}(K_{CM}) \nabla E^2 \quad (2.13)$$

And the imaginary part can be simplified as

$$\bar{F}_{T,DEP} = -\frac{2\pi}{\lambda} \Gamma \bullet \varepsilon_m \text{Im}(K_{CM}) E^2 \quad (2.14)$$

The DEP force depends on the K_{CM} which depends on the dielectric properties of the particle and the suspending medium and the geometry of the particle. For a cylindrical shape particle the

K_{CM} is

$$K_{CM} = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*} \quad (2.15)$$

Where ε_p^* and ε_m^* are the complex permittivities of the particle and the suspending media respectively. This can be is defined as

$$\varepsilon^* = \varepsilon - i \frac{\sigma}{\omega}$$

Where, σ is conductivity and $i^2 = -1$. Again the geometric factor depends on the morphology of the object and for a cylindrical object can be expressed using the length, l and radius, r of the cylinder by

$$\Gamma = \frac{\pi r^2 l}{2}$$

Finally we can express the DEP force experienced on a cylindrical tube when it is placed in an AC electric field given by [90]

$$F = \frac{\pi r^2 l}{2} \varepsilon_m^2 \text{Re}(K_{CM}) \nabla E^2 \quad (2.16)$$

From equation 2.16, we found that the DEP force is zero when a uniform field is applied. This equation also indicates that the DEP force varies with the shape and size of the particle, particle with a large volume experiences grater DEP force. DEP force depends on the physical properties of the SWNT as well as the properties of the medium in which the SWNT is suspended. Depending on the permittivity of the SWNT (ε_p^*) and the suspending medium (ε_m^*), DEP force can be either positive or negative. If $\varepsilon_p^* > \varepsilon_m^*$ then K_A is positive, the particles will align along the electric field and is called positive DEP. The opposite case will occur if $\varepsilon_p^* < \varepsilon_m^*$ in the case the particle will experience repulsion and is called negative DEP. Metallic SWNT (m-SWNT) and semiconducting SWNT (s-SWNT) experiences different DEP forces due to their different dielectric constant. Typically, m-SWNT has a dielectric constant much larger than that of the suspending medium which cause them to experience greater DEP force compared to semiconducting SWNT[90]. The effect of DEP parameters on the directed assembly of SWNT will be discussed in great details in sub section.

2.3.3.3 Parameters controlling the assembly of individual SWNT

Assembly of SWNT via DEP depends on several parameters such as the quality of the SWNT solution, the magnitude of the applied AC voltage, frequency of the AC signal, size and shape of the electrodes, deposition time and substrate oxide thickness. Since DEP is a solution processed assembly technique, the assembly of individual SWNT and their yield are greatly influenced by the quality and stability of the SWNT solution. For high yield assembly of SWNTs, the solution needs to be catalytic particles free, stable, and the nanotubes need to be uniformly dispersed.

Being catalytic particle free is important, as they placed themselves in the channel during DEP assembly. The catalytic particles are highly conductive and their presence in the device can disrupt the device performance.

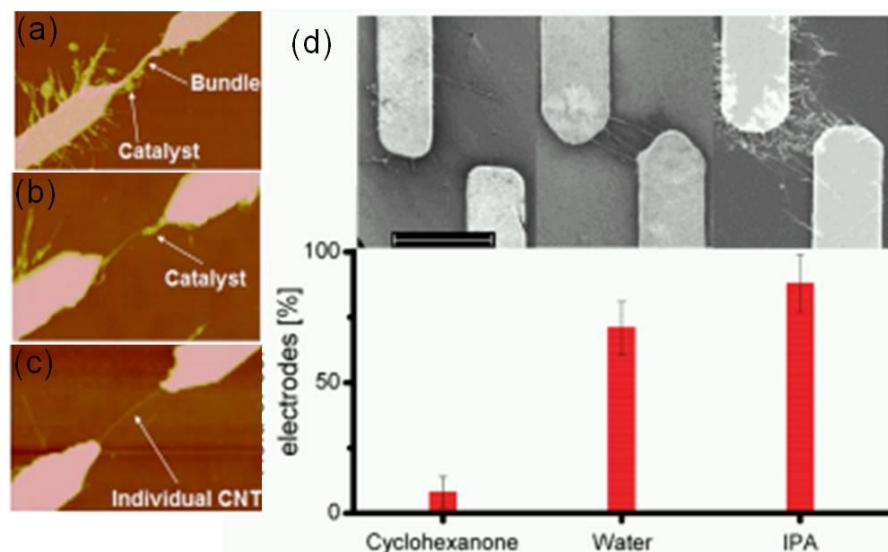


Figure 2.13 Effect of the presence of catalytic particles on DEP assembly of individual SWNT (a) from DMF solution, (b) from DCE solution, and (c) the Brewer Science solution. Scale bar: 1 μ m[91]. Reprinted (d) Statistics of electrode connection yield after dielectrophoresis of CNTs dispersed in cyclohexanone, water, and IPA. Representative SEM micrographs are presented for each solvent with a scale bar of 5 μ m[92]

The effect of catalytic particle on the assembly of individual SWNT is presented in figure 2.13 (a-c)[91], where homemade SWNT solutions (in DMF, and DCE), and commercial catalytic particle-free aqueous SWNT solution (from Brewer Science Inc)[50] were used. It was found that bundles of SWNT were assembled for both the DMF and DCE solution and catalytic particle were attached to the SWNT. Whereas the commercial surfactant free solution gives individual SWNT free from any catalytic particle. Along with being catalytic particle free, the SWNT solution also needs to be highly stable over longer period of time. For a stable SWNT solution, the concentration and the conductivity of the solution remain constant for a long period of time which allows reproducible assembly.

Properties of the solvent in which SWNT are immersed also plays an important role in the assembly. Since the conductivity, permittivity, and dielectric constant of SWNT and various solvents are different [90, 92-95], the DEP force is therefore unique for each solvent used, resulting in differences in assembly yield. SWNTs immersed in a solvent with a low conductivity experience a higher DEP force compared to a solvent with high conductivity [93]. Besides, solvent with a low dielectric permittivity does not contribute to the DEP force resulting in low DEP yield [90]. For example, the dielectric permittivity of both DI water and IPA is higher compared to that of cyclohexanone, which results in a higher assembly yield as shown in figure 6 (d) [92]. In addition, volatile solvents represent additional challenges as the solvent can be evaporated before the assembly can be completed.

Magnitude of the DEP force, and hence the assembly can be manipulated significantly by varying the amplitude and frequency of the applied AC electric field. At low voltage the deposition yield is low as the DEP force is not strong enough for to align the SWNT [96]. The

deposition yield increases with the increase of applied voltage. However, application of a very high voltage can break the assembled SWNT and therefore reduces the assembly yield. Typically a pick to pick voltage (V_{pp}) between $2V/\mu\text{m}$ to $5V/\mu\text{m}$ gives high deposition yield [97-100].

When an AC electric field is created SWNT solution is kept between the electrodes and an AC voltage is applied, the electrodes get polarized, a double layer consisting of surface charges and surface charge induced ions are attracted at electrode/solution interface [101, 102]. This gives rise to a potential (zeta-potential) between electrode surface and solvent which opposes the assembly of SWNT via DEP force. The zeta potential is inversely proportional to the applied frequency. Figure 7 (a) shows how the DEP force (F_{DEP}) and zeta potential (Z) varies with the frequency [103].

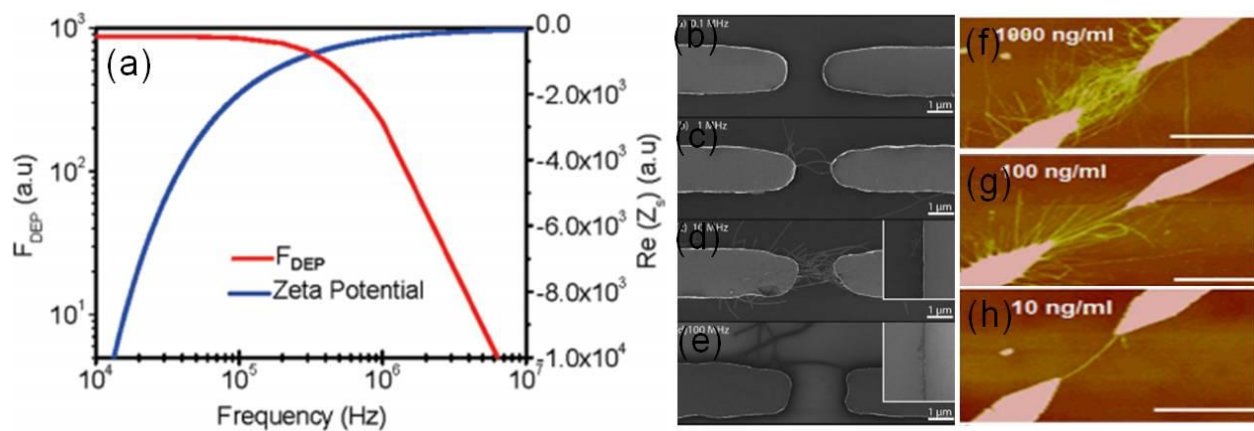


Figure 2.14 (a) Plot of DEP force (left axis) and zeta-potential (right axis) as a function of frequency [103]. Frequency dependent DEP deposition yield studies at constant potentials. (b) 100 kHz (c) 1 MHz. (d) 10 MHz, and (e) 100 MHz [104]. Dependence of solution concentration on the assembly of SWNT (f) 1000 ng/ml (g) 100 ng/ml, and (h) 10 ng/ml in the solution. Scale bar: 1 μm [91].

At low frequency zeta-potential become significant compared to the DEP force and the DEP deposition yield become low. At high frequency the zeta-potential diminishes and a higher DEP assembly yield obtained. However, the DEP force is start to decreases at very high frequency

thus an optimized frequency is required in order to obtain high deposition yield. For the assembly of individual SWNTs highest deposition yield are typically observed at frequency between 1-10 MHz. The effect of frequency on the DEP deposition yield is shown in fig 7 (a) – (d) [104].

DEP assembly of the SWNT is greatly affected by the concentration of SWNT in the solvent. By tuning the density of SWNT in the suspending medium, it is possible to control the number of SWNT between the electrodes. Figure 7(f-h) presents the how the number of SWNT between the electrodes varies with the concentration of SWNT in the solution (mixed)[91]. In this case, the applied voltage, the frequency and the assembly time was kept fixed. A lot of SWNT assembled in the channel when a high concentration solution is used. By systematically reducing the solution concentration even an individual SWNT can be assembled [105]. It is important to note that the solution concentration and DEP time are interrelated [106]. The number of SWNT between the electrodes can also be tuned to some extent by varying the DEP time while keeping the concentration fixed. For a particular solution concentration the SWNT density increases with the increase of DEP time. By keeping one of them fixed and varying the other parameter it is possible to control the number of SWNT in the channel [105, 107].

The dielectric oxide thickness and substrate conductivity play important role for the DEP assembly of SWNT. In particular, during simultaneous deposition method, the SWNT assembly yield is greatly influenced by the SiO₂ thickness. For a particular areal size of electrodes, the capacitance between the drain electrode and gate electrode (C_{DE-GE}) is inversely proportional to the thickness of SiO₂. Substrate with an optimized gate oxide thickness is required for an optimum capacitive coupling which will provide the highest deposition yield. For example, using

a 800nm SiO₂ layer, it was shown by xx et al that an assembly yield of up to 90% [97] is possible whereas 250 nm SiO₂ gives only ~ 25% [98-100].

For a particular type of SWNT solution and electrode pattern the DEP parameters can be optimized for high yielded assembly of individual SWNT. Changing the SWNT solution and electrode geometry require re-optimization of DEP parameters for the new design. Since different groups use different kinds of SWNT solutions, surfactants, substrates and electrode patterns, the optimized parameters are not universal and are different for each group. However once the parameters are optimized for a particular batch it will consistently give a similar device yield.

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CHAPTER 3: DEVICE FABRICATION AND EXPERIMENTAL METHODS

3.1 Introduction

Fabrication of a good device is the foundation of a good experiment in nanoscience research. Device fabrication involves many steps and all the steps are crucial. It requires significant effort to obtain a good device. All the devices described in this thesis consist of individual SWNT. The steps involving the fabrication process of individual SWNT devices are presented by the flow chart figure in 3.1. After successful fabrication of the devices electron transport measurement of the devices will be performed both at room temperature and at low temperature. The electron transport properties of those devices will be discussed in chapter 4, chapter 5 and chapter 6.

Here I will describe fabrication of metal electrode array using lithography techniques. Then I will discuss set up for assembly of individual SWNT using DEP. Parameter optimization for the high yield assembly of SWNT will be discussed in section 4. Finally, I will discuss the measurement setup for the room temperature and low temperature electron transport of SWNT devices.

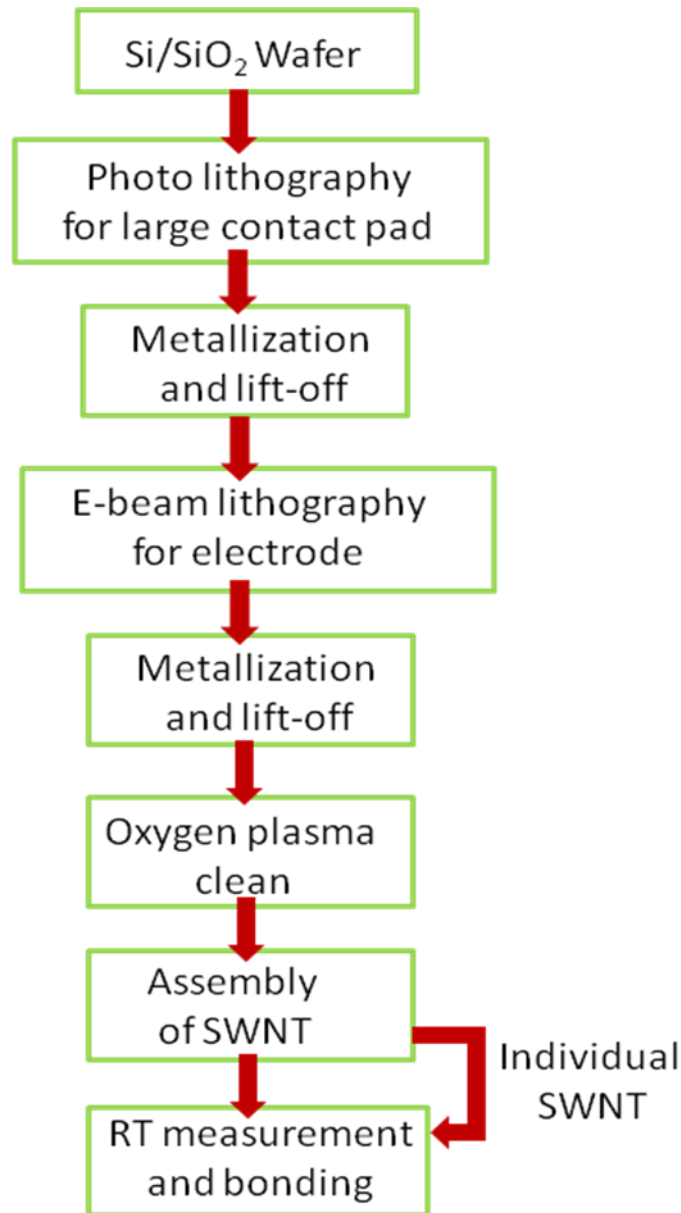


Figure 3.1 Flow-chart of the experimental procedures. Photolithography is used to define larger contact pads, followed by evaporation of Cr and Au, and standard lift-off. Electron beam lithography (EBL) is used to define smaller feature electrode followed by evaporation of Cr and Pd, and standard lift-off. Then the devices are, exposed to O₂ plasma etching for 15 minutes to remove residual resists. Individual SWNTs are then integrated between this metal electrodes via dielectrophoresis (DEP). Yield for SWNT assembly is checked via scanning electron microscope. Subsequently, the electron transport measurements of the devices are carried out at room and low temperature.

3.2 Electrode fabrication

I used a combination of photolithography and e-beam lithography (EBL) for the fabrication of electrodes. All the electrodes were defined on top of oxidized silicon substrates. I use highly doped (p-doped) Si-substrates so that they remain conductive at low temperatures and can serve as a backgate in our devices. Heavily doped ($< 0.005 \Omega\text{-cm}$) 3 inch wafer with a thermally grown 250 nm capped layer SiO_2 was purchased from Silicon Quest International. Photolithography is used to define large size contact pad and the alignment marker for the EBL.

3.2.1 Optical lithography

3.2.1.1 Double layer photo resist

Figure 3.2 portray the different steps involving fabrication of metal electrodes using photolithography. I use two layers of photo resist for the photolithography as it helps easier lift off for metal electrodes. Usually a highly sensitive resist is used as the bottom layer and a less sensitive resist is used as top layer[1]. An undercut is formed in the high sensitive bottom layer during wet etching following the photolithography. This undercut helps easier lift off by removing the continuous metal deposition through resist and developed area.

At first the 3-inch Si/SiO₂ wafer (purchased from Silicon Quest International[2]) is washed with acetone and iso-propyle alcohol (IPA) and blown dry with a stream of nitrogen gas. The bottom layer photoresist (purchased from MicroChem (LOR-3A))[3] is spin coated at 3000 rpm for 30 seconds and then soft baked on a hot plate at 150° C for 6 minutes. Then the top layer photoresist, Shipley S1318, purchased from MicroChem, is spin coated at 5000 rpm for 30 seconds on the wafer. The wafer is then soft baked at 100°C for 3 minutes. The thicknesses of bottom and top resists are ~ 500 nm and 1000 nm, respectively, which are confirmed from

MicroChem data sheets. It should be noted that a uniformly coated photo resist layer is needed for a consistent and continuous electrode pattern.

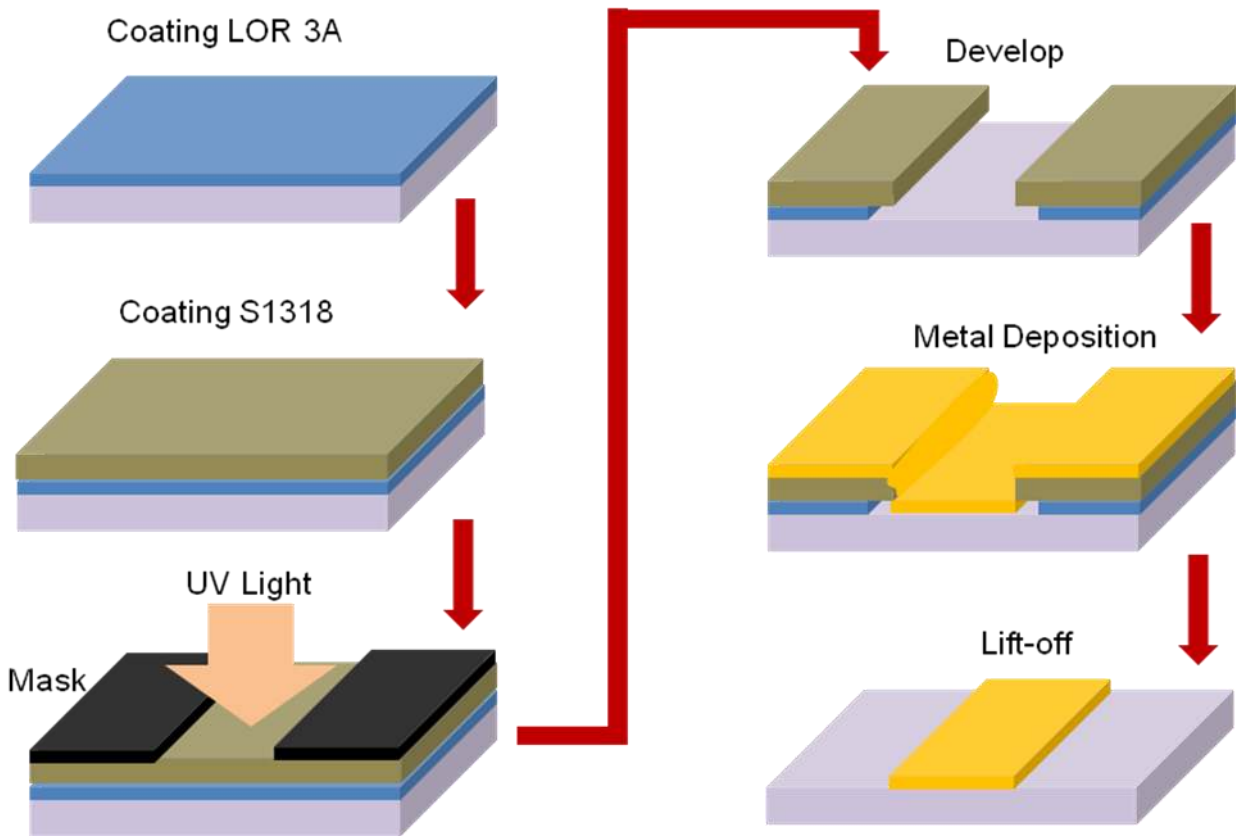


Figure 3.2 Schematic diagram of the photolithography process using double layer photoresist.

After coating the bi layer photo resist the wafer is placed in a UV mask aligner (Karl Sues). Photo mask with desired design is placed on the wafer and is exposed for 8 seconds. Following the photolithography, the wafer is developed in CD-26 for 10 seconds and washed with deionized (DI) water and blown dry.

3.2.1.2 Metallization

After photolithography, a combination of e-beam and thermal evaporation was used for the deposition of metal for contact pad. I use 5 nm of Cr as a sticking layer using e-beam evaporator. Cr deposition was performed with a constant rate of 0.015 nm/sec. After that 45 nm of Au was deposited at a rate 0.020 nm/sec using thermal evaporator. I keep the thickness 50 nm for the contact pad so that the wire can easily stick to the contact pad.

3.2.1.3 Lift-off

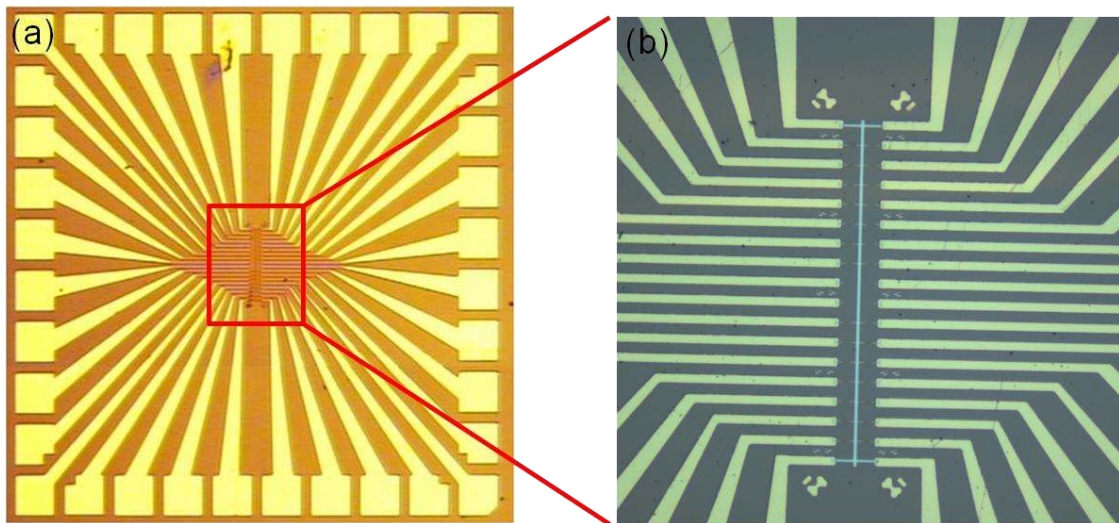


Figure 3.3 (a) Optical photograph of large contact pad defined by photolithography. (b) Zoom in image of the selected part of figure 3.3 (a).

After metallization the wafer is placed inside PG remover (obtained from MicroChem) solution and heated at 60°C for 5 min. The wafer is immersed in PG remover for 1-2 hour. A plastic pipet is used to squirt PG remover on the wafer in order to ensure that no metal is left. A sonication of 10-20 sec in an ultrasonic bath can help the lift off if still some unwanted metal are left. Then the wafer is washed in acetone, IPA, and DI water, and a stream of nitrogen gas is

used to dry it. Optical image of a 3-inch wafer with metal electrode array defined by photolithography is shown in figure 3.3 (a) and the expanded view of the chip is shown in fig 3.3 (b).

3.2.2 Electron beam lithography

After fabrication of large contact pads using optical lithography, EBL was used to define the smaller electrodes. Nano-patterned- generation-system (NPGS) attached to a scanning electron microscopy (SEM) (Zeiss 5500) system was used to define the electrodes in this step. I used both single layer photoresist, PMMA and double layer photoresist MMA/PMMA for electron beam lithography. I use single layer resist to define the source and drain electrode array. Double layer resist is used when a wing free feature is needed. Besides, lift-off is easier with double layer resist. I use double layer resist to define the local gate. However, for smaller feature size single layer resist is preferred over double layer resist.

In single layer EBL, I use PMMA positive photoresist with molecular weight of ~ 950 k purchased from MicroChem. The PMMA resist is spin casted at a rate of 4000 rotation per minute for 1 minute. After that the substrate is soft baked at 180°C for 15 min. Thickness of the PMMA layer obtained from the technical data sheets for this case is 150 nm. As a thickness of photoresist 3 times larger than the metal electrode thickness gives a good lift off, this thickness of 150 nm is good for the metal electrode of thickness 30 nm. While defining the electrode pattern via EBL, the photoresist was exposed with a dose of $280 \mu\text{C}/\text{cm}^2$ at 28 KV. Depending on the minimum feature size I choose different aperture size. For the accurate drawing of the electrodes I use the alignment marker drawn by photolithography.

After EBL exposure, the sample is immersed a mixed solution of Methyl-isobutyl-ketone : Isopropyl-alcohol (MIBK :IPA) at a ratio of 1:3 for 50 second followed by IPA (stopper) for 10 seconds and blow dry with nitrogen gas flow for development. Metal deposition was performed using e-beam evaporator or thermal evaporator. Metal for the electrode patterns are chosen based on the device need to be fabricated. For my case I use Pd for the source-drain contact as their work function matches with that of SWNT giving ohmic contact [4-6]. I evaporate 3 nm Cr as sticking layer and 25 nm Pd by e-beam evaporator. After metallization the sample ware immersed in to warm acetone (55°C-60°C) for 1 hour for lift-off. The sample is sonicated for 5-10 seconds if there still remain some metal at the edge of the electrodes. Then, the chips were washed throughly with IPA and DI water. Then the chips were placed inside a oxygen plasma chamber and etched for 15 minutes to get rid any unwanted PMMA residue. Figure 3.4(a) shows an SEM image of electrode pattern drawn by EBL.

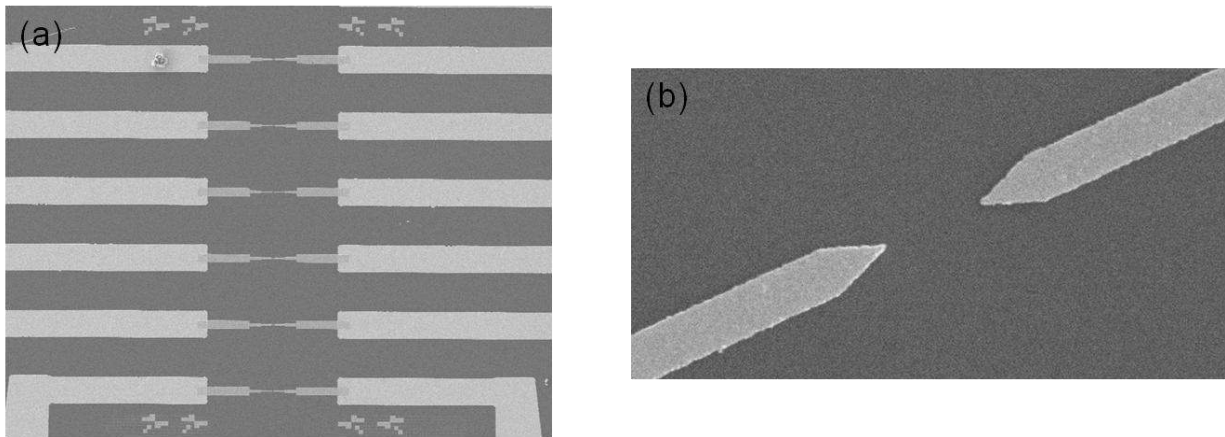


Figure 3.4 Scanning electron micrograph (SEM) of (a) metal electrode arrays defined by EBL (b) single electrode pair with a separated by 1 μm .

In double layer EBL, I use MMA resist purchased from MicroChem as the bottom layer. The MMA resist is spin coated at 4000 rpm for 60 second giving a thickness of 150 nm. Then the

substrate is placed on a hot plate and soft baked at 180°C for 15 min. After that PMMA resist (~950 k) is spin casted at a rate of 4000 rotation per minute for 1 minute followed by soft baking of the substrate at 180°C for 15 min. For double layer resist I use the same EBL parameters as single layer resist

3.2.3 Aluminum local gate fabrication

After defining the source-drain electrode pattern, Al local gate were defined via EBL at the middle of the channel for the fabrication of mechanical templated single electron transistor (will be discussed in section 5). While define the electrode pattern, I draw additional marker for the Al local gate. This additional marker will help aligning the local gate between the electrodes. Double layer resist (described in 3.3.2) was used to define the local gate. Double layer resist was used to ease the lift off and removal of wings from the sidewall of the local gate. After electron beam exposure the sample was developed using MIBK: IPA (1:3) for 60 seconds and rinsed with IPA for 10 seconds. Then the sample is loaded in the evaporator for AL deposition.

Before deposition metal for local gate a thin sticking layer of Cr (2nm) was deposited. After that 18 nm local gate was deposited using e-beam evaporation. If deposited at room temperature, thin film films of Al appears to be grainy and oxide grown on top of this will not be uniform. This would result in current leakage through the local gate. In order to obtain grain less smooth Al thin film, I cooled the sample stage with liquid nitrogen before the Al deposition [7, 8]. Special care should be taken during low temperature Al deposition. Before cooling the sample stage with liquid nitrogen the outer cylinder of the evaporator need to be filled with liquid nitrogen. The inner wall of the side wall will be cooled and all the impurities will be attached to the wall and the pressure fall down very quickly. If the side wall is not cooled before

cooling down the sample stage, all the impurities will be deposited on the sample and creates insulating layer. Because of this after deposition of Al no electrical connection would be made. After Al deposition the sample would be immersed in acetone for lift off and washed with IPA and DI water. Following lift off the samples would be treated by oxygen plasma for 12-15 minutes to ensure 2-3 nm Al_2O_3 layer.

3.3 Dielectrophoresis of SWNTs for device fabrication

I will describe a short outline for the DEP assembly of individual SWNT for the device fabrication here. I will also discuss the experimental set up for DEP assembly.

3.3.1 SWNT solution for DEP

For the assembly of SWNT based devices I use commercially available aqueous solution. I used mixed SWNT solution purchased from BerewerScience [9]. SWNT purchased from BerewerScience are free from catalytic particle and surfactant. This solution contain mixed SWNT i.e. contain both metallic and semiconducting SWNT. This is a stable solution with a shelf life of 6 month. However this solution can be used more than 1 year without any degradation of the solution. The average diameter of the SWNTs in the solution was ~ 1.7 nm as determined by atomic force microscopy[10] and has a length distribution 1-5 μm . The concentration of SWNT's in the originally purchased solution is ~ 50 $\mu\text{g/ml}$. Before DEP, the we added DI water to the solution to obtained desired concentration I used this solution to fabricate metal- contact SET and mechanical templated SET.

I also used chirally separated all semiconducting (99%) solution purchased from NanoIntegras[11]. The s-SWNTs have a diameter distribution of 0.5 to 3.9 nm with an average of average of 1.6 nm, while the length ranged from 0.5 to 4.0 μm with an average value of 1.8 μm as determined from atomic force microscopy (AFM) and scanning electron microscopy (SEM) study [12]. As it is a surfactant based solution, I washed the chip in DI water after DEP assembly in order to get rid of the surfactant. One problem with this solution is that the carbon becomes aggregated after 5-6 months. Assembly yield is severely affected if this aggregated solution is used for DEP since we need individual SWNT for the device fabrication. To ensure this each time before making the solution we sonicate the mother solution in an ultrasonic bath for 20 seconds.

3.3.2 Experimental setup for DEP:

Figure 3.5 (a)-(b) shows the experimental set up for the DEP assembly for the assembly of individual SWNT. I used taper shaped electrodes with sharp tips for the assembly of individual SWNT. For taper shaped electrode, electric field is strongest at the tips, which increase the probability of the alignment of individual SWNT[13]. Few mL of SWNT solution of optimized concentration a onto the substrate with electrodes and an AC electric field of desired frequency created by function generator is applied between the metal electrodes (Fig. 3.5(a)). SWNT in the solution experience DEP force and align between electrodes. Figure 3(b) shows another DEP assembly technique where AC voltage is applied between a common source and gate electrodes, this thechnique is commonly known as simultaneous assembly technique as it allows simultaneous deposition of individual SWNT. In this thesis I use both techniques for the

assembly of individual SWNT. Details about the DEP assembly using this method will be discussed in chapter 4 and chapter 5.

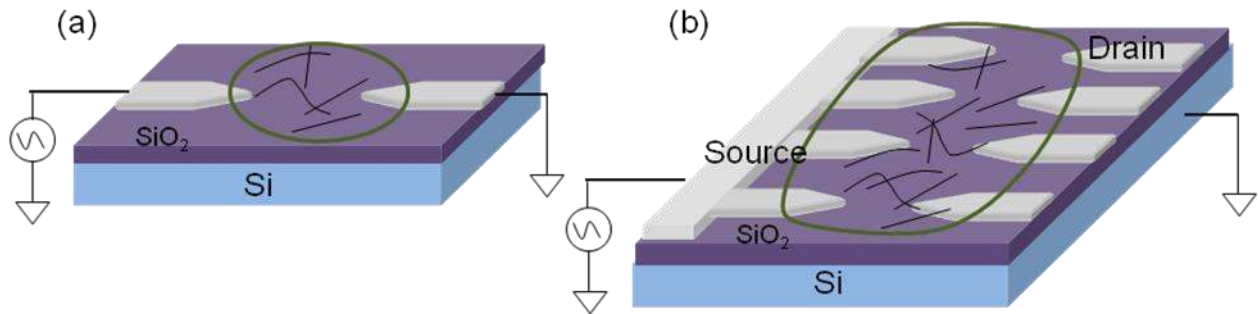


Figure 3.5 (a) Schematic of the DEP assembly set-up for the assembly of carbon nanotube. (a) Point-to-point deposition and (b) simultaneous deposition

3.4 Setup for electrical measurement

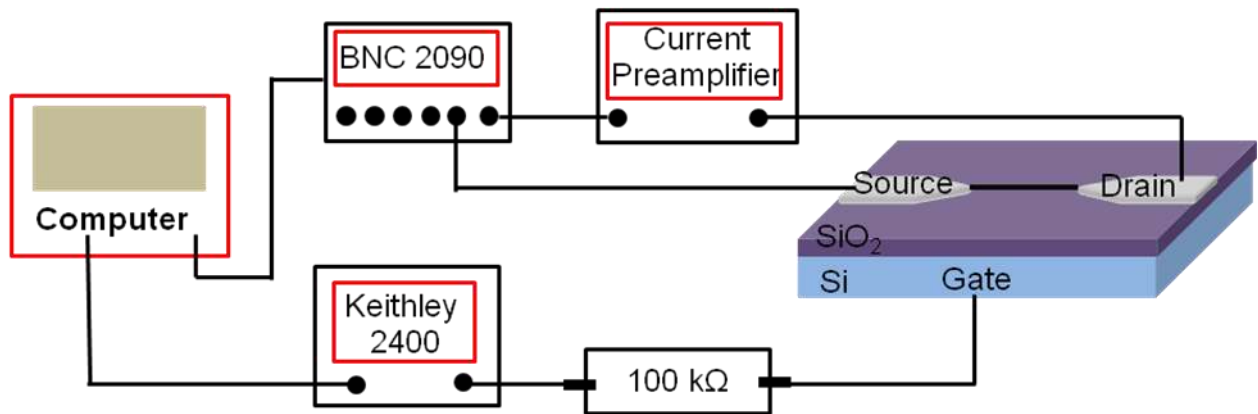


Figure 3.6 Schematic for the room temperature electron transport measurement set-up of SWNT devices

The set up for electron transport measurements of DEP assembled individual SWNT devices is shown in Figure 3.6. A DC power supply, electrometer (BNC 2090 from National

Instrument) and a current preamplifier (DL 1211) capable of measuring sub-pA signal were used. The gate voltage was applied using a Keithley 2400. A resistor having high resistance (100 K Ω) is connected in series with the gate. This will save the device from application of very high voltage to the gate. Before measuring the electron transport of the devices the leakage current was measured. A very low leakage current $> 1\text{pA}$ was obtained for up to $\pm 20\text{ V}$ of gate voltage.

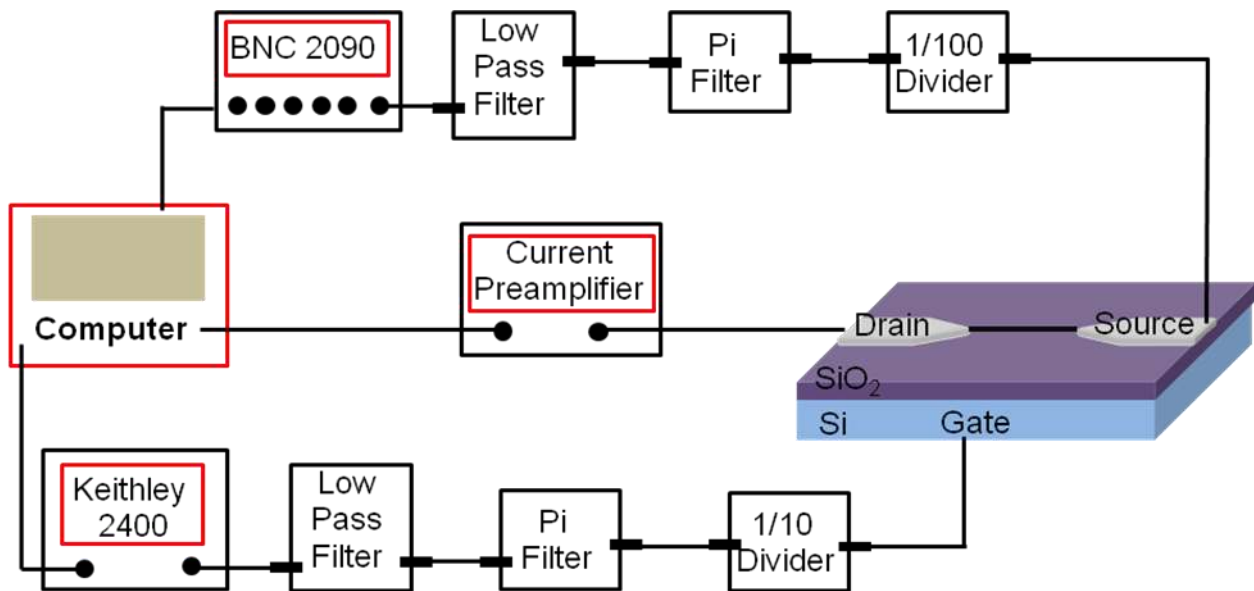


Figure 3.7 Low temperature measurements setup for SWNT SET at low temperature.

The measurement software used is LabVIEW (National Instrument Co.). Low temperature measurement set up is shown in figure 3.7. At low temperature the current signal is low which can be destroyed by the noise present in the line. To reduce noise I use several filters. The Keithley 2400 source-meter is connected to a low pass filter, which pass through a low pass filter. After filtering the signal pass through a 1:10 divider. Current divider is used to improve the voltage resolution.

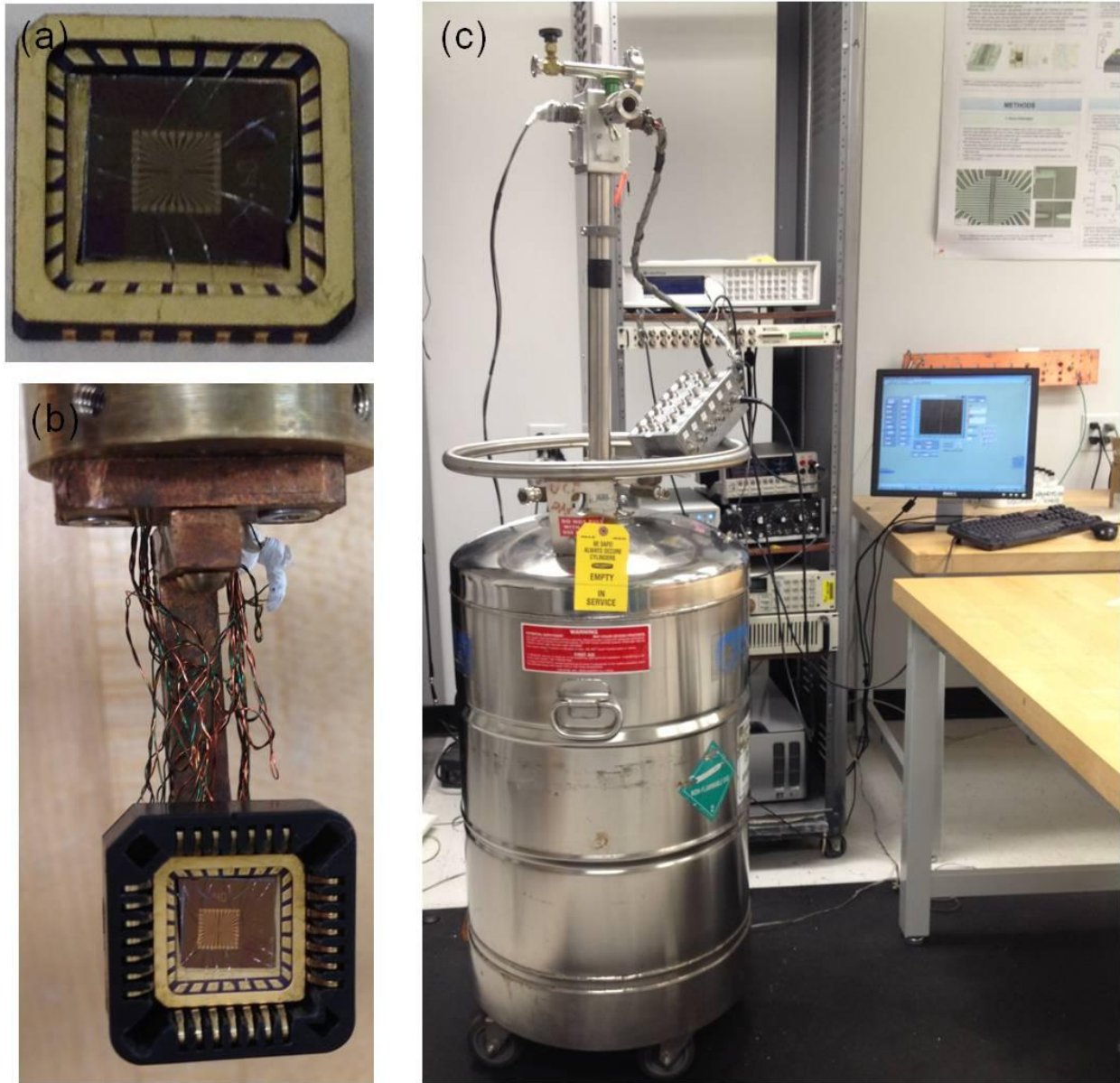


Figure 3.8 Low temperature measurements set up (a) Chip containing SET devices bonded to a chip carrier via aluminium wire (b) bonded chip loaded into a variable temperature ^4He cryostat (c) The cryostat is loaded into a 30 liter He dewar

Prior to the measurement, the chip were attached to a chip carrier. A wire bonding machine is used to attach the chip to the chip carrier via aluminum wires. Backgate of the chip is connected to the surface of the chip carrier via silver pest. Figures 3.8 (a) shows the image of a

bonded chip. After wire bonding the chip is placed onto a ^4He cryostat as shown in Fig 3.8 (b). to perform the low temperature measurements the cryostat is placed inside a liquid He dewar (NanoFAB), presented in Figure 3.8 (c).

3.5 References

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CHAPTER 4: HIGH YIELD ASSEMBLY OF CARBON NANOTUBE FOR DEVICE FABRICATION²

4.1 Introduction

Single-walled carbon nanotubes (SWNTs) have attracted tremendous attention as a promising building block for future nanoelectronic circuits [1-5]. Transistor fabricated from individual SWNTs have demonstrated outstanding device performances including very high mobility, near ballistic conductance and resistance against electromigration, surpassing the properties of current Si based complementary metal oxide semiconductor (CMOS) devices [3, 5]. However, there are several challenges that need to be addressed before SWNT based devices can find widespread practical applications. The most challenging among them are the large scale integration of SWNT in the circuit. This can be addressed by developing strategies to assemble SWNTs at selected positions of the circuits with high yield. Several techniques have been developed for high yield directed assembly of SWNT, including direct growth by chemical vapor deposition (CVD) [6-11] and post-growth solution processing by AC dielectrophoresis (DEP) [12-16]. The CVD technique uses patterned catalytic islands in combination with high-temperature treatment to grow nanotubes directly on a substrate [6-10]. The best optimization of assembly and FET yield reported by Javey et al [6] showed that using the direct growth technique it is possible to assemble individual SWNTs with about 40% yield. However, CVD process requires high growth temperatures in excess of 900°C [6-8, 18-19] making it

² Part of the work presented in this chapter are extensions Muhammad R. Islam, Kristy J. Kormondy, Eliot Silbar, and Saiful I. Khondaker, A general approach for high yield fabrication of CMOS compatible all semiconducting carbon nanotube field effect transistor. *Nanotechnology* 23, 125201 (2012).

incompatible with current CMOS technology. An alternative to direct growth technique for CMOS compatible device integration is the assembly of SWNT from solution phase. Although there are speculations that solution processed SWNTs may be defective and may not be practical for high quality device applications, we have recently shown that progress in solution

In this chapter I will discuss strategy for high assembly yield of individual SWNT. I will describe the optimization of DEP parameter to obtain high throughput for device integration. I will also discuss the electron transport properties of the DEP assembled SWNT devices. I will also describe a strategy to obtain high SWNT transistor yield together with high assembly yield by using all semiconducting SWNT.

4.2 Optimization of DEP parameters for high yield assembly of SWNTs

Integration of individual SWNT is one of the most important and challenging parts of device fabrication. Presence of a straight, single SWNT is desirable for device fabrication. As discussed in previous chapter 2, DEP allows precise positioning of individual SWNT at the desired position of the circuit. The assembly of individual SWNT depends on several parameters such as AC voltage applied, frequency of the AC voltage, DEP time, solution concentration, and substrate thickness. Of which (1) The concentration of SWNTs in the solution, and (2) DEP Time are most important.

In my research I use Si with thermally capped 250 nm SiO₂ as the substrate. For the assembly of SWNT we used a stable, surfactant free aqueous solution of SWNT obtained from commercial source [20]. The average diameter of the SWNTs in the solution was ~ 1.7 nm as determined by

atomic force microscopy (AFM) and having a median length of $\sim 2 \mu\text{m}$ [20]. The concentration of SWNT's in the mother solution is $\sim 10 \mu\text{g/ml}$ with a shelf life of 6 month.

One of the easiest ways to optimize the parameter for the high yield assembly of individual SWNT is to vary one of the parameters while keeping all the other DEP parameters fixed. To obtain a highest assembly yield I use a AC electric field with amplitude 5 Vp-p and frequency of 1 MHz. For the assembly, the concentration of s-SWNT in solution was diluted with deionized (DI) water from the original value of $10 \mu\text{g/mL}$ to a desired concentration. A small drop ($2\text{-}3 \mu\text{L}$) of solution was placed on top of a chip immediately after the preparation of the solution. After that the AC voltage was applied between the source and drain electrode for a fixed amount of time. Figure 4.1 shows a carton of DEP assembly set up that I used. Then the AC voltage is withdrawn and moves to the next electrode pair. To optimization of DEP time for individual SWNT, I varied the SWNT solution concentration and DEP time and check the assembly.

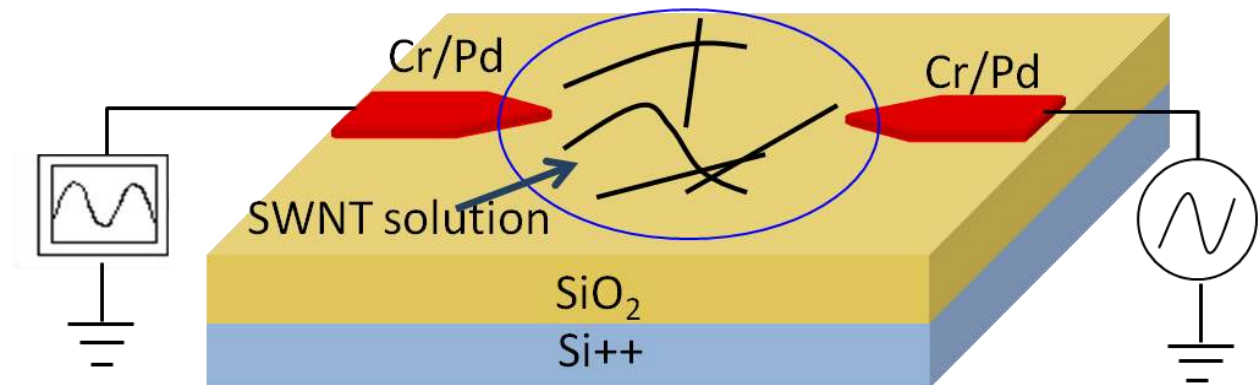


Figure 4.1 Schematic diagram of the DEP assembly set up.

4.2.1 Optimization of DEP parameters: solution concentration

The assembly of SWNT is directly related to the concentration of concentration. A solution concentration of solution will results in a thin film of SWNT in the channel between the electrodes whereas using a low concentration will yield no SWNT in the channel. The SWNT solution we used has an original concentration of 10 $\mu\text{g}/\text{mL}$. I dilute it to three different concentration 1000 ng/mL, 100 ng/mL and 10 ng/mL by adding DI water into it.

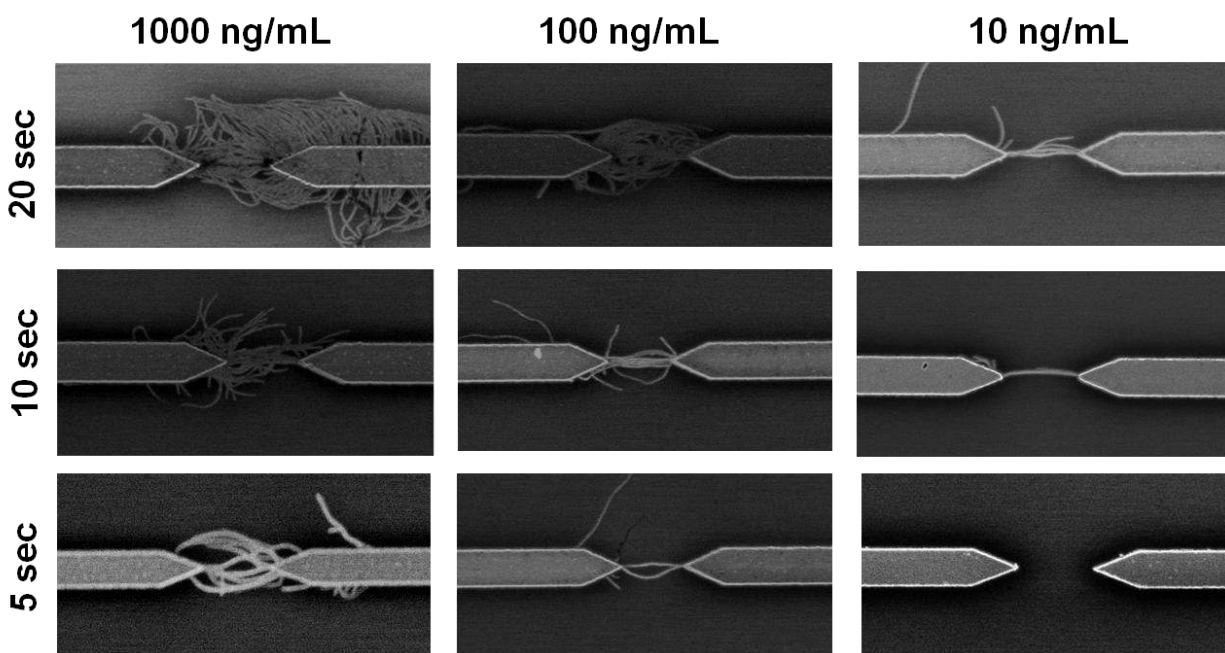


Figure 4.2 Scanning electron micrographs (SEM) image of a number of individual SWNT deposited by dielectrophoresis (DEP) at three different concentration 1000 ng/mL, 100 ng/mL and 10 ng /mL and a DEP time ~ 20sec, 10 sec and 5 sec. Distance between adjacent electrodes is 1 μm for all images

When a large solution concentration is used a large change in output voltage is observed once the AC voltage is set means that the channel is connected by a number of SWNT. We use three different DEP time DEP times: 5 sec, 10 sec, and 20 sec for each solution concentration and

study the DEP assembly yield. The SEM image of the devices obtained by using different DEP time with different solution concentration are shown in Figure 4.2. Definitely a higher solution concentration together with high DEP time results in a large number of SWNT in the channel. The number of SWNT can be reduced by changing the solution concentration or by reducing the DEP time. From figure 4.2 it observed that a 5 sec DEP assembly with a solution concentration of 10 ng/mL will give an individual SWNT.

4.2.2 Optimization of DEP Parameter: DEP time

I also optimize the DEP time for obtaining highest individual SWNT yield. In this case I kept the same AC voltage and frequency that I used in previous sub-section. To optimization of DEP time for individual SWNT, I varied the DEP time and check the assembly. Three different time 5 sec, 10 sec, and 20 sec was used for the assembly. The outcome of DEP aseembly is shown in figure 4.3.

For a DEP time of 10 sec the assembly yield was low, in most cases SWNT were not present between the source and drain electrodes. A total of 60 electrode pairs that we used for this assembly, we found that only 5 electrodes were connected by individual SWNT giving a total of 8% assembly yield. Higher assembly yield yield was obtained for 10 sec DEP time. The numbers of SWNT between the electrodes vary between 1 to 3 for this assembly. Out of the ~400 electrode pairs used in this study, we found that on an average 25% were bridged by individual SWNT, another 5% were connected by 2 SWNTs and 3% were connected by 3 SWNTs giving a total of 33% assembly yield. To improve the assembly yield, the DEP time was increased to 20 sec while keeping other parameters fixed. A total of 76 electrode pairs that we

used for this assembly, we found that 69 electrode pairs were bridged with 1-5 s-SWNTs giving an average assembly yield of 90%.

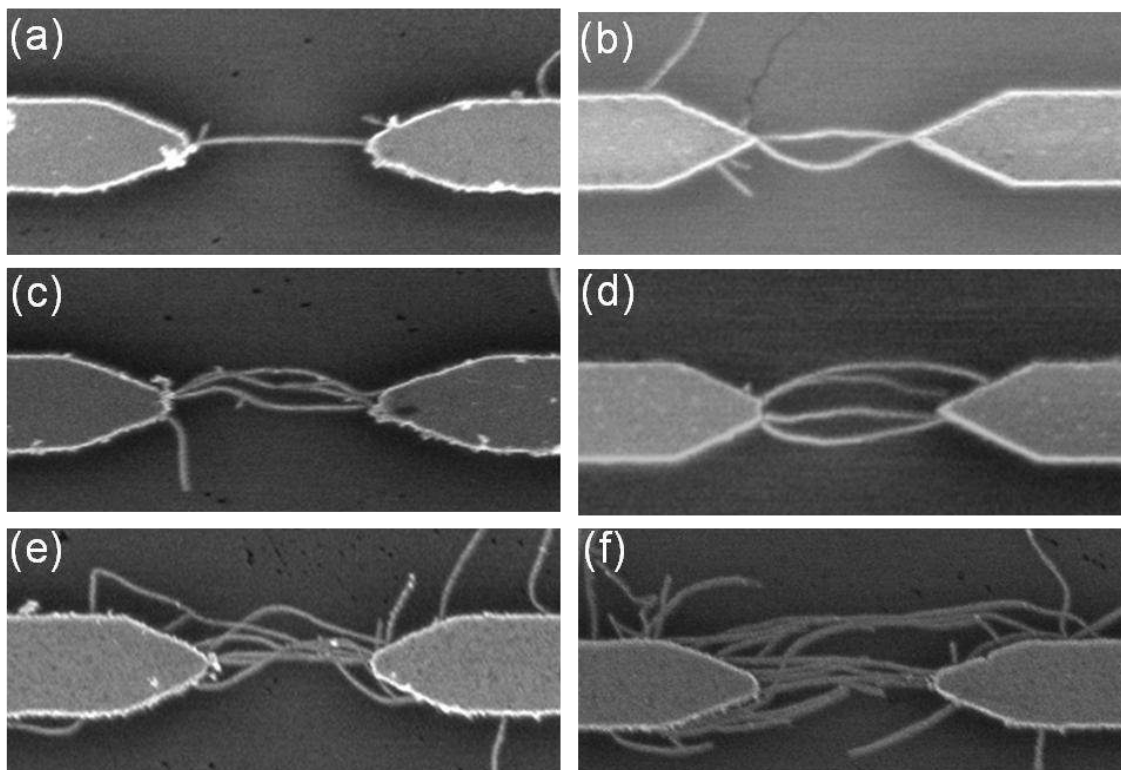


Figure 4.3 Results of DEP assembly for 10 sec DEP time and a solution concentration of 10 ng/mL. SEM images for the DEP assembled devices containing (a) one (b) two (c) three (d) four (e) six and (f) eight s-SWNTs between the electrodes..Separation between the electrodes in each case is 1mm.

In this assembly 15% of the electrodes were connected by individual SWNT, 60% by 2-3 SWNTs and 25% by 4-5 SWNTs. We have attempted to increase the assembly yield further by increasing the DEP assembly time to 35 sec while keeping all other DEP parameters fixed. Out of the 54 electrode pairs used in this study, all of them were connected by 1-10 s-SWNTs per site giving an assembly yield of 100%. Here, 55% of the devices were bridged with 1-5 s-SWNT and

the rest of the devices had 6-10 s-SWNT per site. Figure 4.3 (a-f) show representative SEM images of the DEP assembled s-SWNT devices containing one (fig 4.3a), two (fig 4.3b), three (fig 4.3c), four (fig 4.3d), six (fig 4.3e) and eight (fig 1f) s-SWNT per site.

4.2.3 Assembly of individual SWNT via DEP

From the above discussion it is clear that a solution concentration of 10 ng/mL, and a DEP time of 10 sec will give a higher assembly yield for individual SWNT.

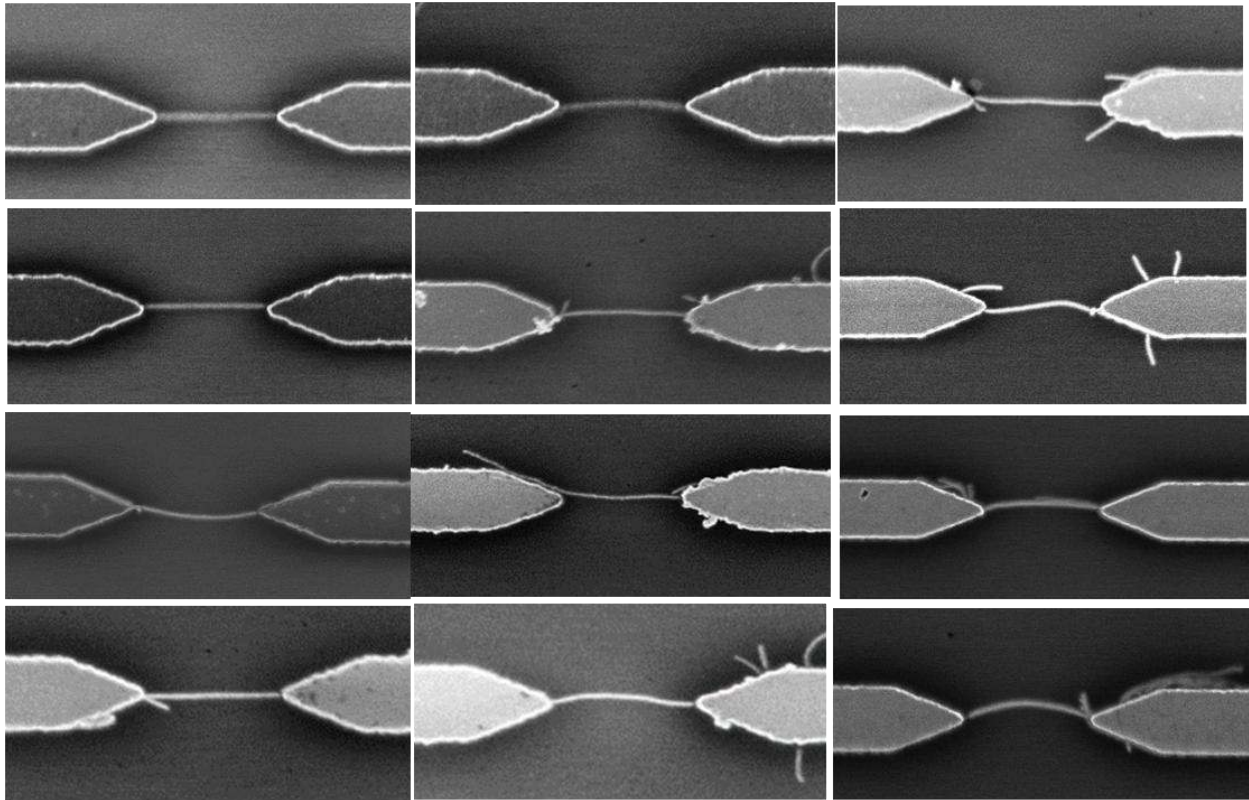


Figure 4.4 Scanning electron micrographs (SEM) image of a number of individual SWNT deposited by dielectrophoresis (DEP). Channel length is 1 μm .

Using this DEP parameters, an average $\sim 23\%$ of the electrode pairs were found to be bridged by individual SWNT. For the rest of the electrodes, no SWNT is presented in the channel, a smaller

SWNT is connected to any of the electrode, or several SWNTs are connecting the electrodes. For the successful deposition cases, mostly a single SWNT was present in channel, without having any short SWNT connected to the electrodes. This is desirable for the fabrication of SET because the presence of a short SWNT in channel acts as a memory node and affects the transport. Figure 4.4 shows the SEM images a number of source-drain electrode pair's attaché with individual SWNT.

4.3 Room temperature transport properties of SWNT devices

After assembly we measured the electronic transport measurement of the devices. For the transport measurement we used heavily doped SiO₂ as back gate. Below I will discuss the room temperature transport properties of SWNTs.

4.3.1 Transport properties of metallic SWNT devices

Figure 4.5 shows the transfer characteristics (drain current I_{DS} versus backgate voltage (V_G) measured at a fixed source-drain bias voltage $V_{DS} = -0.5V$ for an individual metallic SWNT (m-SWNT) devices. Metallic devices show a little or no change in I_{DS} as a function of V_G .

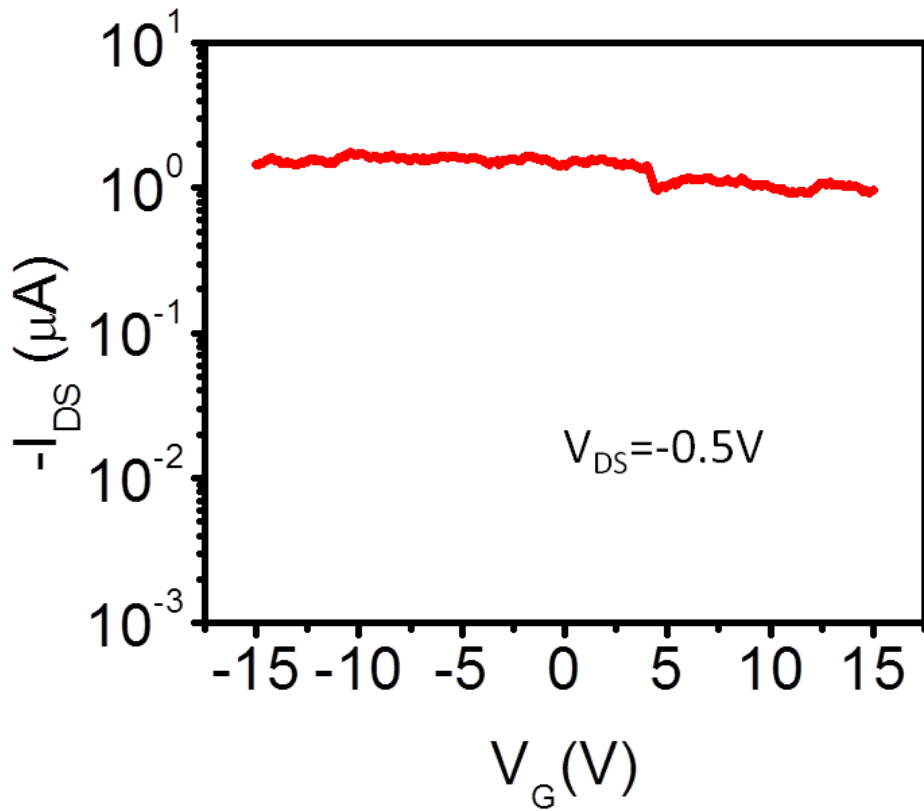


Figure 4.5 Transfer characteristics of a representative individual metallic SWNT device.

4.3.2 Transport properties of semiconducting SWNT devices

Figure 4.6 (a) shows the transfer characteristics for performing typical individual semiconducting SWNT (s-SWNT) devices measured at a fixed $V_{DS} = -0.5V$ before and after thermal annealing. A switching behavior in I_{DS} going from on state to off state is observed as we sweep the gate voltage. In addition, the current on-off current (I_{on}/I_{off}) ratio and on-state conductance ($G_{on} = I_{on}/V_{DS}$) are increased significantly after annealing. The $G_{on} = 0.2 \mu S$ for the as-assembled device which after thermal annealing increased by an order of magnitude to $\sim 2\mu S$.

The I_{on}/I_{off} of the device was increased from 2.3×10^3 to 2×10^4 after annealing. The subthreshold swing $S = [d \log I_D / dV_G]^{-1}$ of the device before and after annealing are 1.5 V/dec and 1.4 V/dec respectively, typical of backgated s-SWNT FET devices [12-13, 35-36]. Figure 4.6(b) shows the output characteristics (I_D vs V_{DS}) for the same device up to the saturation regime at different gate voltages (from -10 V to 10 V in a gate steps of 2.5 V) after annealing.

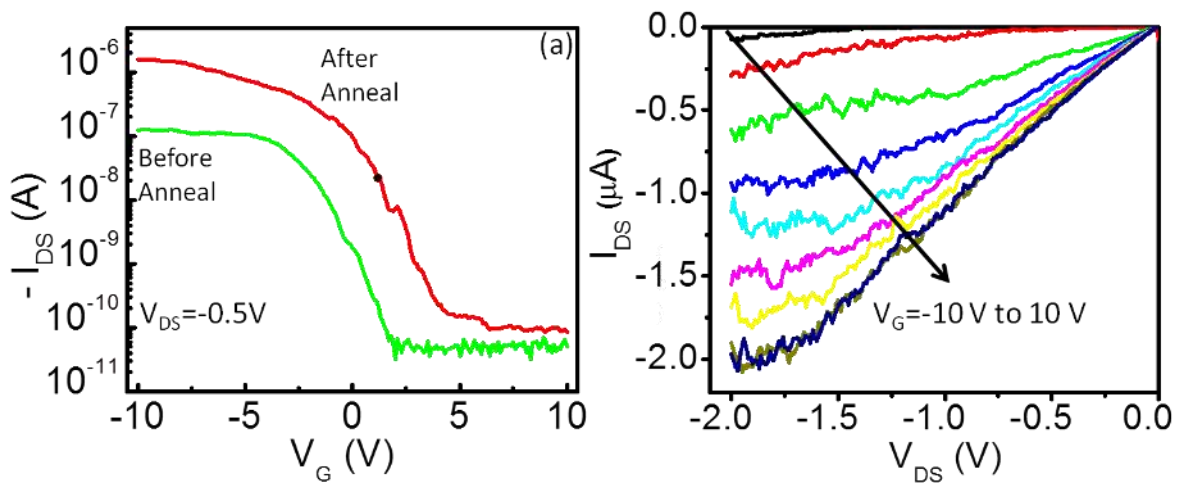


Figure 4.6 (a) Transfer characteristics of a representative individual SWNT FET device before and after annealing. $V_{DS} = -0.5$ V. (b) Output characteristics of the same device...

The output current show linear behavior at low bias and saturation at high bias voltage indicating that the current is not limited by contact resistance or short channel effect. The mobility of the device was calculated using the relation $\mu = (L^2 / C_G \times V_{DS}) (dI_{DS} / dV_G)$, where L is the channel length of the device and $C_G = (2\pi\epsilon L) / \ln(2h/r)$, is the gate capacitance, where ϵ is the effective dielectric constant of $\text{SiO}_2 \sim 3.9\epsilon_0$, h is the thickness of the oxide and r is the radius of the s-SWNT. The mobility was found to be $28 \text{ cm}^2/\text{Vs}$ and $210 \text{ cm}^2/\text{Vs}$ before and after annealing respectively. The mobility value after anneal is comparable to other high quality solution processed individual s-SWNT FET device fabricated from mixed SWNT solution.

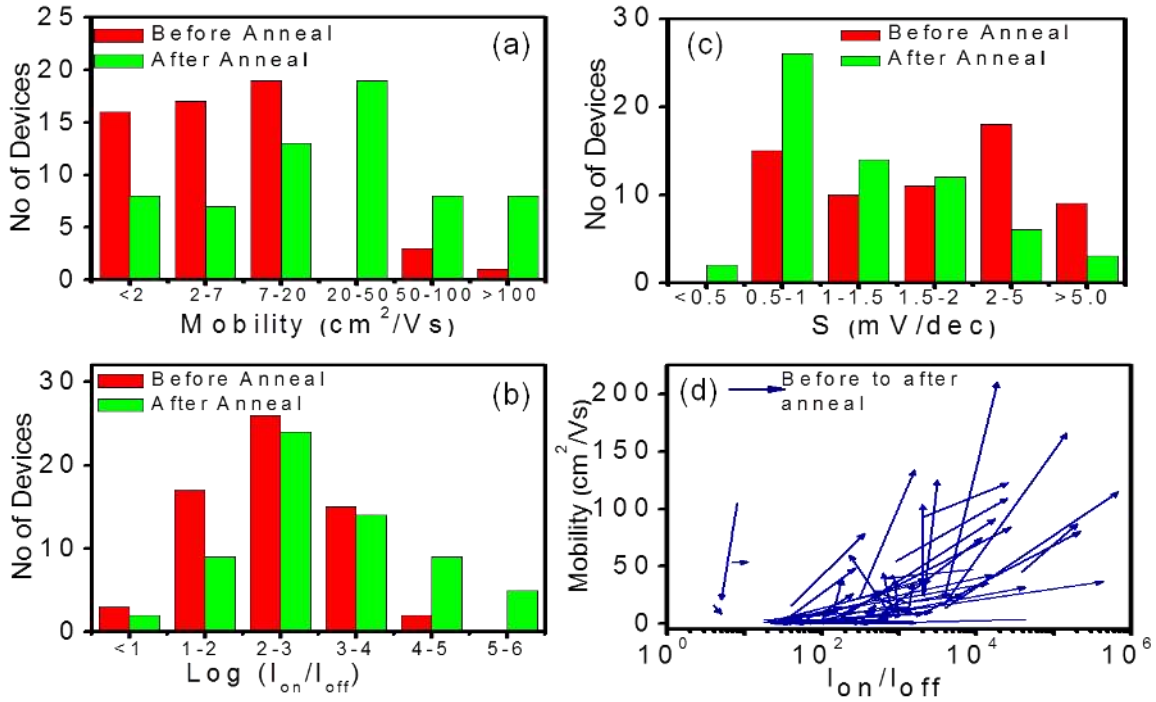


Figure 4.7 Summary of FET properties for all individual s-SWNT devices before and after anneal. Histogram of mobility(a), Ion/Ioff (b), subthreshold swing S (c), and Vector diagram of mobility and Ion/Ioff representing the changes of each SWNT FET upon annealing (d).

The increased on current, on/off ratio and mobility after annealing can be attributed to a the reduction of Schottky barrier height between the metal electrode and s-SWNT after annealing [37]. This reduced barrier favors injection of hole, causing high on current, which in turn increases on/off ratio and mobility.

Detailed FET characteristics were measured before and after anneal for a total of 63 individual s-SWNT devices. This is summarized in Figure 3 where we show histograms of μ , I_{on}/I_{off} , S as well as vector plot of μ vs I_{on}/I_{off} . Figure 4.7(a) shows that μ of the as assembled devices varied from 1 to 113 cm²/Vs with an average of 13 cm²/Vs, which after annealing increased to 2 to 210 cm²/Vs with an average of 40 cm²/Vs. The variation of S before and after

annealing is shown in figure 4.7(b). The median value of S decreased from 1.2 to 1 V/dec after annealing. This improvement can be attributed to the reduction of trap charges between the SiO_2 and s-SWNT interface [38]. Figure 4.7(c) shows the median value of I_{on}/I_{off} increased from 184 to 720 (mean value from 2×10^4 to 3×10^5) upon annealing. The median on conductance also increased from 0.03 μS to 0.2 μS due to annealing. Figure 4.8(d), a vector plot showing how the mobility and I_{on}/I_{off} changes for each of the measured devices upon annealing. A maximum increase of μ and I_{on}/I_{off} from 28 to 210 and 10^2 to 2.7×10^4 (or, 4×10^3 to 6.8×10^5) has been observed respectively. As discussed in previous section the reason for such improvements is the reduction of contact barrier upon annealing. Two important conclusions can be drawn from here. From figure 4.7(c), we see that 61 out of the 63 devices measured shows on off ratio more than one order of magnitude, signifying a FET yield of 97%. By combining properties of a few other devices containing 2-3 SWNTs (discussed in the following section) from the 5 sec assembly, the FET yield remained 97%. Here the devices with I_{on}/I_{off} greater than 10 were considered as FET [8]. However, if we choose the $I_{on}/I_{off} > 3$ as FET as mentioned in ref [25] the FET yield would become 99%. Figure 4.7 also show that the FET properties vary from device to device. Such variations may be explained by the differences of chirality and diameter from tube to tube; these physical features affect the bandgap and contact resistance of the s-SWNT, and in turn the mobility, on/off current ratio and subthreshold swing of each device [39-40]

4.4 General approach for the assembly of all semiconducting carbon nanotube devices

In the preceding section we demonstrate controlled assembly of the solution processed SWNTs have been demonstrated at individual level using mixed carbon nanotube solution.

Those devices shows excellent transport properties including large mobility, and high on-off ratio. However in DEP metallic SWNT feel a greater force than semiconducting SWNT during the assembly [24]. Therefore, while using a mixed solution of semiconducting and metallic SWNTs, a FET yield of 50% or lower was demonstrated, leaving a large fraction of devices non-functioning [13,25]. In this respect, it is important to fabricate devices using all semiconducting nanotube solution. Recently, solution based sorting techniques have been developed to separate nanotubes by chirality [26-28]. In particular, density gradient ultracentrifugation (DGU) approach of surfactant-based separation has been used to sort semiconducting SWNT in aqueous solution [26]. Raman studies of such sorted SWNTs show 99% of them are semiconducting [29]. These sorted nanotubes may hold the key to address the challenges of high yield CMOS compatible fabrication of SWNT FETs [30-32].

In this section, to address the aforementioned issues we used such a semiconducting-enriched high quality SWNT solution in combination with DEP to achieve high yield of SWNT-FETs and surveyed the electronic properties of the device statistically. We demonstrate that by optimizing the DEP time, an assembly yield of 90% is obtained with the 1-5 s-SWNT per device where 90% of the device shows FET behavior. A 100% assembly yield can be possible by further increasing the DEP but this increases the number of SWNT per device that reduces the FET yield to 59%.

4.4.1 Electron transport measurements of 1-5 s-SWNT devices

We now examine the transport characteristics of the devices assembled with a DEP time of 20 sec containing 1-5 s-SWNTs. Since annealed devices show better performance compared

to as assembled devices as discussed in previous section, from now on, we no longer discuss the properties of as-assembled devices. Figure 4.8(a) show the transfer characteristics of this device at different bias voltages showing p type behavior with $I_{on}/I_{off} \sim 2 \times 10^4$. The output characteristic curve of this device upto the saturation regime at different gate voltages is shown in figure 4.8(c). The on conductance of the device is 3 μ S and output current is up to $\sim 8 \mu$ A. The value of I_{on}/I_{off} is similar to that of individual SWNT however the on conductance and output current is higher than individual SWNT. For devices containing more than 1 SWNT, we did not attempt to calculate mobility due to the ambiguity in determining the channel width. Instead, we calculated the value of $S = 1.9$ V/dec, similar to what has been obtained for individual s-SWNT devices. Similar characteristics were measured for many devices containing 2-3 s-SWNT. The I_{on}/I_{off} for 41 such devices are shown in the box diagram (green box) of fig 4.8(e). From here, we see that the I_{on}/I_{off} of most of the devices bridged by 2-3 s-SWNT are higher than two orders of magnitude with a median value $\sim 3 \times 10^2$, similar to what has been observed for the individual s-SWNT device. Out of the 41 devices, 38 devices show on-off ratio more than one order of magnitude. This suggests that device fabricated by 2-3 s-SWNTs are similar to that of the individual s-SWNT FET, however with an increased on conductance.

Transfer characteristics of another device with 4 s-SWNT is shown in figure 4.8(c) with an $I_{on}/I_{off} \sim 10^2$. Output characteristic of the device is presented in figure 4.8(d), showing a higher output current (12 μ A), however, without a saturation. The red box of figure 4.8(e) represents the variation of I_{on}/I_{off} of all the 18 devices containing 4-5 s-SWNT. It has also observed that the median I_{on}/I_{off} for 4-5 s-SWNT device is 25 which is one order of magnitude lower compared to

1-3 s-SWNT devices. This may be explained using figure 4.7(c) where we see a variation of I_{on}/I_{off} from 10 to 10^5 for the individual SWNT devices.

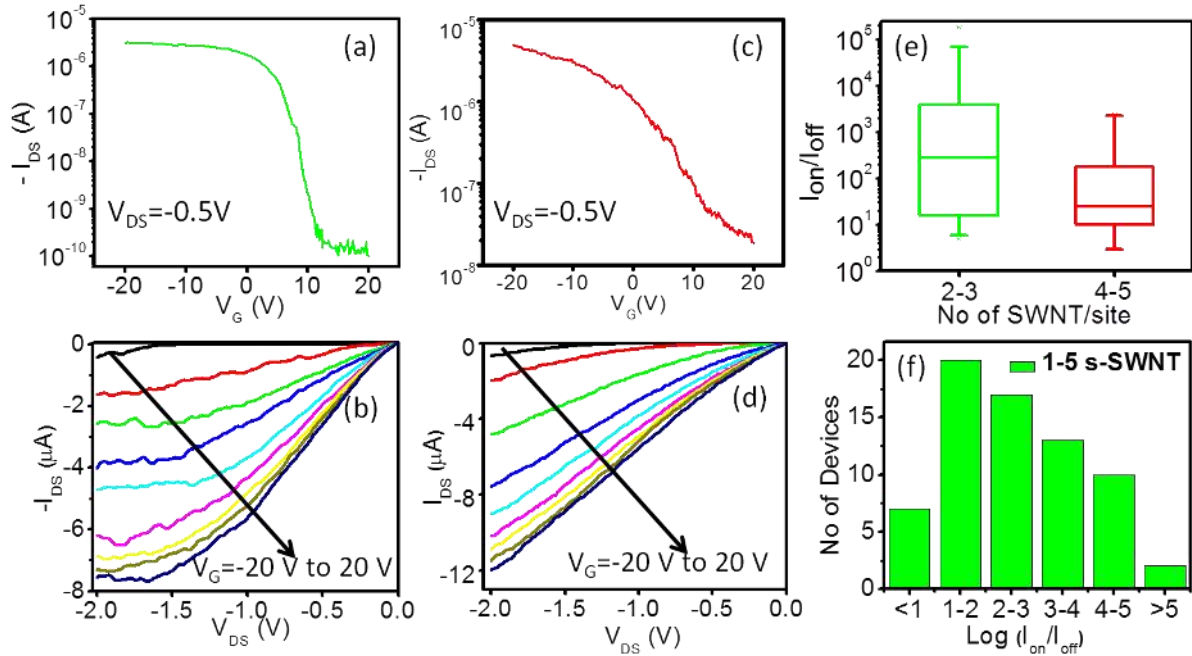


Figure 4.8 (a) Transfer characteristics of a FET device with 2 s-SWNT. (b) output characteristics of the same device for different gate voltages ranging from +20 V to -20 V. (c) Transfer and (d) and output characteristics of a device with 4 s-SWNT. (e) Box plot of I_{on}/I_{off} for 2-3 and 4-5 s-SWNT showing the range and median value. (f) Histogram of the I_{on}/I_{off} for all devices with 1-5 s-SWNT obtained from 20 sec assembly.

When there are more than 1 SWNTs per site, the chances of getting one larger diameter SWNT per site increases. Since the total I_{on}/I_{off} is limited by the SWNT with lower I_{on}/I_{off} , the overall I_{on}/I_{off} of the device decreases. In addition, when the number of SWNT per site increases, the inter-tube spacing decreases. If this spacing is lower than the gate oxide (SiO_2) thickness of 250 nm, the gate voltage may be screened causing an incomplete depletion of charge carriers with gate voltage resulting in lower I_{on}/I_{off} [44-45]. Figure 4.8(f) represent an overall summary of the I_{on}/I_{off} of all the s-SWNT with 1 to 5 s-SWNT per site resulting from 20 sec DEP assembly.

From here, we see that out of 69 devices measured, 62 show on-off ratio greater than 10 giving a 90% FET yield. Similar to individual SWNT a large device-to-device variation is observed for 1-5 SWNT devices. Narrowing the distribution of diameters and chirality may facilitate more homogeneous device behavior [41-42] and future effort should be directed in improved sorting of s-SWNTs by diameter. Such device to device variation may help explain many interesting behavior observed in semiconducting rich nanotube networks and arrays [23, 43]

4.4.2 Electron transport measurements of 1-10 SWNT devices

Transport properties were also studied for the devices assembled with a DEP time of 35 sec containing 1-10 s-SWNTs with an assembly yield of 100%. Figure 4.9(a) shows the transfer characteristics of a device with 6 s-SWNT. This device has an I_{on}/I_{off} of only 20.

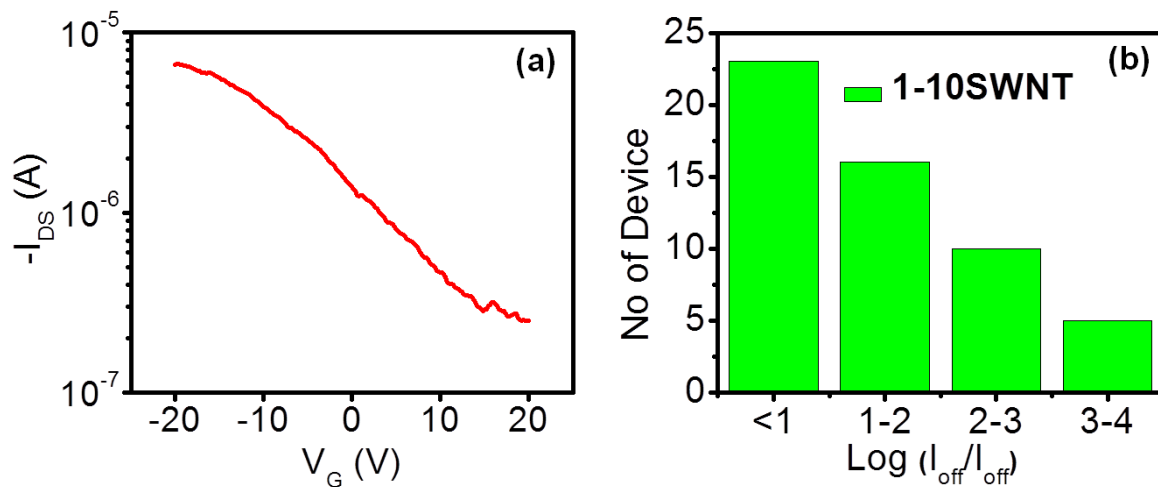


Figure 4.9 (a) Transfer characteristics of a representative FET device with 6 s-SWNT. (b) Histogram of the I_{on}/I_{off} for device with 1-10 s-SWNT devices.

A very high on conductance of $\sim 7\mu S$ is observed which is expected as the on current is the sum of the on current of individual SWNT. The devices consisting of 8-10 s-SWNT shows almost

metallic behavior and no FET performance was observed. Figure 4.9(b) shows the histogram of I_{on}/I_{off} determined from the transport measurement of 54 devices. Only 59% of the devices show FET behavior, a significant decrease compared to 1-5 s-SWNT devices.

We used a total of 504 electrode pairs used in this study for different DEP assembly time and we perform electron transport measurements on 186 devices. A higher FET yield (97%) is obtained with 1-3 s-SWNT per site using low DEP time (5 sec), but this leave almost two third of the electrode pairs empty. Whereas using higher DEP time (35 sec) it is possible to obtain 100% assembly yield, however, with a FET yield of 59%. Higher assembly yield (90%) with high FET yield (90%) can be obtained using an intermediate DEP time of 20 sec, where the device consist of 1-5 s-SWNT per site. This study provides not only the optimum DEP parameter but also the maximum number of s-SWNT per site to obtain high FET yield. The previous reports of the optimization showed 50% assembly yield with ~67% of those showing FET behavior [6]. In comparison, our 90% FET yield with 90% assembly yield is a large improvement and by far the best value reported to date. We note that if the FET is defined with $I_{on}/I_{off} > 3$ the corresponding FET yield is 99%, 94% and 73% for 5, 20 and 35 sec assembly respectively.

4.5 Conclusion

In summary, we demonstrate large scale assembly of individual SWNT using solution processed SWNT. By optimizing the DEP parameters it is possible to tune the number of SWNT in the channel. Individual SWNT devices show excellent transport properties. We also demonstrated a general route for the high yield fabrication of FET using AC dielectrophoresis of

semiconducting enriched s-SWNT solution. A 90% FET yield together with 90% assembly yield can be achieved using all s-SWNT. Higher assembly yield (~100%) was demonstrated by optimizing the number of s-SWNT between the channels. Variation of FET performance with the number of s-SWNT has also been observed.. This large-scale parallel fabrication technique using all semiconducting carbon nanotube will provide a roadmap to pave the way for future SWNT based nanoelectronic devices.

4.6 References

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CHAPTER 5: TOWARDS PARALLEL FABRICATION OF SINGLE ELECTRON TRANSISTOR USING TOP METAL CONTACT OF CARBON NANOTUBE

5.1 Introduction

The rapid miniaturization of the Si-Metal Oxide Semiconductor Field Effect Transistor (Si-MOSFET) and its integration into electronic circuits has posed several challenges in achieving the overreaching goals of Moore's law. If the current trend of miniaturization of Si transistor has to continue, the device size will hit sub-5 nm scale in a decade or so.² Not only that the fabrication of sub-5 nm device by current top down technology will be extremely challenging but also the operation of such a device will not be based on diffusive transport. This is due to the fact that as the device size becomes smaller, the self capacitance C (proportional to the dimension) of the device also becomes smaller. Therefore, there is a finite energy cost of $U_C = e^2/C$ (called charging energy) for placing an additional electron into the device. This energy is inversely proportional to the size of the device and can become significant in nanoscale devices. Consequently such a device will operate quantum mechanically via single electron tunneling. A device in which single electron tunneling is controlled by one electron at a time is called single electron transistor (SET). The observation of SET behavior require that (i) the electron addition energy must be greater than the thermal energy ($U_C > k_B T$) and (ii) the tunnel resistances are sufficiently high ($R \gg h/e^2$), so that quantum fluctuations are insignificant and the electrons are localized in the island. Since the U_C is inversely proportional to the C and C is proportional to the size of the dot, the charging energy is bigger for smaller sized dots.

It has been suggested that the quantum effect that leads to SET behavior can be advantageous in electronic device applications as it offers very low power consumption and high switching speed two major problems faced by the current CMOS technology. As a result, SET is considered to be a potential candidate for the post CMOS era quantum electronic device applications including ultrasensitive sensors, memory and quantum information processing. However, the fabrication of SET based devices is still at its infancy. SET was first demonstrated in aluminum tunnel junction by Fulton and Dolan about three decades ago. Since then SET has been realized in several material systems and device geometries including lithographic defined dot in GaAs/AlGaAs heterojunction, metallic grain, etching of Si, nanoparticles, nanowires and nanotubes.³⁻³⁹ However, most of these devices are fabricated to study fundamental physics related to the QD and are difficult to reproduce either due to the complex fabrication processes or challenges in integration of the nanoscale island in a reliable way. For example, lithography defined dots in GaAs/AlGaAs heterojunction are quite large. Such device operates only at ultra-low temperature. Besides, the complicated steps involved in device fabrication makes it hard to control the charging energy. It is possible to obtain high temperature (100 K) operating reproducible SET by using metallic grains and colloidal nanocrystals. However, fabrication of such devices is very challenging due to the difficulty in placement in nanosized gaps, hence leading to extremely low device yield. Fabrication of SET using SWNT has also been demonstrated, for example, by bending the SWNT using atomic force microscopy (AFM) tip. However, AFM manipulation is time consuming and reproducibility of the same sized device can be challenging. As a result, a viable technique for the scaled up fabrication of SET is yet to be demonstrated which is necessary for the practical applications of SET based devices.

In this chapter, I will present an approach for the scalable fabrication of SWNT SET. The approach is based on the integration of solution processed individual SWNTs between the pre-fabricated metal electrodes via DEP followed by deposition of metal contact to create 100 nm SWNT devices. We have exploited the fact that a metal contact with SWNT creates a Schottky barrier at the metal-SWNT interface and can act as tunnel barriers to define a QD [15, 24-26]. I performed low temperature (4.2K) transport measurements for 50 devices. I found that majority of the devices with $R_T > 100 \text{ K}\Omega$ show SET behavior. Periodic, well-defined Coulomb diamonds with a charging energy $\sim 15 \text{ meV}$ was observed for the devices with $100 \text{ K}\Omega < R_T < 1 \text{ M}\Omega$, representing single quantum dot (QD) behavior while multiple QDs behaviors with charging energy up to 200 meV were observed for devices with high $R_T (> 1 \text{ M}\Omega)$. A total of 38 devices showed SET behavior giving an overall yield of 76%. The approach presented here is a significant step forward for the scaled up fabrication of SET and practical application of SET based devices.

5.2 Device design and sample preparation

The devices were fabricated on heavily doped Si substrates with a 250 nm-capped layer of SiO_2 . Optical lithography was used to define the larger contact pads with position alignment markers and evaporation of 3 nm chromium (Cr) and 42 nm gold (Au) and of source drain electrode pair with separation 1 μm were defined by electron beam lithography (EBL). We used tapered shaped electrodes to maximize the individual SWNT assembly yield. In order to obtain sharp tip I used single layer resist as increased thickness of the resist flattened the edge of electrode. Following EBL, 3 nm Cr and 25 nm Au were deposited by evaporation followed by lift off in acetone. The channel length between the electrodes were kept fixed at 1 μm , since the

median length of the SWNT used were 1.4 μm , this channel length would give the highest yield[27]. Fabrication of SET using top contact involves two major steps: Assembly of individual SWNT and Fabrication of top contact on the assembled SWNT. In the next sub section I will discussed the details of those fabrication steps.

5.2.1 Dielectrophoretic assembly of individual SWNT

Integration of individual SWNT is one of the major and most important parts of SET fabrication. Presence of a straight, single SWNT is the key requirement to fabricate SWNT SET. Even though bundle of SWNT show SET operation, because of the larger diameter of the bundle it requires very low temperature for the operation of SET[6]. The channel between source and drain need to be free from any additional smaller SWNT in the channel. Presence of additional small SWNT in the channel can act as memory node and affect the charge transport of the SET[28, 29] . Besides bending can create defects in the SWNT and act as tunnel barrier and can also take part in the transport [11, 30]. Integration of individual SWNT is one of the major and most difficult parts of SET fabrication.

As discussed in previous chapter 2, DEP allows precise positioning of individual SWNT at the desired position of the circuit. High yield assembly of SWNT has been demonstrated using the DEP parameters. Proper choice of those parameters strongly affects the assembly yield. Those parameters need to be optimized for every set of electrode design, solvent used. The choices of parameters are strongly influenced by the thickness of SiO_2 , separation of electrodes, presence of surfactant. Again for a particular set of devices some parameters has strong effect on the assembly of individual SWNT than the others. For example a shorter DEP time is required

for trapping individual SWNT, unless it can increase the number of SWNT in the channel. Besides the SWNT need to be uniformly dispersed in the solution. Because the presence of bundle of SWNT make their way to the channel as they experienced greater DEP force compared to the single one. Also the solution need to be free from catalytic particle as the catalytic particle are attracted by the DEP force and make their way inside the channel together with the SWNT. Presence of catalytic particle can severely degrade the performance of SET.

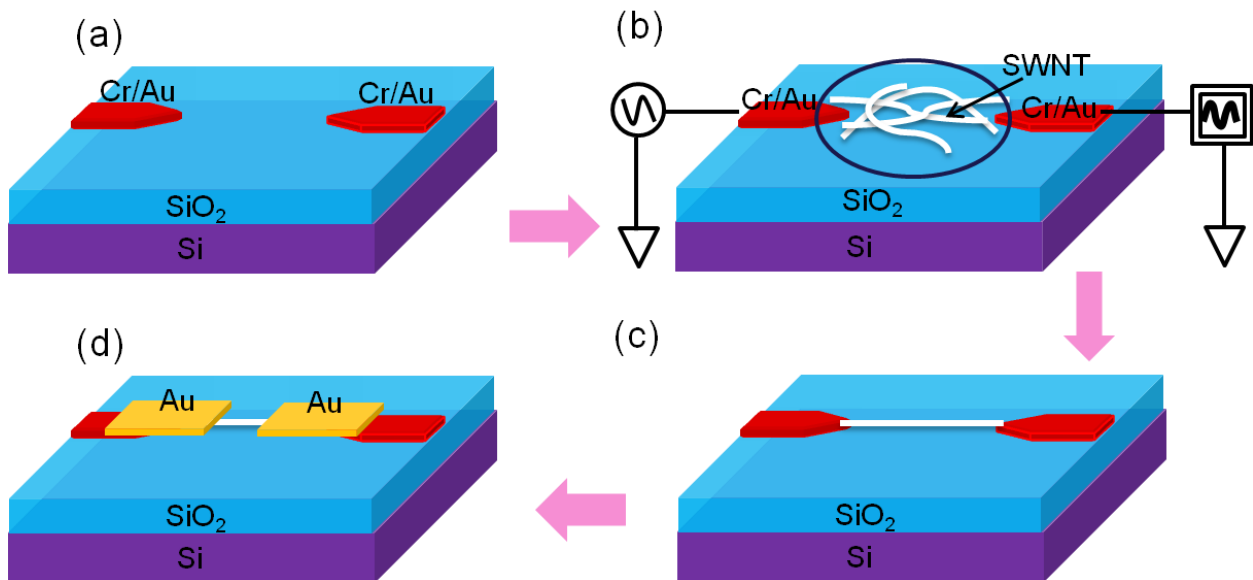


Figure 5.1 Three-dimensional illustration of the device fabrication steps: (a) Source and drain electrode pattern (b) DEP assembly set up. (c) Individual SWNT assembled between electrodes. (d) Fabrication of top electrode contact on individual SWNT.

For the assembly of individual SWNT we used a stable, surfactant free commercially available solution obtained from Brewer Science [32]. The average diameter of the SWNTs in the solution was ~ 1.7 nm as determined by atomic force microscopy (AFM) and having a median length of ~ 2 μm [33]. The concentration of SWNT's in the mother solution is ~ 50 $\mu\text{g/ml}$

with a shelf life of 6 month. For the assembly, the concentration of SWNTs was diluted to ~10 ng/ml using DI water. A small drop (2-3 μL) of solution was cast onto the chip immediately after the preparation of the solution. One of the easiest ways to optimize the parameter for the high yield assembly of individual SWNT is to vary one of the parameters and keeping the remaining DEP parameters constant. Here I will vary the DEP time. I vary the DEP time only and keep all the other parameters constant. To optimization of DEP time for individual SWNT, I varied the DEP time and check the assembly. Three different time 5 sec, 10 sec, and 20 sec was used for the assembly. The cartoon for the DEP aseembly set up is shown in Fig 5.1 (a). It is seen that for the 10 sec DEP assembly, an average ~ 23% of the electrode pairs were bridged by individual SWNT, similar deposition yield was reported by other research groups [25, 34, 35]. For the successful deposition cases, mostly a single SWNT was present in channel, without having any short SWNT connected to the electrodes. This is desirable for the fabrication of SET because the presence of a short SWNT in channel acts as a memory node and affects the transport.

5.2.2 Deposition of metal contact on individual SWNT

While making the top contact on SWNT we consider several factors. Structural defects and disorders are commonly observed in SWNT with a scattering length of ~ 100 nm [36-38]. Those defects can act as a tunnel barrier and break a long SWNT into a series of QD which can be avoided by using small channel length of SWNT for the device. Besides, smaller QD have higher charging energy and thus can perform at elevated temperature. That is why we set the separation

between the two electrodes smaller ~ 100 nm. To define the metal top contact we perform a second layer of EBL. After developing, 25 nm Au was deposited by e-beam evaporation.

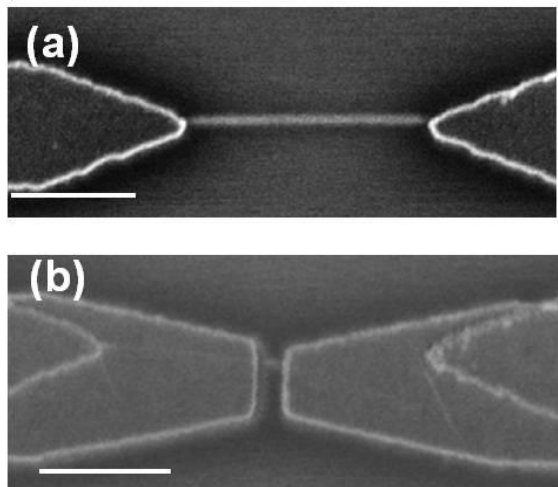


Figure 5.2 (a) SEM image of (a) aligned SWNT between electrode with a separation of $1 \mu\text{m}$ and (b) top contact device with 100 nm separation. Scale bar: 500 nm

Figure 5.2 shows an SEM image of a representative device before (a) and after (b) top contact. After fabrication, the top-contact devices were annealed in Ar/H_2 gas mixture (1:3ratio) at 200°C for one and half hour.

5.3 Room temperature electron transport properties

The room temperature transport measurement of the devices was carried out in a probe station. Figure 5.3 shows a cartoon of room temperature measurement set up for top contact devices. A 95% electrical characterization yield was achieved for the top contact devices. We measured a total of 50 individual SWNT top contact devices. Figure 5.4 (a) shows the histogram of resistance measurements for all top contact SWNT devices. A large variation in the room temperature resistance (from $22 \text{ K}\Omega$ to $50 \text{ M}\Omega$) was observed for the top contact SWNT devices.

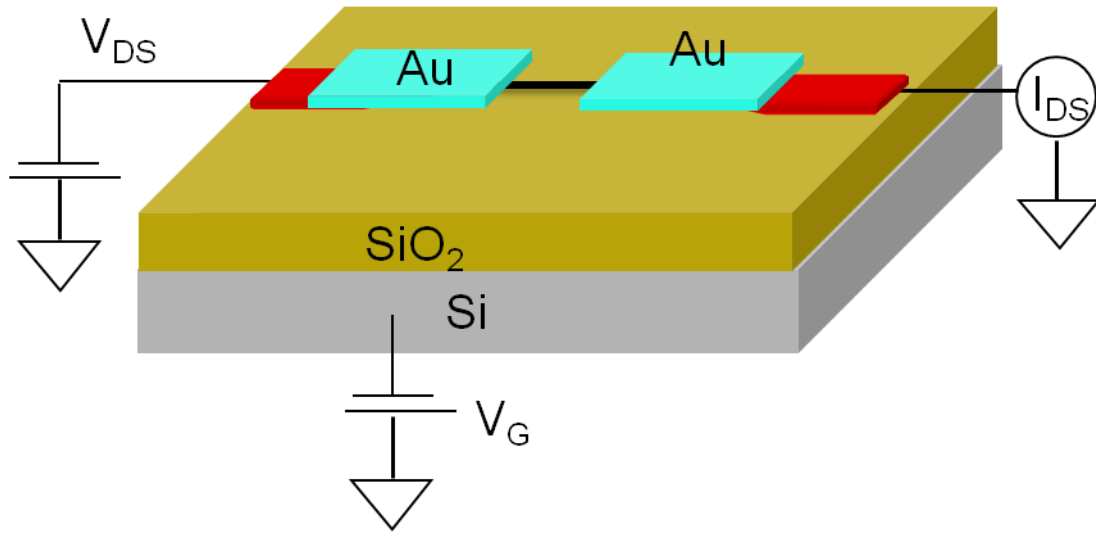


Figure 5.3 Schematic diagram of top contact SWNT device geometry and measurement setup showing a SWNT between Pd top contacts.

These wide ranges of variation in room temperature resistance can be attributed to the difference in diameter, and chirality of the assembled SWNT together with the variation in contact area between SWNT and metal electrodes [39-41]. It is generally observed that the devices made of SWNT with higher diameters give smaller resistance compared to that with smaller diameter because of larger contact area[39].

After reducing the channel length to 100 nm, we measured their room temperature transport properties such as current (I_{DS}) vs bias voltage (V_{DS}) and I_{DS} vs gate voltage (V_G) characteristics. From the I - V_G curve, it was observed that about ~ 60% of the devices show semiconducting behavior with $I_{on}/I_{off} > 10$. Rest of the devices showed metallic behavior, a little change or no change of current with back gate voltage. From the I - V curve, we found that the contact resistance of the devices. Figure 5.4 (a) shows the histogram of resistance for top contact SWNT devices. A e variation in the room temperature resistance from 22 K Ω to 50 M Ω was observed for the top contact SWNT devices.

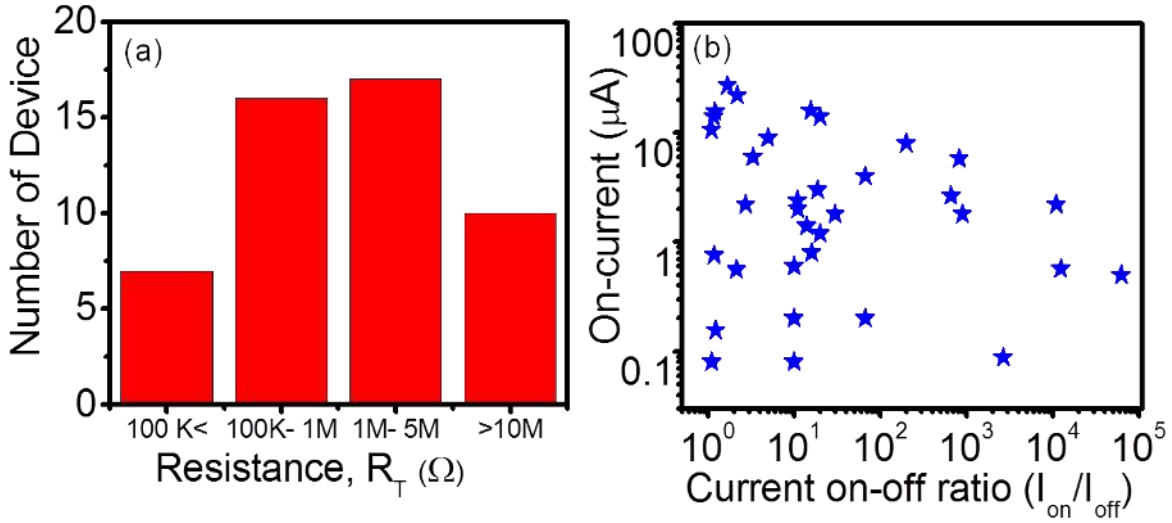


Figure 5.4 (a) Histogram of the contact resistance for top contact SWNT devices after annealing. (b) Current on-off ratio and on-current of the top contact devices at room temperature.

Transport characteristics, I_{DS} vs V_G was measured to find out the electronic type of the SWNT. The highly doped Si was used as a back gate. Of all the top contact devices, on an average ~60% show semiconducting behavior with $I_{on}/I_{off} > 10$. 30% of the devices show metallic behavior and no change was observed when back gate voltage was applied. Rest of the devices shows little variation in current with back gate voltage indicating small band gap devices[42]. Figure 5.4 (b) shows a histogram of the on-off ratio of the top-contact SWNT devices. The maximum on-off ratio obtained for the top contact devices was 4×10^4 . Such variations may be explained by the differences in chirality and diameter from tube to tube; these physical features affect the band gap and contact resistance of the s-SWNT, and in turn, on-off current ratio of each device.

5.4 Low temperature electron transport measurement of top contact device

We studied the transport properties of 50 devices. Below I will discuss the low temperature transport properties of three representative devices having low (device A), medium (device B), and high (device C) contact resistance.

5.4.1 Electron transport measurement of Device A

Figure 5.5 shows electron transport properties of a representative sample (device A) with a low contact resistance of $\sim 26 \text{ K}\Omega$ ($\sim h/e^2$) determined from the I_{DS} - V_{DS} curve at $V_G = 0 \text{ V}$ (Fig 5.5(a)). Figure 5.5(b) shows the transfer characteristics ($I - V_G$) measured at a fixed $V_{DS} = 100 \text{ mV}$. The device shows negligible change in I_{DS} with V_G , indicating a metallic SWNT. The I_{DS} - V_{DS} curve with $V_G = 0 \text{ V}$ measured at 4.2 K is shown in Figure 5.5(c). Although a small non-linearity in the I_{DS} vs V_{DS} curve was observed near zero bias, no current suppression (representative of CB) was observed. Figure 5.5(d) shows I_{DS} vs V_G at a $V_{DS} = 10 \text{ mV}$ measured at 4.2 K . No current oscillations, hallmark of SET behavior, were observed at this temperature. This is expected since the contact resistance is not large enough to form a tunnel barrier at the metal-SWNT interface. As a result, a QD is not formed in the SWNT, hence no SET.

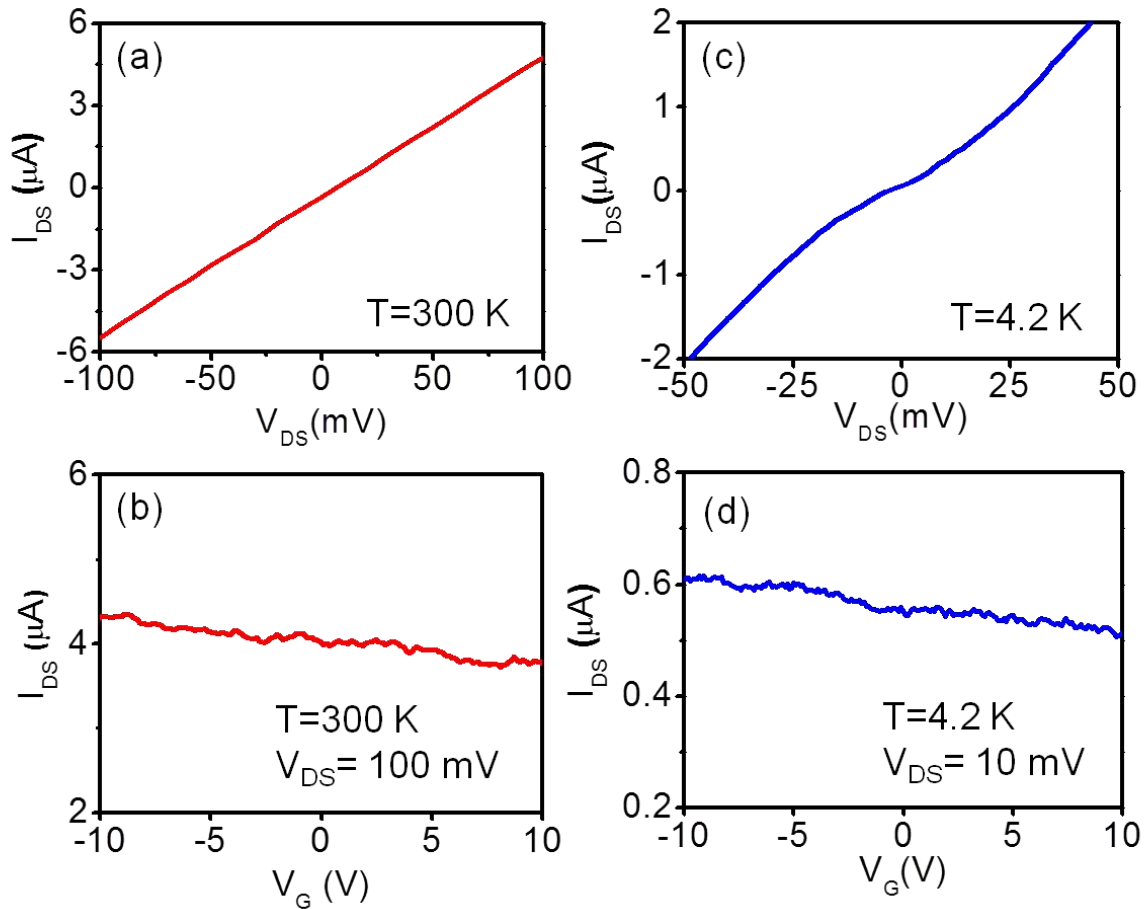


Figure 5.5 Electron transport characteristics of devices A. I_{DS} - V_{DS} curve (a), and I_{DS} - V_G (at $V_{DS} = 100\text{ mV}$) curve of the device at room temperature; (c) I - V_{DS} curve of the device at 4.2 K does not show coulomb oscillation. (b) I - V_G curve of the device and Coulomb oscillation is not observed.

5.4.2 Electron transport measurement of Device B

Figure 5.6 shows the room temperature transport measurements of another sample B. The contact resistance of the device was found to $500\text{ K}\Omega$ ($\sim 19\text{ h}/e^2$) from the I_{DS} - V_{DS} curve of figure 5.6 (a). Figure 5.6 (b) shows the transfer characteristics of the device at a fixed $V_{DS}=100\text{ mV}$. The I_{DS} decreased by several orders of magnitude with increasing V_G , demonstrating a p-type FET behavior.

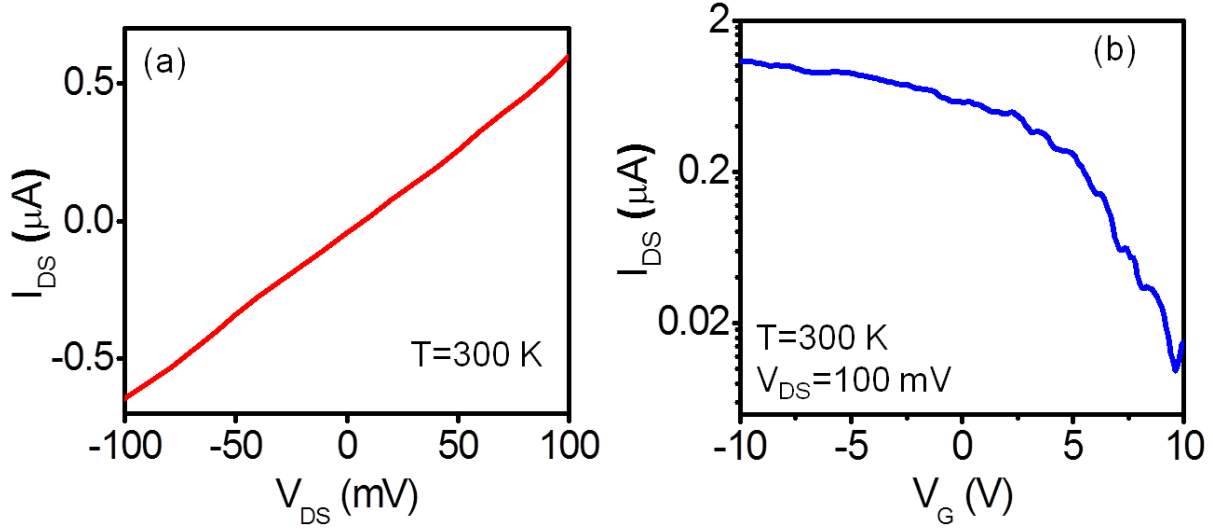


Figure 5.6 Room temperature electron transport characteristics of devices B: I_{DS} - V_{DS} curve (a), and I_{DS} - V_G (at $V_{DS} = 100\text{ mV}$).

The low temperature ($T = 4.2\text{ K}$) electron transport measurements of the device are presented in figure 5.7. Figure 5.7 (a) is a plot of I_{DS} of the device at $V_G = 0\text{ V}$ and $V_G = 0.05\text{ V}$. For $V_G = 0\text{ V}$ the current is blocked and Coulomb blockade is observed in bias voltage range of from -15 meV to 15 meV . The Coulomb blockade is lifted by applying $V_G = 0.05\text{ V}$. Figure 5.7(b) shows a plot of I_{DS} vs V_G for a fixed $V_{DS} = 2\text{ mV}$. Current oscillations are observed while sweeping the V_G , typical of SET behavior,⁴⁸ suggesting that QD has formed in the SWNT channel. Figure 5.7 (c) shows expanded zoomed in view of current oscillation for the selected part of Fig. 3(d) in $-1\text{ V} < V_G < 2\text{ V}$. Within this range, regular and periodic current oscillations were observed with a period of $\Delta V_G \sim 100\text{ meV}$, which indicates presence of single QD in the SWNT channel.

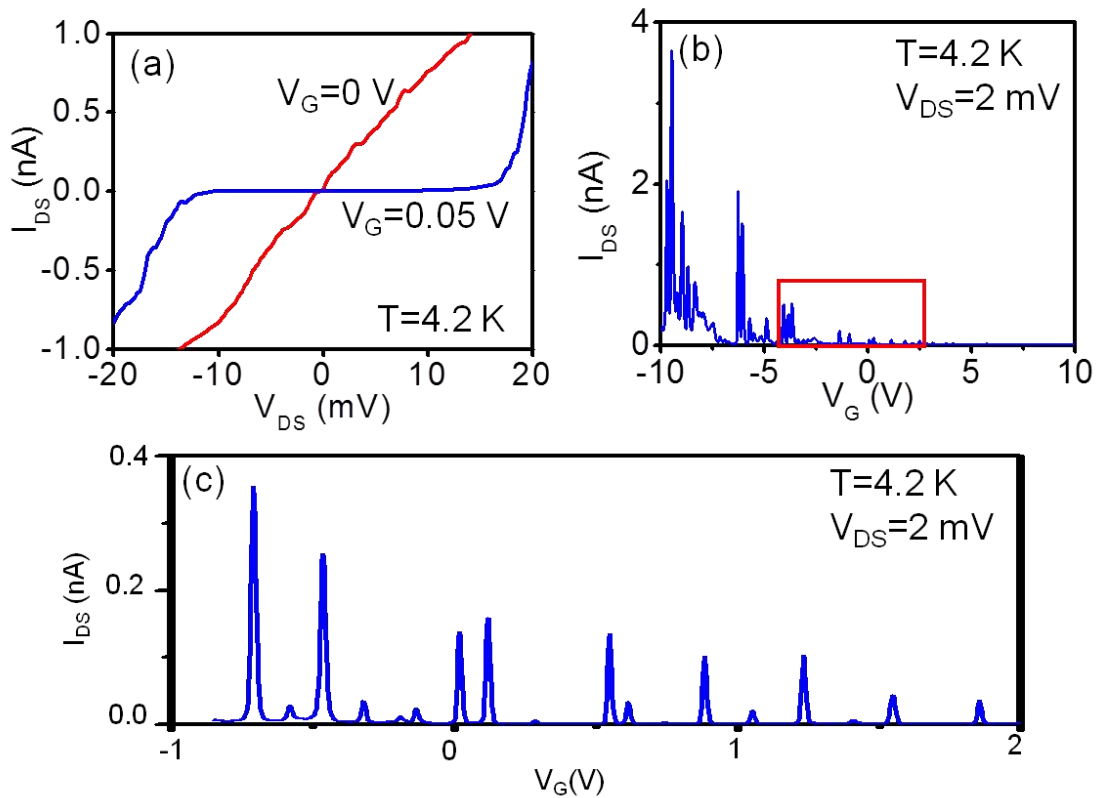


Figure 5.7 Electron transport properties of device B at $T=4.2$ K. (a) $I_{DS}-V_{DS}$ at two different gate voltages at $T=4.2$ K, showing coulomb blockade and single electron tunnelling (b) $I_{DS}-V_G$ curve of the device at 4.2 K at $V_{DS} = 2$ mV showing coulomb oscillation. (c) Expanded view of the $I-V_G$ curve showing periodic oscillations..

Figure 5.8(a) display a color scale plot where differential conductance (dI/dV_{DS}), plotted by sweeping both V_{DS} and V_G , often called stability plot, taken at $T = 4.2$ K. The bright region signifies high conductance, whereas the dark region represent coulomb blockade. The bright region indicates high conductance, whereas the dark region indicates Coulomb blockade. Throughout the plot, a series of diamond shaped regions (often called Coulomb diamond) were observed. The diamonds are almost equidistant with a period of ~ 100 mV. The diamonds closing at $0V$ (V_{DS}) having constant slopes over the entire range of V_G indicates the presence of a single QD [7].

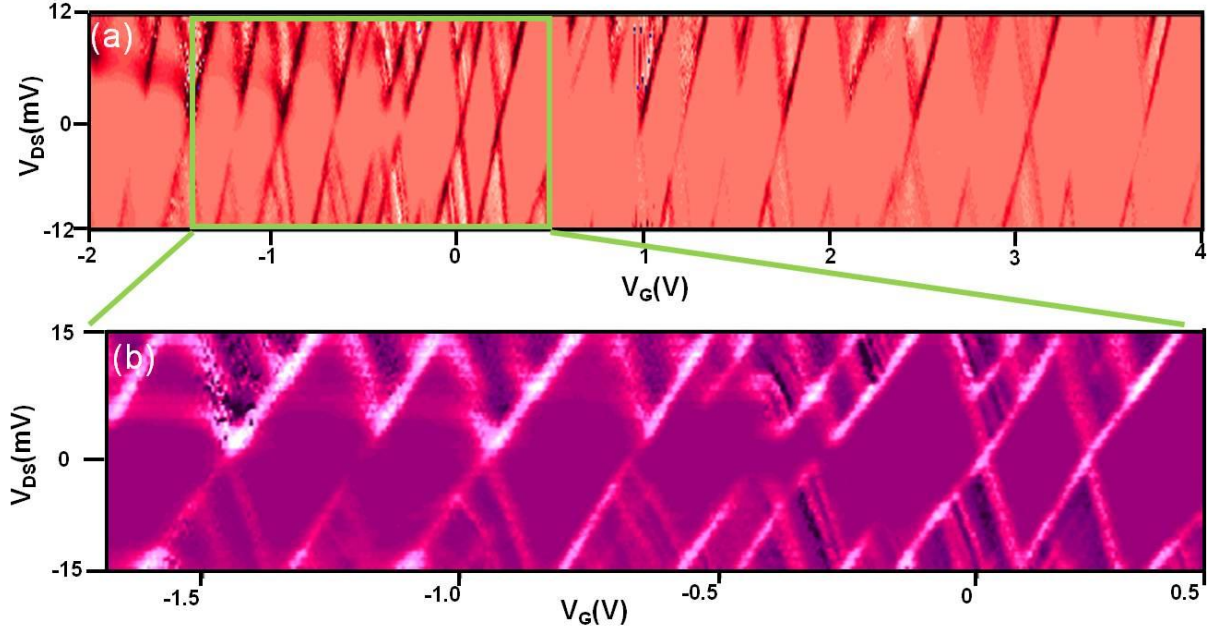


Figure 5.8 (a) Color scale plot of differential conductance (dI/dV_{DS}) as a function of V_G and V_{DS} at $T=4.2$ K, showing regular diamond patterns. (b) Expanded view of the Coulomb diamond showing single QD behavior with excited energy level.

To further investigate the SET parameters we plot $dI_{DS}/dV_{DS}-V_{DS}-V_G$ at higher resolution as shown in Fig. 5.8 (b). The plot exhibit well defined peaks in dI_{DS}/dV_{DS} in addition to the single electron tunneling appears as lines parallel to the diamond edge corresponding to the single particle energy level spacing ΔE . By analyzing the data we obtain average values ΔE for first few levels of ~ 5 meV. This values agrees reasonably well with the ΔE estimated using dispersion relation $\Delta E \sim 0.5eV/L(\text{nm})$ [6, 43], which is 5 meV for a 100 nm QD. The height of the diamond is a direct measure of charging energy (U_C) yields, $U_C \sim 15$ meV.

The capacitance values of the SET can be calculated from the Coulomb diamond using constant interaction model[44]. The gate capacitance is calculated from the period ($\Delta V_G \sim 250$ mV) between the diamonds using the formula $C_G = e/\Delta V_G$ which yields $C_G \sim 1.6$ aF. The source and drain capacitances is calculated from the positive slope $\alpha_1 = -C_G/C_1$ and negative slope $\alpha_2 = C_G/(C_1 + C_2)$ of the diamond respectively, which yield $C_1 \sim 2$ aF and $C_2 \sim 8.1$ aF. The total capacitance of the SET is $C_\Sigma = C_1 + C_2 + C_G = 11.7$ aF which can be used to calculate the charging energy of $U_C = e^2/C_\Sigma \sim 13.6$ meV similar to the value measured directly from the height of the diamond in this regime. For SWNT we can measure the size of the QD from the U_C using the formula $U_C = 1.4$ eV/L (nm), where L is the length the SWNT QD in nm[43]. From here, we obtained L= 93 nm which matches with the separation between the electrodes (100 nm). One important thing need to mention here is that this low temperature spectroscopy data resembles presence of a very clean quantum dot. This also signifies that no defects are induced in the SWNT during the fabrication steps.

Figure 5.9 shows temperature dependent plot of I_{DS} - V_{BG} for the single QD at fixed value of $V_{DS} = 2$ mV. It can be seen that as the temperature is elavated, the peaks become flat and can not be observed at all at 120K. The charging energy of the QD can be determined from the temperature dependent data using the formula, $U_c = K_B T$. For T= 120 K, $U_c \sim 10$ meV which is close to the charging energy obtained from the stability plot. Low temperature transport measurements were performed on 28 top contact devices with resistance in the region II, out of them 24 devices showed single QD behavior with charging energy between 10-20 meV. Among

the rest of the devices, QD behavior was not observed for three devices, and one device shows multiple QD behavior.

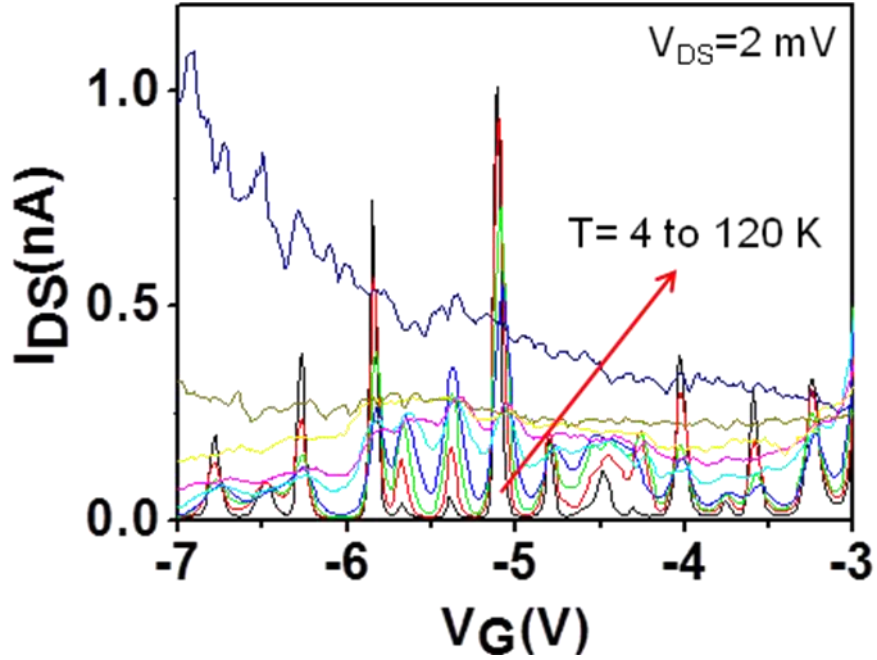


Figure 5.9 Plot of I_{DS} - V_G for $V_{DS} = 2$ mV at various temperatures from 4.2 up to 120 K.

5.4.3 Electron transport measurement of Device C

Figures 5.10 demonstrated the electron transport properties of device C. The I_{DS} vs V_{DS} graph at $V_G=0$ V is presented in Fig 5.10(a) giving a room temperature resistance of ~ 2 M Ω , Fig 5.10(b). The I_{DS} vs V_G curve is plotted in Fig. 2 (f) represents a p-type semiconducting behavior with current on-off ratio ~ 120 .

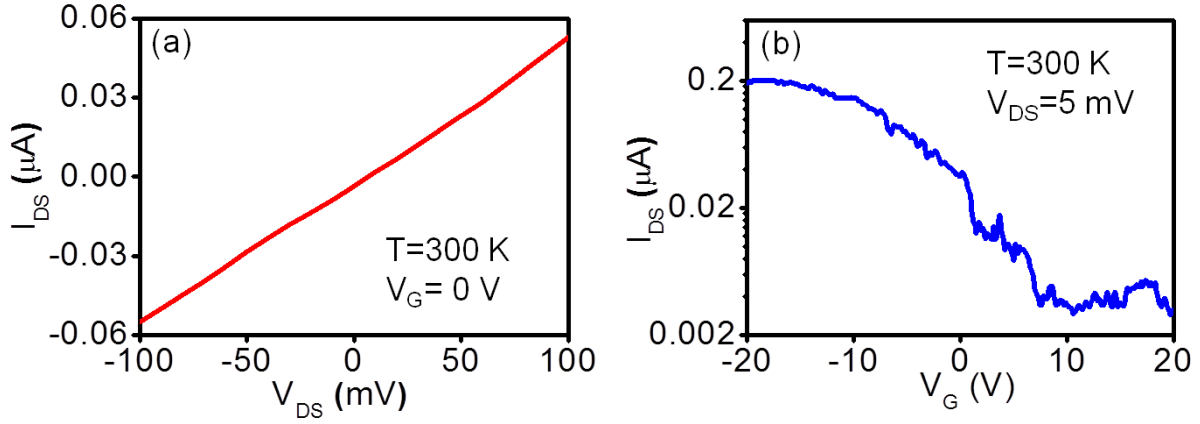


Figure 5.10 Room temperature electron transport characteristics of devices C: I_{DS} - V_{DS} curve (a), and I_{DS} - V_G (at $V_{DS} = 100$ mV) curve of the device at room temperature.

Figure 5.11 demonstrate the low temperature transport measurements of the device. Figure 5.11(a) shows I_{DS} vs V_G graph at $T=4.2$ K with a fixed $V_{DS} = 100$ mV. Same as regime II, current oscillations are also observed while sweeping the V_G . However, the oscillations are not periodic in V_G . The stability plot is shown in Figure 5.11(b). Several irregular Coulomb diamonds with different height is shown. In addition, the diamonds are not closing and the slopes of the diamonds are different for different diamond. The irregular current oscillations and Coulomb diamonds are characteristics of SET having multiple QDs.³⁹ The multiple QDs resemble presence of defects or disorder in SWNT.^{49, 50} The U_C of the device varies from 20 to 30 meV. From the U_C , the size of the QD is found to be varied between 40-70 nm. For this device, some additional defects are present in the SWNT in addition to the tunnel barrier created at metal-SWNT interface.

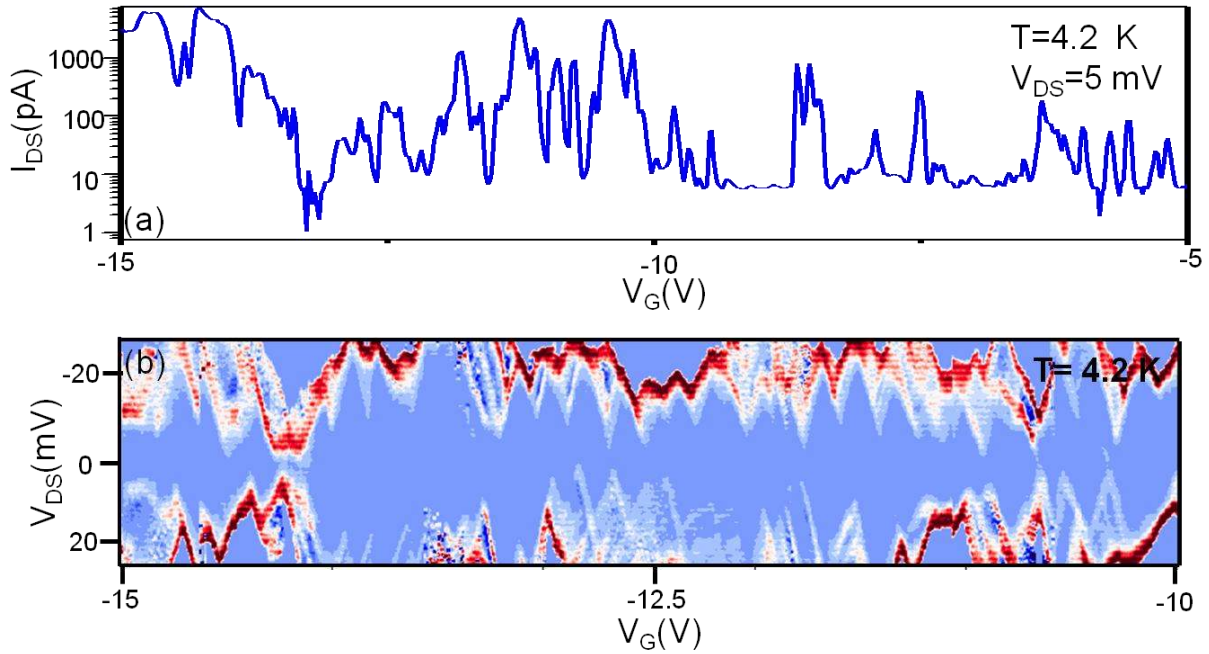


Figure 5.11 Electron transport characteristics of device C at $T=4.2$ K. (a) $I-V_G$ curve of the device at 4.2 K at $V_{DS} = 5$ mV showing irregular coulomb oscillation. (b) dI/dV_{DS} plotted as a function of V_G and V_{DS} showing irregular diamond patterns characteristics of multiple QDs.

This is a well known phenomenon in semiconducting SWNT as they are more prone to structural disorder, defects than metallic one. Presence of defects in SWNT also increases the R_T of the device [1]. Those defects or disorder acts as tunnel barrier and breaks the individual SWNT into a number of QD in series resulting in multiple QD behavior at low temperature transport. Out of 11 devices measured in this range, 10 devices show multiple QDs behavior.

5.5 Discussion and Summary

In order to analyze the electrical properties of the SWNT devices, we can categorized them into three groups based on their room temperature resistance. A total of ten devices with $R_T < 100$ K Ω (range I) were measured at 4.2K and only one of them shows coulomb oscillations.

Low temperature electron transport measurements were performed on 28 devices with $100 \text{ k}\Omega < R_T < 1 \text{ M}\Omega$ (range *II*) while 24 devices show single QD behavior with U_C varies between 10-20 meV. For the rest of the devices, multiple QD behavior was observed for one device and three devices did not show any QD transport. Out of 12 devices measured with $R_T > 1 \text{ M}\Omega$ (range *III*), 11 devices showed such multiple QDs behavior.

A summary of the variation of charging energy for the 100 nm contact devices with room temperature resistance is shown in figure 5.12. From the electron transport measurements of 50 top contact devices we can conclude that QD is not formed for the devices with $R_T < 100 \text{ k}\Omega$. Most (~90%) of the devices with R_T in the range *II* shows single QD behavior with consistent charging energy ($\sim 15 \pm 5 \text{ meV}$). Multiple QD behavior with high charging energy (between 10-200 meV) is observed for the devices with R_T in the range *III*.

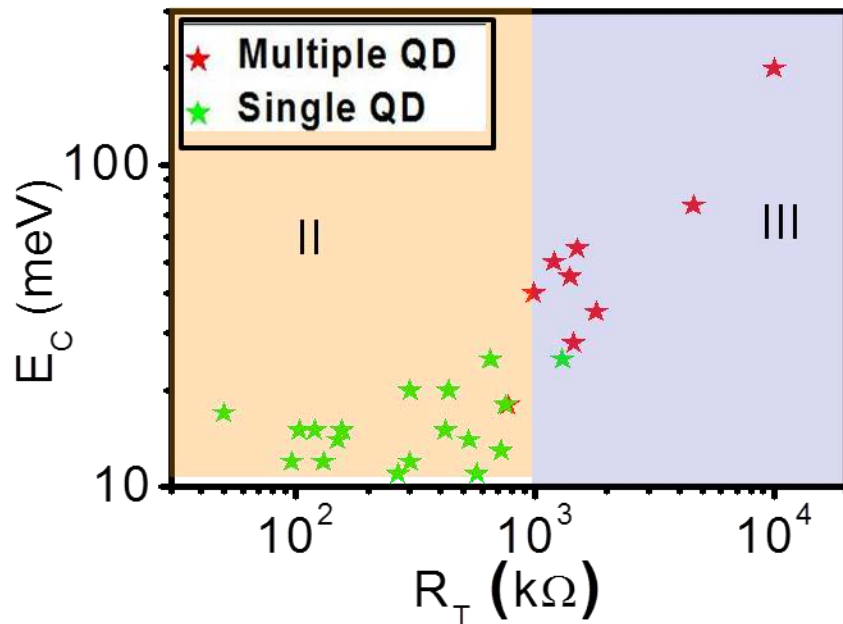


Figure 5.12 Summary of the devices at three different resistance ranges. Inset of the figure shows the possible model for the observed behavior of SWNT in distinct regime.

For the device in range *II* one can expect a clean SWNT and tunnel barrier is formed at the SWNT-metal interface giving relatively higher R_T . The devices in this region are semiconducting or small diameter metallic one. Due to the higher curvature, and chemical reactivity of those SWNT are greatly perturbed by the contacting metal [39]. This can give rise to a defect at or near the metal-SWNT interface which act as tunnel barrier[45]. SWNT confined by two such tunnel barrier acts as single QD.

Again for the device in range *III*, in addition to the tunnel barrier created at metal-SWNT interface, there might have some additional defects present in the SWNT. This is a common phenomenon in semiconducting SWNT as they are more prone to structural disorder, defects than metallic one. Presence of defects in SWNT increases the R_T of the device. Those defects or disorder acts as tunnel barrier and breaks the individual SWNT into a number of QD in series resulting in multiple QD behavior at low temperature transport.

Table 5.1 The SET behavior of 100 nm top contact devices at different room temperature resistance (R_T) ranges

Range	# of devices	Single QD	Multiple QD
<i>I</i>	10	1	N/A
<i>II</i>	28	24	1
<i>III</i>	12	1	11

Table 5.1 summarizes result obtained from the low temperature transport of 50 devices used in this study. From here it is found that ~75% of the devices shows SET behavior giving an

overall 18% yield for SET. One important thing to note here is that 86% of the devices in range *II* give single QD SET behavior. This implies that large-scale assembly of SWNT SET made of single QD is possible by fabricating devices with R_T in range *II*.

5.6 Conclusion

In conclusion, a scalable, CMOS-compatible technique for the fabrication of SWNT based SET has been demonstrated. The devices were fabricated by the directed assembly of individual SWNT via DEP followed by metal top contact and the electron transport properties of the fabricated devices were investigated. We showed that 75% of the top contact SWNT devices give SET performance. A correlation between SET behavior and the room temperature resistance (R_T) of the devices was observed. It was found that the devices with *I*) $R_T < 100 \text{ K}\Omega$ does not show SET behavior, *II*) $100 \text{ K}\Omega < R_T < 1 \text{ M}\Omega$ show single QD behavior, and *III*) $R_T > 1 \text{ M}\Omega$ show multiple QD behavior. This easy and simple fabrication process will provides a much desired insight towards the large scale fabrication of SWNT SET

5.7 References

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CHAPTER 6: PARALLEL FABRICATION OF SINGLE ELECTRON TRANSISTOR USING MECHANICAL TEMPLATING OF CARBON NANOTUBE

6.1 Introduction

Single walled carbon nanotubes (SWNTs) have been considered to be a promising building block for the creation of QD for SETs because of their extraordinary electronic properties, extremely small diameter along with unique one dimensional nature[1-8]. Controllable and reproducible fabrication of SWNT based SET using SWNT requires formation of tunnel barriers at desired positions along the nanotubes so that charges can be confined in a quantum dot defined by the tunnel barriers. Metal contact induced Schottky barrier have been used to define SWNT based SET[2, 9-12]. However, the fabrication of SET using this technique is a “hit or miss” and controllability has yet to be demonstrated. In SWNT tunnel barrier can be formed by bending it [4, 13, 14]. SET had been fabricated by forming two bend at SWNT using AFM tip [4, 14]. However, in this technique it is very difficult to control the size of the QD and and is not give reproducible SET fabrication technique.

In order to create more controllable and reproducible SETs, our group has recently introduced a simple technique to bend SWNT by placing it on top of a local Al/Al₂O₃ gate between the source and drain contact which is demonstrated in fig 6.1 (a)[15]. The local Al/Al₂O₃ gate act as a “mechanical template” and it was hypothesized that SWNT bent by the local gate due to van der Waals force between the tube and substrate and the bent act as tunnel barrier. As a result, a QD with size equal to the width of the local gate is created. Besides, the

local bottom gate tunes the operation of the SET. This indicates that tunnel barriers to the SWNT using this scheme can be advantageous over other techniques because of its simplicity of design and compatibility with large scale fabrication.

However, in the previous proof-of concept demonstration, random deposition techniques had been used to assemble the SWNT to make the mechanical template SET. In random deposition technique, chance of integrating an individual SWNT depends on luck, which is not appropriate for scalable integration of SWNT based device. Selectively depositing SWNT onto prefabricated electrodes by dielectrophoresis (DEP) can circumvents this difficulty. DEP is a directed assembly technique in which parallel large-scale assembly of SWNT is facilitated by capacitively coupling the drain electrodes to the gate electrodes separated by an insulating oxide layer.

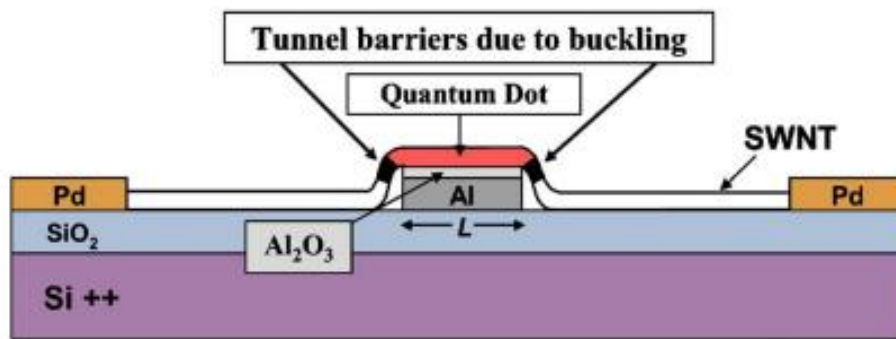


Figure 6.1 Schematic diagram of mechanical template based SWNT SET device [15]. Tunnel barriers are created at the edge of the local gate and the size of the quantum dot is equal to the width of the mechanical template.

Even though mechanical template technique is successful in making tunnel barrier in metallic SWNT nevertheless for controllable fabrication of SET it is necessary to address several issues. One of which is to find out the suitable electronic type of SWNT for the mechanical

template. SWNT is formed by rolling graphene sheet into the form of a cylinder. Depending on the direction of folding, carbon nanotube shows different electronic properties known as chirality which determined the electronic type of SWNT i.e. metallic (m-SWNT) or semiconducting (s-SWNT). Besides the optical, and mechanical properties of SWNT are also depends on its chirality [16-18]. For large scale fabrication of SET using mechanical template technique we have to know, what type of SWNT is suitable for template technique or in other words the chirality dependence on the tunnel barrier formation by the mechanical template. It was speculated that tunnel barrier is formed due to bending caused by the Van der Waals force acting between the surface and the SWNT at the edge of the local gate [19]. Theoretical studies show that highly symmetric m-SWNT is less susceptible to the scattering compared to the semiconducting carbon nanotube upon bending [20, 21]. Also upon bending the conductance of m-SWNT remains almost constant whereas the conductivity of s-SWNT changes significantly [20, 22]. The exact reason for this has not been well understood but all the theoretical results show that upon deformation only a little change occurs in metallic SWNT. Therefore, we can expect that the bending induced deformation will be much more in s-SWNT or in other words in s-SWNT tunnel barrier would be more easily formed than metallic one upon mechanical template. In this work, we will verify this hypothesis and figure out the electronic type of the SWNT suitable for mechanical template.

In this chapter we present the parallel fabrication of SWNT-SET using mechanical template technique mechanisms for the tunnel barrier formation. We will also figure out the effect of electronic type on the creation of tunnel barrier by mechanical templating. We fabricate devices

using a mixed SWNT solution containing both m-SWNT and s-SWNT. We investigate the low temperature (down to 4 K) transport for both m- and s-SWNT devices.

6.2 Design and fabrication of mechanical template devices

Figure 6.2 shows schematic diagram of different steps for the fabrication of mechanical template SWNT-SET. I use a Si substrate with a 250 nm SiO₂ layer for the fabrication of SET. Cr/Au (5 nm/45 nm) was metalized for larger contact pad was defined by photolithography. I used Cr/Pd (2 nm/23 nm) for source and drain electrode. The channel length was kept fixed at 1 μm. I use electron beam lithography (EBL) to define the smaller size metal electrodes. After EBL the pattern was developed in (1: 3) methyl isobutyl ketone : isopropyl alcohol (MIBK : IPA). Then I perform metallization by e-beam evaporation and lift-off. I used tapered shaped electrodes as it increases individual SWNT assembly yield. A second EBL was then performed to define a mechanical template between the metal electrodes. The width of the template was 100 nm and 25 Al was deposited by e-beam evaporation to define the local gate. During the Al deposition, the sample stage was cooled with liquid nitrogen to minimize the surface roughness of the Al.[28] Finally, the sample was placed inside a oxygen plasma chamber and treat it for 12-15 minutes which will create an aluminum oxide (Al₂O₃) layer of thickness 3-4 nm on top of Al.

Directed integration of individual SWNT between the taper shaped electrode was done via dielectrophoresis (DEP) using a high quality aqueous solution. A stable, surfactant free solution with a concentration of SWNT's ~ 50 μg/ml was obtained from Brewer Science.[40] The average diameter of the SWNTs in the solution was ~ 1.7 nm obtained from atomic force microscopy (AFM) measurements. For DEP assembly, the concentration of the original solution

was diluted to ~ 10 ng/ml using DI water. Few μL of prepared solution was then placed on the chip and an electric field of 5 V was then created between common source and gate electrodes for three minutes (Figure 6.2 (c)). As the drain electrodes experience the same voltage as the gate since they are capacitively connected. This leads to an electric field between the metal electrodes and the SWNTs are trapped (Figure 6.2 (d)).

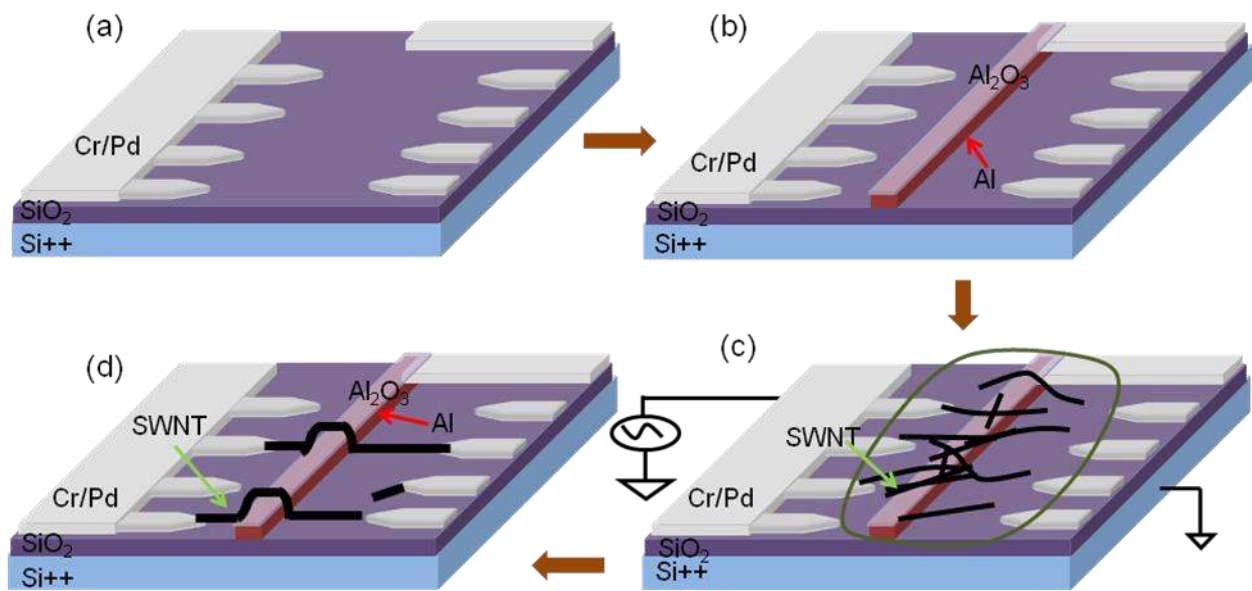


Figure 6.2 Fabrication of SWNT SET using mechanical template technique. (a) Source - drain electrodes with a separation of 1 μm . (b) Mechanical template is defined by EBL and few nm Al₂O₃ is formed by oxygen plasma treatment. (c) DEP assembly of SWNT by simultaneous deposition. (d) After DEP a number of devices assembled on the same chip.

After DEP assembly, the result for individual assembly was examined by a Zeiss Ultra 55 field emission SEM. A total of 312 electrode pairs in 13 chips were tested. Out of them 67 electrodes were found to be bridged by individual SWNT. This gives an average device assembly yield of $\sim 21\%$. For the unsuccessful assembly case, no SWNT were observed between electrodes, small SWNT connected to only one electrode, or multiple SWNT connected to the electrodes. Since fabrication of SWNT requires a single SWNT to be bridged between the

electrodes, here we focus on devices containing individual SWNT. Figure 6.3 shows the SEM image of several single SWNT integrated between the metal electrodes and on top of the local gate. After DEP assembly, the local-gated devices were annealed at 200° C for one and half hour in a gas mix of Ar/H₂ (1:3ratio) to reduce the contact resistance. Then the devices were connected in a chip carrier and placed in a ⁴He cryostat for studying .

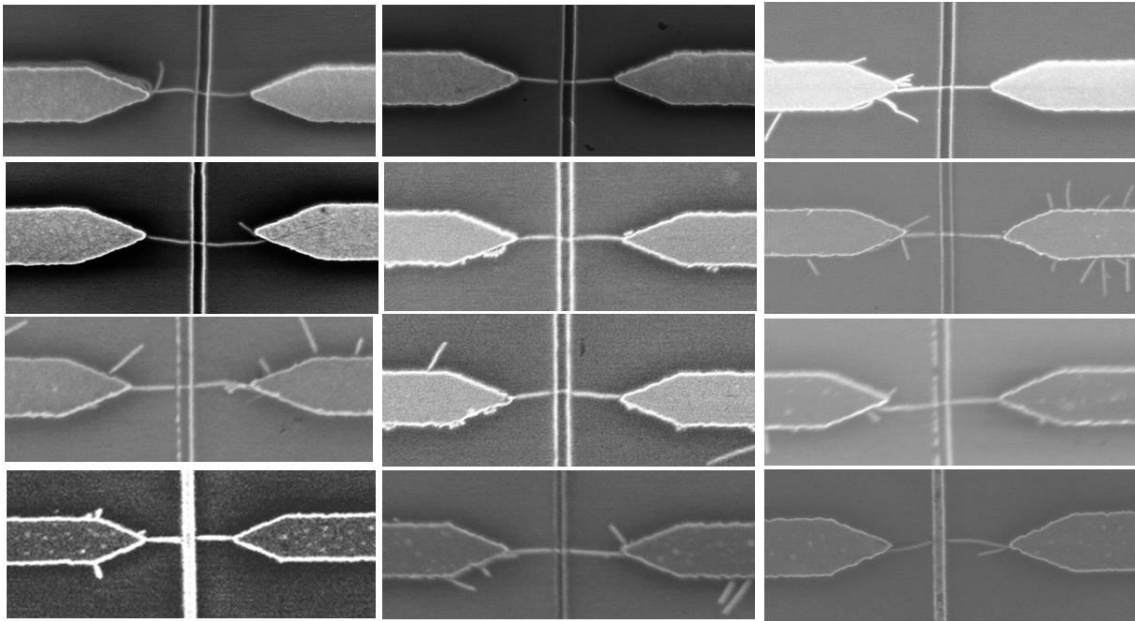


Figure 6.3 Scanning electron micrographs (SEM) image of mechanically templated individual SWNT devices deposited by dielectrophoresis (DEP). Distance between adjacent electrodes is 1 μm.

6.3 Room temperature transport of mechanical template devices

The room temperature electrical measurements of the mechanical template devices were performed in using the setup described in chapter 3. Figure 6.4 (a) delineates the setup for

transport study where we use the Al/Al₂O₃ mechanical template as a local gate. I have studied 65 mechanical templated devices.

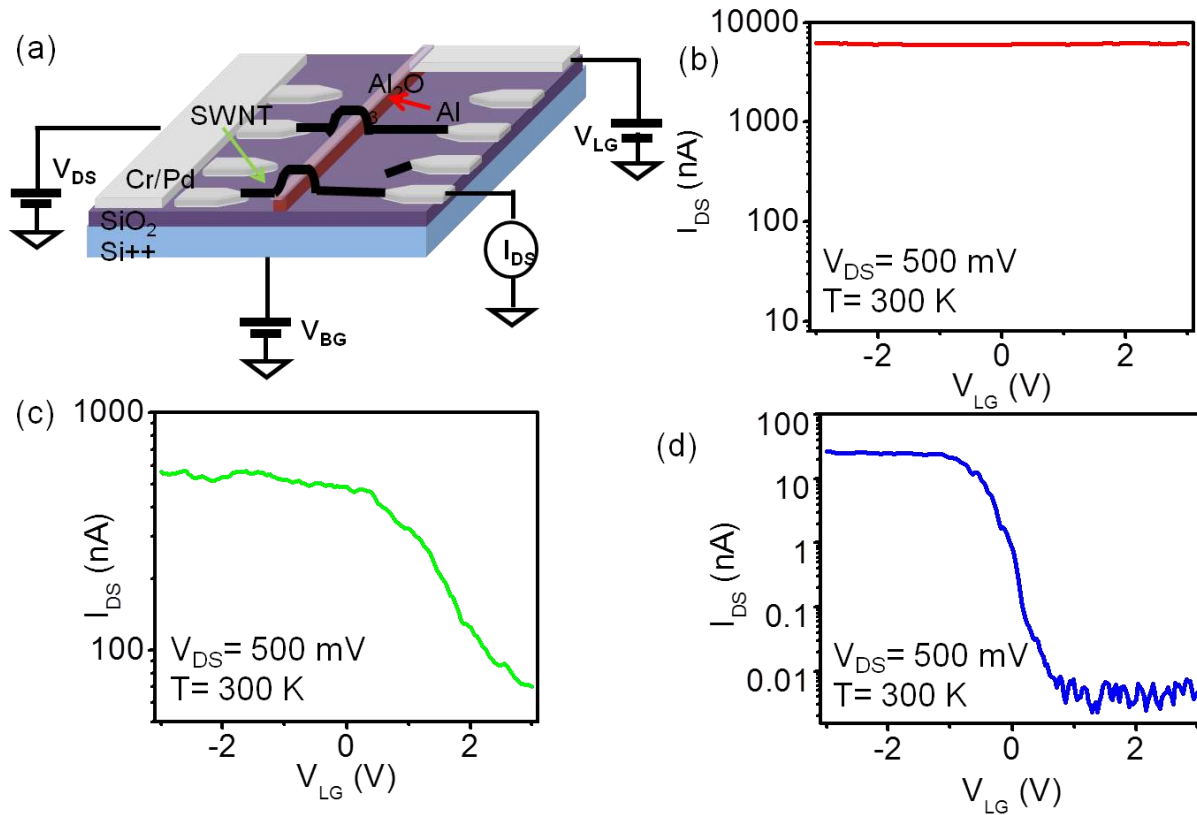


Figure 6.4 Schematic diagram of measurement setup for mechanical template local gated device. Current (I_{DS}) versus local gate voltage (V_{LG}) at $V_{DS} = 0.5$ V of representative (b) metallic, (c) small band-gap, and (d) semiconducting device.

The resistances of the devices were measured from I_{DS} - V_{DS} measurements at $V_G=0$ V and it varies from 50 k Ω to 100 M Ω . This value of contact resistance matches with that of the DEP assembled SWNT devices measured by other groups. Figure 6.4 (b) represents the drain current (I_{DS}) vs local gate voltage (V_{LG}) of typical metallic device for constant bias voltage ($V_{DS} = 0.5$ V). It was observed that the current does not vary while sweeping the local gate voltage. The transport characteristic of a typical semiconducting SWNT (s-SWNTs) device is presented in figure 6.4

(b). It gives a current on-off ratio (I_{on}/I_{off}) ~ 11500 . Approximately 50% of the devices show metallic or semi-metallic behavior with I_{on}/I_{off} less than one order of magnitude and 50% of the devices show semiconducting behavior with I_{on}/I_{off} greater than 10. Figure 6.5 shows comparison between the performance of local-gated and back-gated device. I measured the bias current (I_{DS}) for a device as a function of back gate and local gate. For back gate measurement switching behavior is obtained for sweeping large back voltage (20 V) while for local gate it is obtained for a much smaller voltage sweep (6V). A slower switching speed is obtained for the back-gated operation. The subthreshold swing ($d \log I_{DS} / dV_G$) a measure of device speed calculated for back-gated operation is ~ 1000 mV/dec. Whereas local-gated operation gives much faster switching speed which is ~ 300 mV/dec. Thin gate oxide (2-3 nm) used in local bottom gate in contrast to the back gate (250 nm) resulting in faster switching speed.

6.4 Effect of electronic structure on the low temperature transport spectroscopy:

It has already been reported by couple of papers published by our group proving that tunnel barrier is created in the SWNT at the edge of the local gate [15]. However several issues still need to be resolved: 1) there remaining an open question whether mechanical templating favors any particular electronic type of SWNT or in other words whether the m-SWNTs or s-SWNT will work efficiently with the mechanical template 2) large scale fabrication of SWNT SET using this method was not demonstrated. In this section I will address those issues. I will discuss the low temperature transport of m-SWNT, and s-SWNT mechanical templates devices assembled by dielectrophoresis.

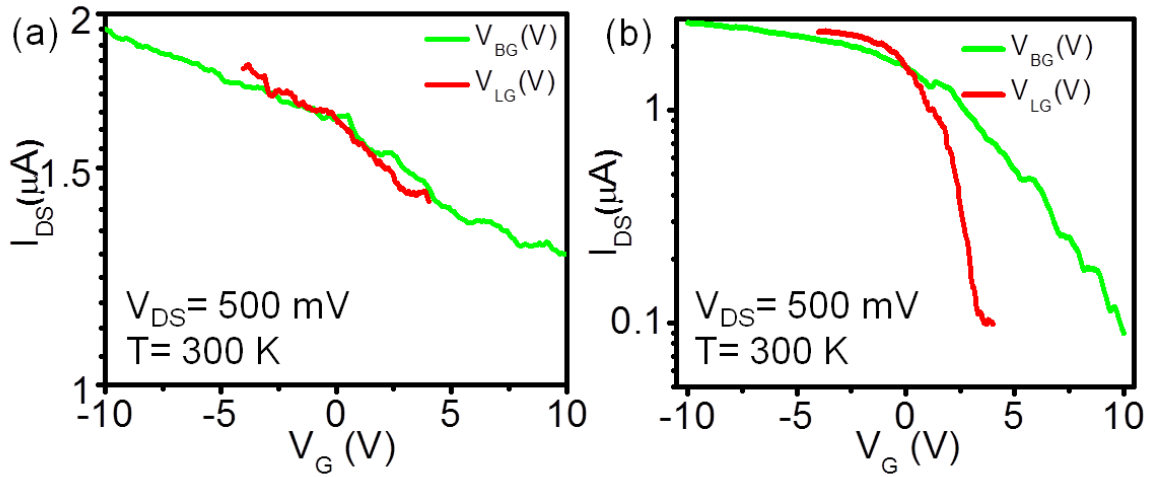


Figure 6.5 Comparison in device performance between the local gated and back gated device. (a) metallic SWNT, and (b) semiconducting SWNT. $V_{DS} = 0.5$ V for both curves.

6.4.1 Low temperature transport of mechanical template metallic SWNT

Figure 5.6 (a) shows I_{DS} plotted by sweeping the (V_{BG}) between -10 V to +10 V at low temperature ($T = 4.2$ K). Current oscillation is observed while modulating the back gate voltage over the entire range of V_{BG} which signifies SET behavior. Figure 5.6 (b) shows a color scale plot, where dI_{DS}/dV_{DS} is plotted while sweeping both V_{DS} and V_{BG} . A series of coulomb diamond is observed in the plot. All the diamonds are closed at $V_{DS} = 0$ V and have constant slope. This indicates the presence of a single QD in the mechanical template SWNT. The charging energy of the QD can be measured from height of the diamond and is found to be $U_C = 15$ meV. The size of the QD can be calculated from the charging energy using the formulae $U_C = 1.4$ eV/L (nm) which gives the size of the QD to be 95 nm. This size of QD is in close agreement with the width of the local gate. This observation suggests that a single QD is created due to the mechanical template induced tunnel barrier.

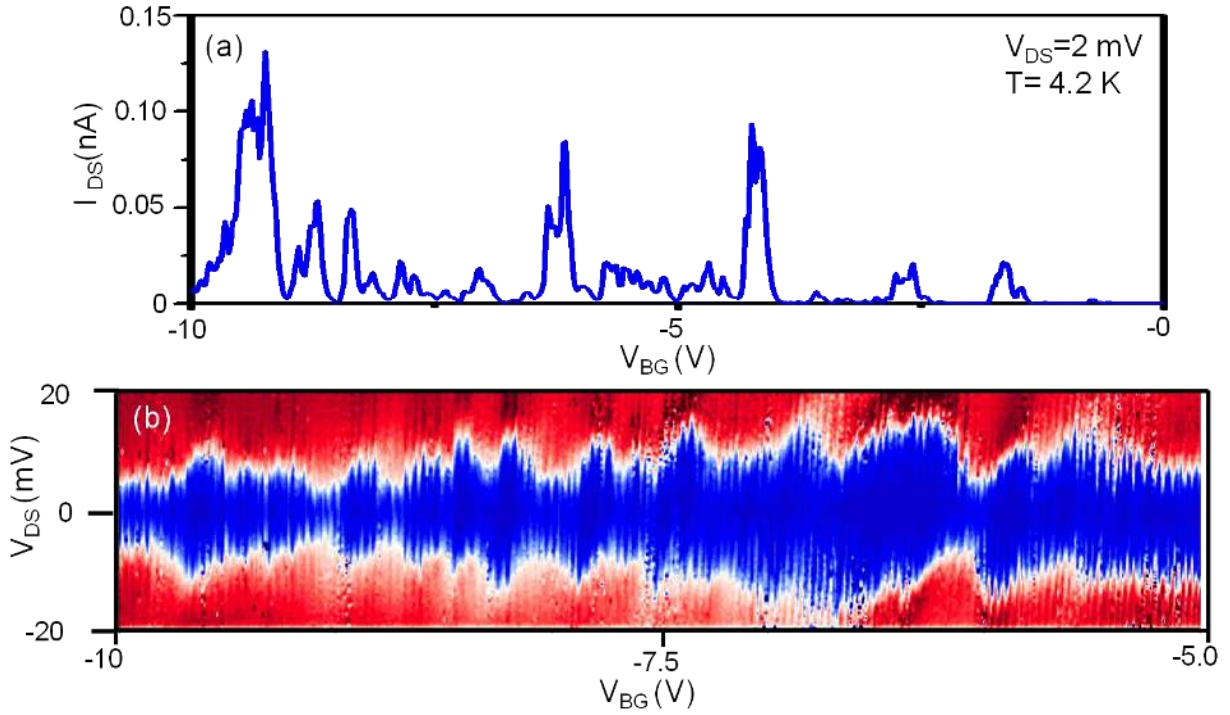


Figure 6.6 (a) I - V_{BG} curve of a metallic SWNT the device at 4.2 K at $V_{DS} = 2$ mV showing current oscillation, typical of a SET behavior (b) color scale plot, dI/dV_{DS} vs V_{BG} vs V_{DS} plotted at $T = 4.2$ K.

To confirm that the QD is created due to the mechanical template we will further investigate the low temperature measurements by applying the local gate voltage. Figure 6.7 (a) is a plot of I_{DS} versus V_{LG} at temperature, $T = 4.2$ K for a fixed $V_{DS} = 2$ mV. Semi-periodic current oscillations are observed as while sweeping V_{LG} , signifies the presence of a QD [12, 23].

Figure 6.7 shows the color scale plot of the device obtained by plotting the conductance by sweeping both bias voltage and local gate voltage. A number of regular diamond shaped regimes (Coulomb diamond), which are signature of SET are observed throughout the entire local gate voltage range. In order for a guide to the eye the diamonds are outlined by white dotted line. The diamonds are found to be equally spaced with $\Delta V_{LG} \sim 25$ mV. The diamonds

have constant slopes over the entire range of V_G and are closed at $V_{DS} = 0V$ indicates presence of a single QD in the channel[24].

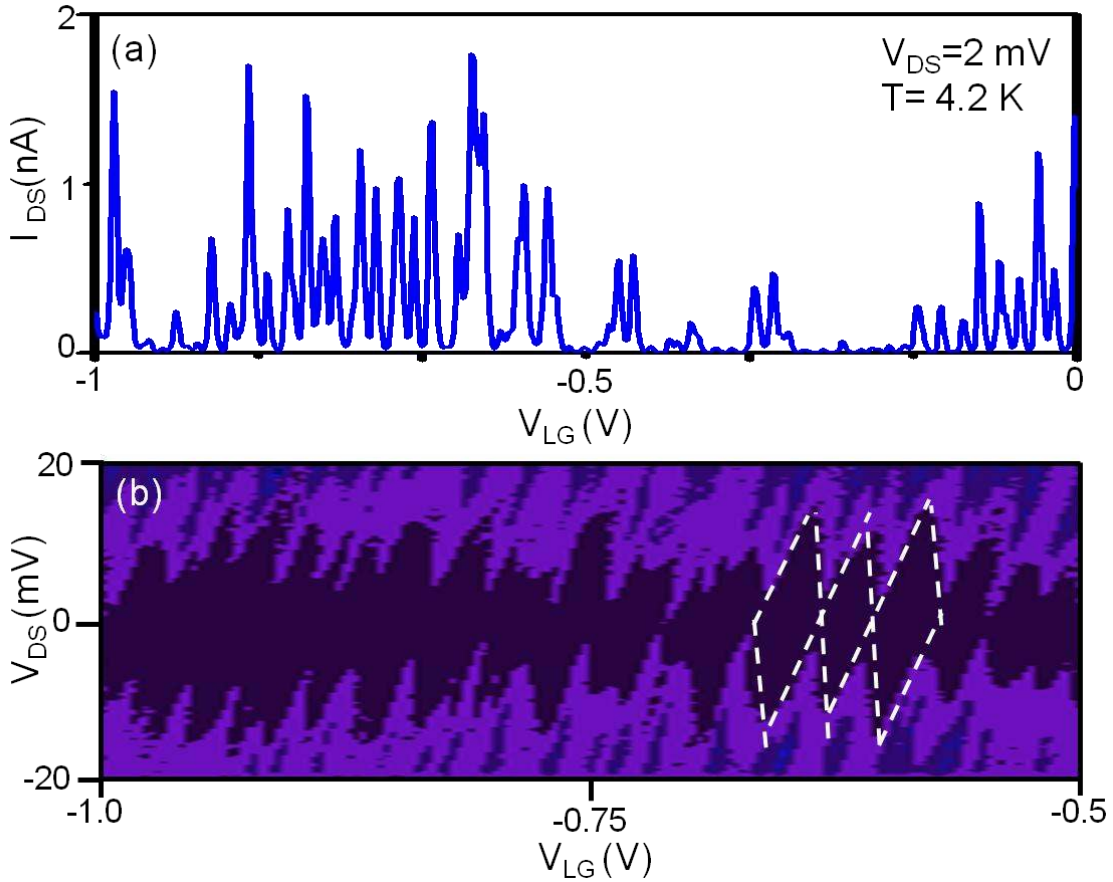


Figure 6.7 Low temperature electron transport properties of a representative mechanically templated metallic SWNT device (a) I_{DS} - V_G curve of the device at 4.2 K at $V_{DS} = 3$ mV showing periodic coulomb oscillation. (b) Color scale plot of dI_{DS}/dV_{DS} vs V_G vs V_{DS} at V_{LG} between -1.0V to -0.5 V $T= 4.2$ K.

The charging energy (U_c) of the QD can be measured directly from the height of the diamond and is found to be $U_c \sim 13$ meV. Using the constant interaction model[24], we can calculate the capacitance values of the SET. The gate capacitance is calculated using the formula, $C_G = e/\Delta V_G$, where ΔV_G is the period between the diamonds. The period of the

diamond, $\Delta V_G \sim 25$ mV obtained from the stability plot yields $C_G \sim 6.4$ aF. The source and drain capacitances can be calculated from the positive slope $\alpha_1 = -C_G/C_1$ and negative slope $\alpha_2 = C_G/(C_1 + C_2)$ of the diamond respectively, which yield $C_1 \sim 4.4$ aF and $C_2 \sim 3.4$ aF. The total capacitance of the QD is $C_\Sigma = C_1 + C_2 + C_G = 14.1$ aF. The charging energy of the SET can be obtained by using the relation $U_c = e^2/C_\Sigma$, yielding a charging energy which can be used to calculate the charging energy of $U_c \sim 12$ meV, which matches very closely with height of the diamond measured from stability diagram. For SWNT, the length of the QD can be obtained using the formula $U_c = 1.4 eV/L$ (nm), here L is length of SWNT QD in nm [2, 25]. From here, we obtained $L = 115$ nm as the size of the quantum dot which is in agreement with the width of the mechanical template.

Now it may be possible that the quantum dot is not created by the mechanical template instead by the random defects presents in the channel. In order to confirm that we compare the gate capacitance of the dot obtained from the charge transport spectroscopy with the theoretical value of the capacitance of the 100 nm SWNT section. To calculate the theoretical value we will use the cylinder-plane geometry and the capacitance is given by, $C_{LG} = 2\pi\epsilon_{avg}\epsilon_0 L / \cosh^{-1}(1+2t/d)$ with L and d being the length and diameter of SWNT, t is gate oxide thickness, ϵ_{avg} is the dielectric constant [7]. For dielectric film of thickness $t = 5$ nm, and SWNT of length $L = 100$ nm with diameter d between 1.5 nm to 3 nm the gate capacitance C_{LG} varies between 6.1 to 7.7 aF. This value matches with the experimentally obtained value of gate capacitance[15].

We have measured 16 other m-SWNT devices. Out of them, 11 devices show similar behavior with charging energy between 11 meV to 16 meV. The rest 5 device does not show any

coulomb blockade or coulomb oscillation at low T. The devices that does not give SET behavior had contact resistance in the range between 20K Ω to 100 K Ω . That means tunnel barriers are not created by mechanical template in those devices.

6.4.2 Low temperature transport of mechanical template semiconducting SWNT

A plot of I_{DS} versus at V_{LG} at T= 4.2 K for a fixed V_{DS} (= 2 mV) is presented in Fig. 5.8 (a). This s-SWNT also shows current oscillations while sweeping the gate voltage, indication of SET behavior [24]. Figure 5.8 (b) presents a plot of conductance dI_{DS}/dV_{DS} vs V_{DS} vs V_{LG} . Same as metallic SWNT a series of regular Coulomb diamond outlined by black dot, which are signature of SET are observed throughout the entire local gate voltage range. The Coulomb diamonds are equally spaced with $\Delta V_{LG} \sim 27$ mV. The diamonds have constant slopes over the entire range of V_G and are closed at 0V (V_{DS}) indicates presence of a single QD in the channel. We read off the charging energy (U_c) of the QD directly from the height of the diamond in the stability plot and is found to be $U_c \sim 15$ meV.

Using the constant interaction model [24], we calculate the different capacitance values of the SET. The gate capacitance is calculated from period of the diamond, $\Delta V_G \sim 27$ mV using the formula, $C_G = e/\Delta V_G$, yields $C_G \sim 6.3$ aF. The source and drain capacitances can be calculated from the positive slope $\alpha_1 = -C_G/C_1$ and negative slope $\alpha_2 = C_G/(C_1 + C_2)$ of the diamond respectively, which yield $C_1 \sim 0.3$ aF and $C_2 \sim 3.7$ aF. The total capacitance of the QD is $C_\Sigma = C_1 + C_2 + C_G = 10.3$ aF. Using the relation, $U_c = e^2/C_\Sigma$, the charging energy of the SET is found to be $U_c \sim 14.7$ meV, matches with the U_c obtained from the height of the diamond.

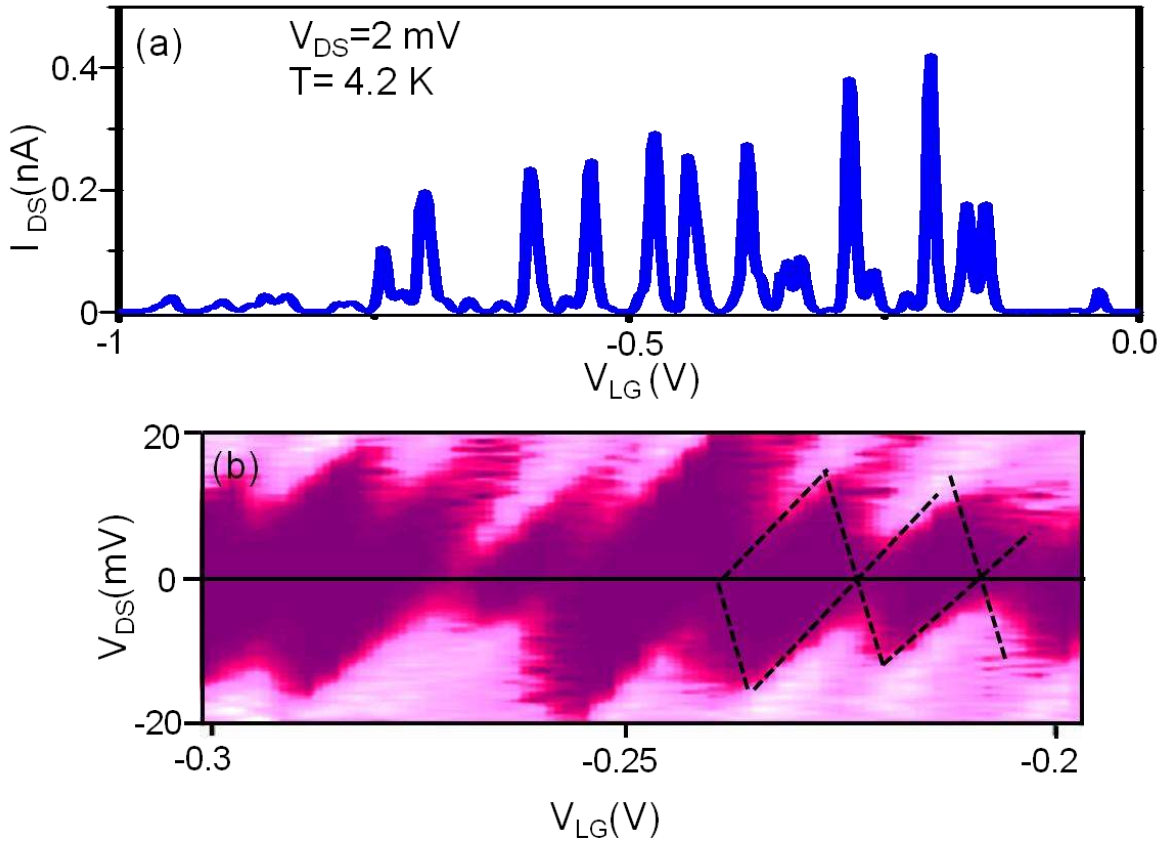


Figure 6.8 Low temperature electron transport properties of a representative mechanically templated semiconducting SWNT device (a) I_{DS} - V_G curve of the device at 4.2 K at $V_{DS} = 2$ mV showing periodic coulomb oscillation. (b) Color scale plot dI_{DS}/dV_{DS} vs V_{DS} vs V_{LG} at $T = 4.2$ K.

The size of the QD can be measured from the charging energy using the formula $U_C = 1.4 eV/L$ (nm), [25] yields, $L = 95$ nm which is the same as the width of the mechanical template. We have measured 20 s-SWNT devices. Out of them, 13 devices show similar single QD behavior with charging energy between 10 meV to 15 meV.

The rest 7 device does not show any coulomb blockade or coulomb oscillation at low T. However in this case the current oscillation is random. Besides the stability plot shows that the Coulomb diamond are not regular. The slopes of the diamond are different for different diamond and are not closing. This is an indication of multiple QD formation in the SWNT.

Semiconducting SWNTs generally have intrinsic defects. Those intrinsic defects act as tunnel barrier and break the SWNT into a number of QD in series.

6.5 Discussion

A summary of SET yield for the device fabricated using mechanical template technique is shown in table 5.1. It was found that SET behavior was observed for both metallic and semiconducting SWNT. This result suggests that the mechanical templating technique works for both metallic and semiconducting SWNT. This demonstrates that a combination of mechanical templating with the DEP is a scalable approach for the fabrication CMOS compatible SWNT SET.

Same as the top contact devices we see a correlation between the SET behavior and the room temperature resistance of the device. Mostly for the metallic devices with room temperature resistance (R_T) less than 100 K Ohm, SET behavior is not observed. This indicates that tunnel barriers are not created due to the mechanical templating. Besides, few of the semiconducting SWNT devices show multiple quantum dot behavior. These multiple QD can come from two sources. The first one is the structural defects intrinsic to semiconducting SWNT are present in the nanotube which act as tunnel barrier and give multiple QD behavior. Secondly, in addition to the tunnel barrier the edge of the local gate two more tunnel barrier could be created at the base of the mechanical template which could also give rise to multiple QD behavior at electron transport.

Table 6.1 Summary of the SET yield for mechanical template device

Type of SWNT	# of devices	Single QD	Multiple QD
<i>Metallic</i>	20	12	2
<i>Semiconducting</i>	25	18	7

6.6 Conclusion

In conclusion, we discuss a scalable way for CMOS compatible fabrication of SWNT based SET. This approach is based by controlled creation of tunnel barrier in SWNT via Al/Al₂O₃ local gate assembled in large scale via dielectrophoresis. Using electron transport measurement we demonstrate that a high SET yield. We also study the role of electronic type on the tunnel barrier formation in this device engineering method. We found those tunnel barriers are created for both metallic and semiconducting SWNT

6.7 References

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CHAPTER 7: ROOM TEMPERATURE OPERATING CARBON NANOTUBE SINGLE ELECTRON TRANSISTOR

7.1 Introduction

One of the major challenge for SET based device is to increase the operating temperature to room temperature[1-3]. For the practical application and commercialization it is indispensable that the SET based device should work at room temperature. Over the last one decade several techniques had been introduced for the fabrication of SWNT based room temperature operating SET (RTSET). This includes bending SWNT by AFM tip, local chemical modification of SWNT, introduction of defects by ion or nanoparticle[4-8]. In AFM manipulation techniques tunnel barrier is created by bending the SWNT using AFM tip. 20 nm QD is created by bending SWNT and the device shows room temperature SET operation. However, it is a complex device fabrication method and is very difficult to control the size of the QD. Introduction of defects via La nanoparticle or ion beam are not controlled fabrication process. Mostly multiple tunnel barriers are created in the SWNT which gives rise to multiple QDs. During the local chemical modification involve placement of a nanowire on the SWNT and removing it after coating the rest of the SWNT by polymer followed by oxygen plasma deposition at the exposed part. In this technique nanowires are thrown randomly and it is very difficult to place it on SWNT which reduces the device fabrication yield. In addition to the complex device fabrication steps, these techniques used random deposition of CVD growth techniques for the assembly of SWNT which makes them incompatible with current CMOS technology.

In this chapter we will discuss the fabrication of room temperature operating SWNT based SET. We use mechanical template technique to create the tunnel barrier and reduce the width of local gate down to 40 nm in order to fabricate smaller QD.

7.2 Device design and fabrication

For room temperature operation of the SET the charging energy of the device must be greater than the thermal energy at room temperature. However in order to get rid of thermal fluctuation the charging energy should be $U_C \sim 4k_B T$ [9, 10] which is ~ 100 meV for $T = 300$ K. The charging energy of SET is related to the capacitance of the quantum dot, $U_C \sim e^2/C_{tot}$. Thus in order to observe room temperature operation the capacitance of the SET should be smaller than 1.6 aF. The capacitance $C_{tot} = C_S + C_D + C_G$ where C_S , C_D , C_G are source, drain and gate capacitances respectively. The source and drain capacitance depends on the metal nanotube contact and cannot be controlled. While the gate capacitance of the carbon nanotube depends particularly on the length of the carbon nanotube and can be written as, $C_G = 2\pi\epsilon\epsilon_0 L / \ln(2h/r)$, where L is length and r is radius of the SWNT respectively and h is oxide thickness. So in order to fabricate room temperature SET a very small channel length is to be made. A plot of the charging energy of SWNT and length of SWNT is plotted in figure 6.1. From here it is observed that a SWNT device with channel length 50 nm or less can give a charging energy necessary to operate at room temperature.

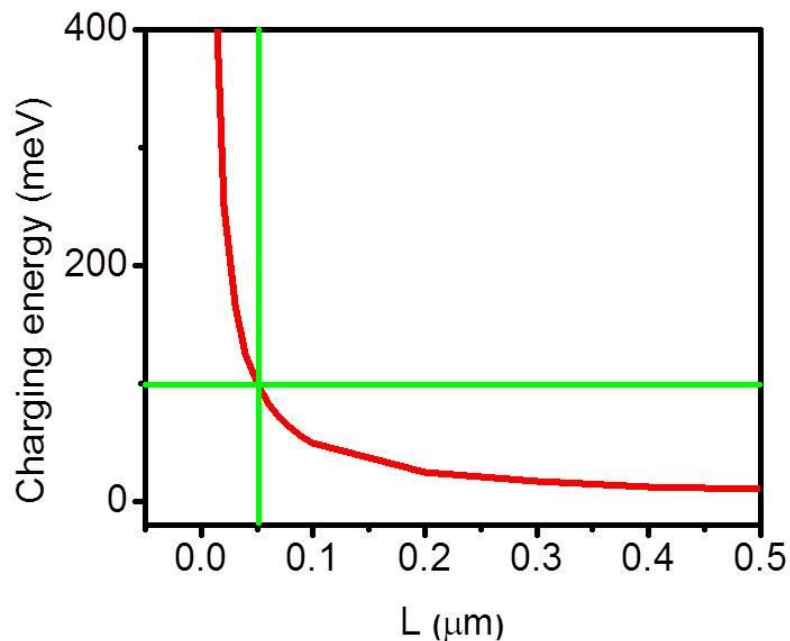


Figure 7.1 Charging energy as a function of the length of the SWNT QD

Here in this section we will propose parallel fabrication technique for room temperature operating SWNT based SET. In the previous chapter we have demonstrated that mechanical templating technique offer an attractive technique for the controllable fabrication of SET. The major advantage of mechanical template technique is that, we can control the size of the quantum dot by controlling the gate width. A small size of quantum dot is necessary for the fabrication of room temperature SET. Therefore, in order to obtain room temperature operation we will fabricate the local gate with very small width (~40 nm). A very tight control over the EBL is needed to fabricate SWNT of such small feature. After fabrication of the source and drain by Pd/Cr contact and defining the Al/Al₂O₃ local gate, we assemble individual semiconducting SWNT via DEP (figure 7.2 (a)-(b)). For the DEP assembly we use mixed SWNT solution from

Berewerscience. We use simultaneous deposition method for the DEP assembly and using the same DEP parameters applied in chapter 6.

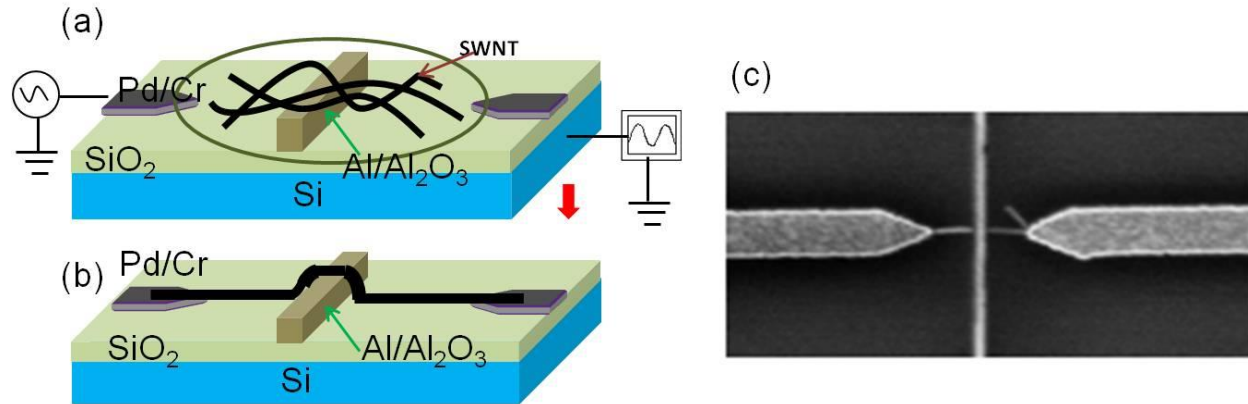


Figure 7.2 (a) Schematic for assembly of SWNT for the fabrication of RT SET by SWNT via dielectrophoresis (b) fabricated device after assembly (c) Scanning electron micrograph of individual SWNT assembled on top of a 40 nm Al/Al₂O₃ local gate.

Figure 6.2 (c) shows an SEM of individual SWNT assembled between metal electrodes with a the local gate of width 40 nm at the middle. Following DEP integration the devices were annealed at 200° C for one and half hour in a gas mixture of Ar/H₂ (1:3ratio) to reduce the contact resistance.

7.3 Electron transport measurements of RT SET

Figure 7.3 shows the diagram where current (I_{DS}) was plotted by sweeping the local gate voltage (V_{LG}) for a fixed bias voltage ($V_{DS}= 20$ mV) at various temperature from 40 K to 285 K. We found that I_{DS} shows periodic oscillation upto 285 K. These periodically spaced Coulomb oscillations peaks are signature of single-electron transistor characteristics. The spacing between successive peaks ΔV_{LG} was measured to be ~ 250 mV. It should be noted that the peaks have

broadened and the modulation amplitude of the total current becomes slightly smaller with increasing the measurement temperature.

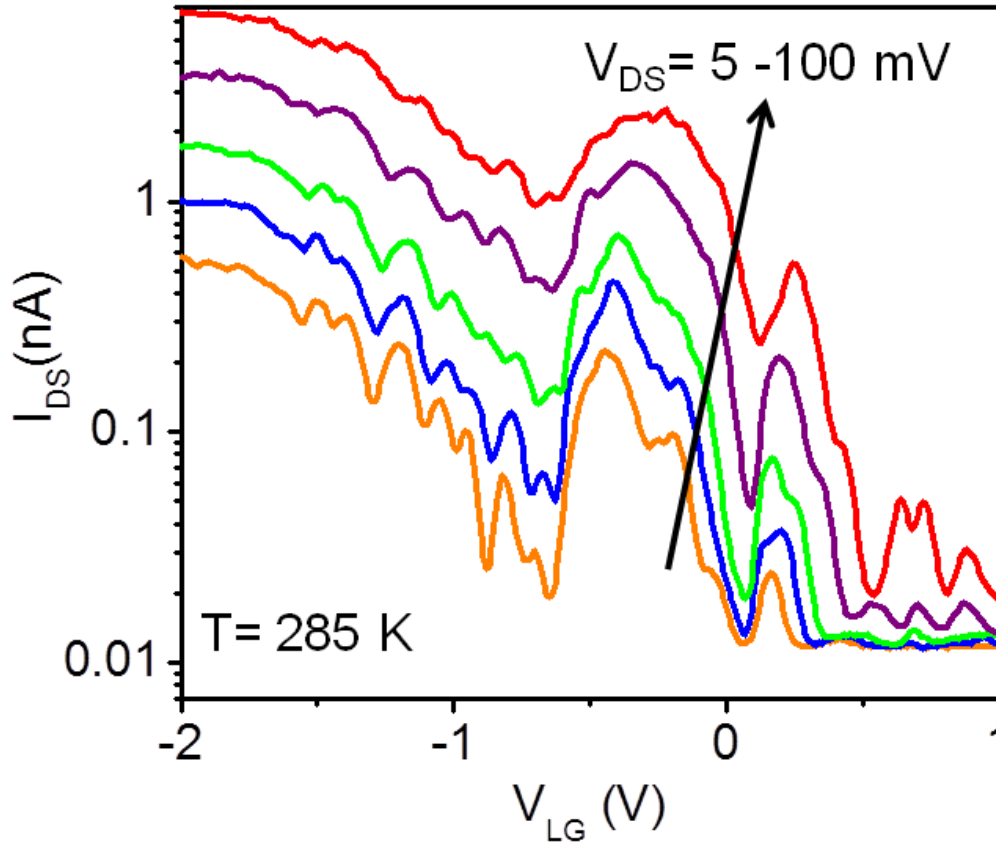


Figure 7.3 Drain current (I_{DS}) plotted by sweeping local gate voltage (V_{LG}) at room temperature ($T=285$ K), at different bias voltage (V_{DS})=5, 10, 20, 50, 100 mV.

As the temperature increases, electrons become thermally excited and take part in tunneling which results in an earlier onset and a delayed end to the Coulomb oscillation peak. The higher value of the baseline current can also be attributed to thermally activated electron tunneling which results in the Coulomb blockade region being smeared out. Similar transport behavior was obtained for RT SET made by SWNT using the other techniques[4].

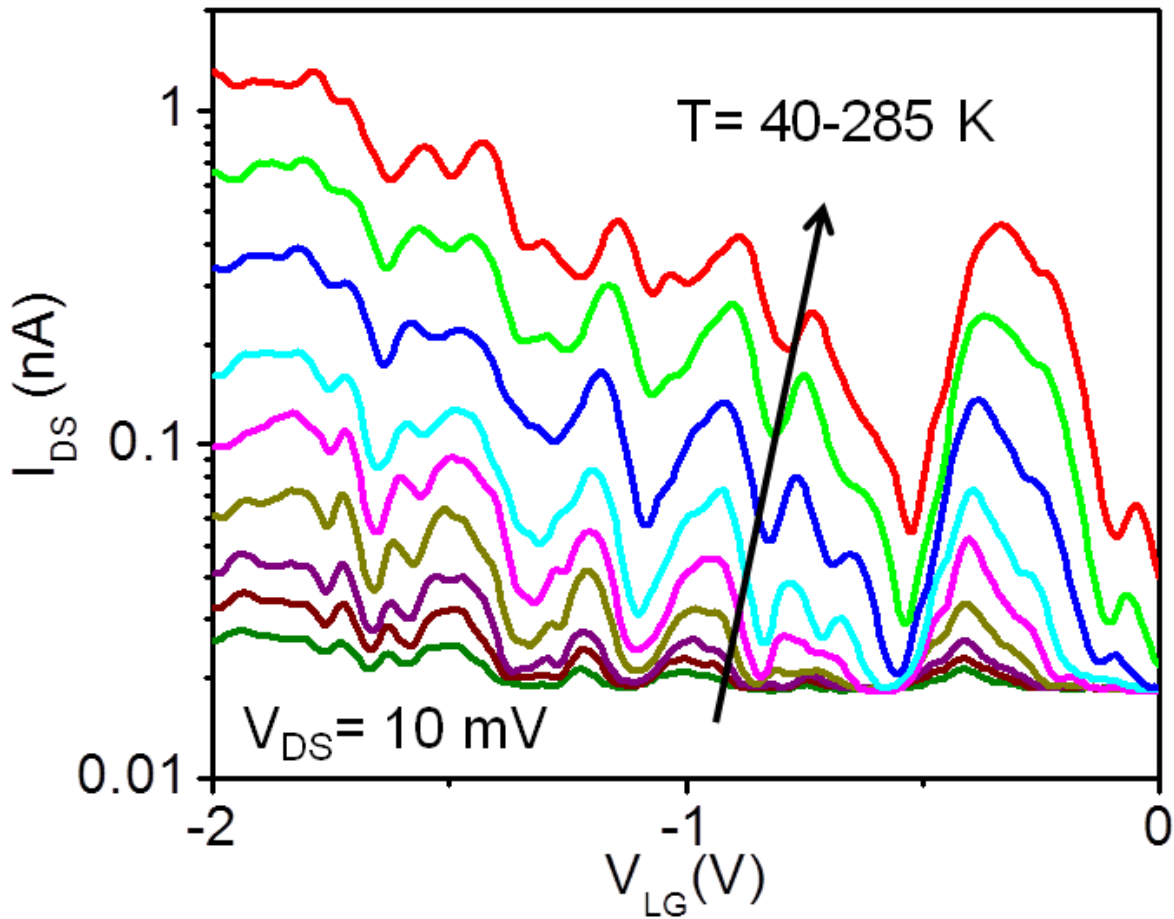


Figure 7.4 Drain current (I_{DS}) plotted by sweeping local gate voltage (V_{LG}) for different temperature (T) = 40, 50, 78, 125, 100, 150, 200, 250, 285 K). at fixed bias voltage (V_{DS})= 10, mV.

Figure 7.4 shows I_{DS} plotted by sweeping V_{LG} at $T=285$ K for a representative device. Here we swept the V_{LG} from -2V to 2V in steps of 10 mV at different $V_{DS} = 5, 10, 20, 50, 100$ mV. From figure it was found that I_{DS} increased with decreasing V_{LG} , indicating a p-type behavior. In addition to this current oscillation peaks were distinctly visible at 285 K. The current oscillation picks are found to be almost at the values of V_{LG} for different curve. The average gap between two successive Coulomb oscillation peaks ΔV_{LG} for the room temperature

measurement was also ~ 230 mV. The gate capacitance of the single electron transistor can be calculated from the orthodox theory using the formula $C_G \sim e/\Delta V_G \sim 0.7$ aF.

Figure 7.5 (a) is a color scale plot for I_{DS} vs V_{DS} vs V_{LG} . The brighter region symbolize single electron tunnelling, whereas the darker region represent coulomb blockade. Series of regular diamond shaped regimes (Coulomb diamond), which are signature of SET are observed throughout the entire local gate voltage range.

Figure 7.5 (b) is a plot of dI_{DS}/dV_{DS} vs V_{DS} vs V_{LG} . Here we keep the gate voltage range same as fig 7.5 (a)x. The brighter region presents single electron tunneling and coulomb blockade occur at the darker regions. A series of diamond shaped regions (often called coulomb diamond), which are signature of SET are observed throughout the entire local gate voltage range. In order for a guide to the eye the diamonds are outlined by black dot. It was found that each diamond is equally spaced with $\Delta V_{LG} \sim 250$ mV. Besides slopes of each diamonds are same and all the diamonds closes at $V_{DS}=0V$. This indicates the measurements of a single QD.

The charging energy (U_C) of the QD can be directly obtained from the height of the diamond and is found to be $U_C \sim 150$ meV. The gate capacitance is calculated using the formula, $C_G = e/\Delta V_G$, where ΔV_G is the period between the diamonds. The period of the diamond, $\Delta V_G \sim 270$ mV obtained from the stability plot yields $C_G \sim 0.6$ aF. The source and drain capacitances can be calculated from the positive slope $\alpha_1 = -C_G/C_1$ and negative slope $\alpha_2 = C_G/(C_1 + C_2)$ of the diamond respectively, which yield $C_1 \sim 0.3$ aF and $C_2 \sim 0.2$ aF.

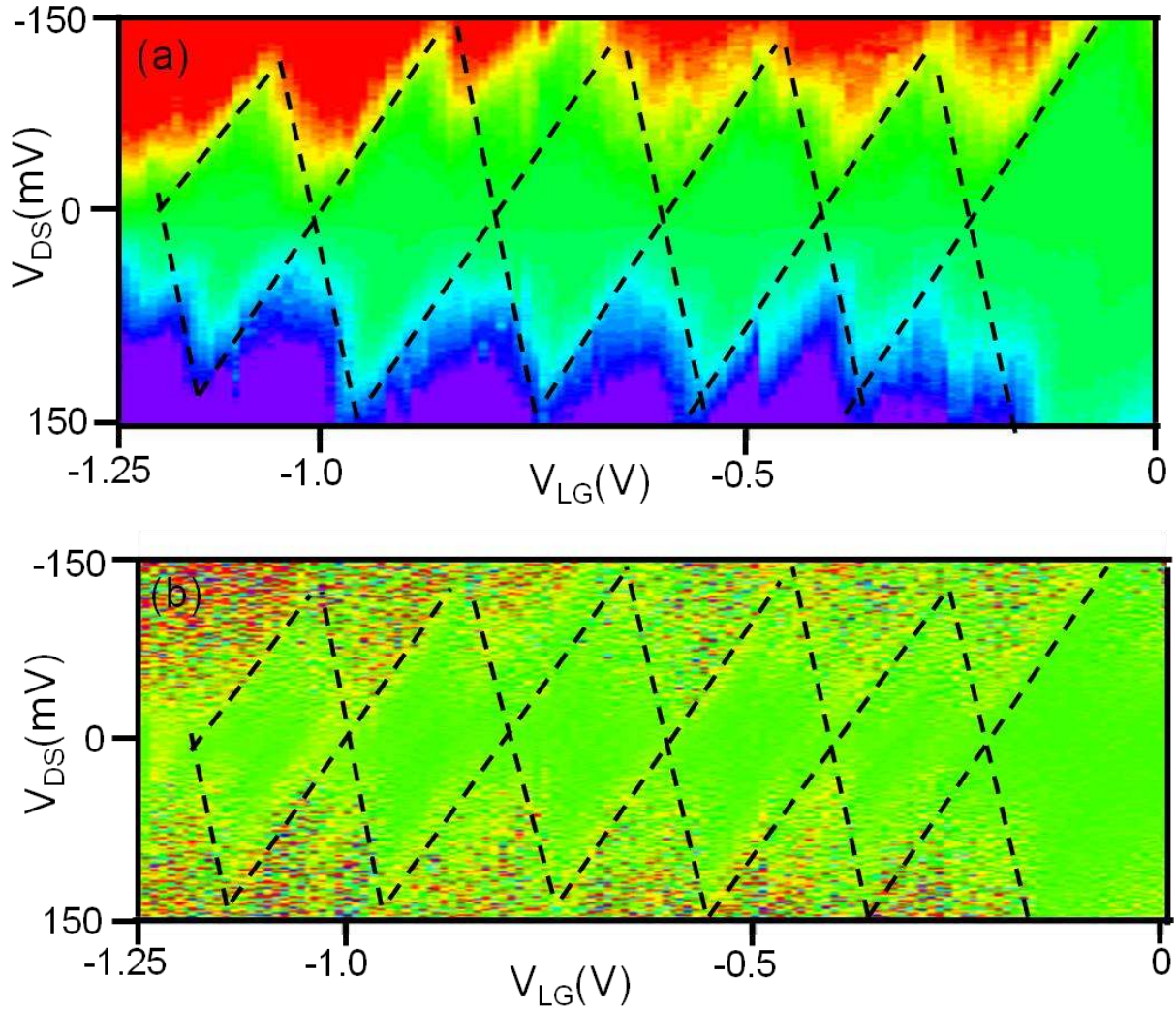


Figure 7.5 (a) Plot of I_{DS} as a function of V_{LG} and V_{DS} at $T=78K$ showing Coulomb blockade (b) Plot of dI_{DS}/dV_{DS} as a function of V_{LG} and V_{DS} at $T=78K$ showing Coulomb diamond.

Which gives total capacitance, $C_{\Sigma} = C_1 + C_2 + C_G = 1.1$ aF for the QD. The charging energy of the SET can be obtained using the relation $U_c = e^2 / C_{\Sigma}$, yielding a charging energy which can be used to calculate the charging energy of $U_c \sim 145$ meV, matches well with the value measured directly from the height of the diamond in the stability diagram.

A total of 11 devices were measured in this study. Out of them 4 devices show metallic behavior and 7 devices show semiconducting behavior at room temperature. It was observed that the metallic device does not show any coulomb oscillation even at low temperature ($T= 4.2$ K), this means that tunnel barrier was not created for metallic SWNT. On the other hand all of the 7 semiconducting SWNT devices show coulomb oscillation at low temperature. However, only 4 of them give coulomb oscillation upto room temperature. The other three devices coulomb oscillation persist upto 150-200K.

Since only the semiconducting devices show coulomb oscillation at room temperature one might argue that this is due to the intrinsic structural defects presents in the SWNT. In order to verify whether the QD is really formed due to mechanical template or due to the intrinsic defects presents in the semiconducting SWNT, we make several SWNT device with channel length 400 nm same as the separation of SWNT between the edge of the local gate and source (drain). Figure 8.6 shows the temperature dependent I_{DS} vs V_{BG} for a fixed $V_{DS}= 50$ mV for such a back gated device at various temperature from 77 K to 285 K. Unlike local gated device periodic current oscillation at 77K. Even though few oscillation picks appear at 77K, however the picks were not consistent and it diminishes with increase of temperature and position of the pick changes with temperature. This indicates that the current oscillation is due to the presence of intrinsic defects in the SWNT channel. However this is not the case for our mechanically template SWNT

Similar transport properties were observed for 3 other devices. It is interesting to note here is that metallic SWNT does not show SET characteristics at room temperature. Similar phenomena were reported for the room temperature operating SWNT SET fabricated by gate

modification. For our case the reason for not observing the SET behavior with 40 nm local gate is that tunnel barrier might not be created by the mechanical template.

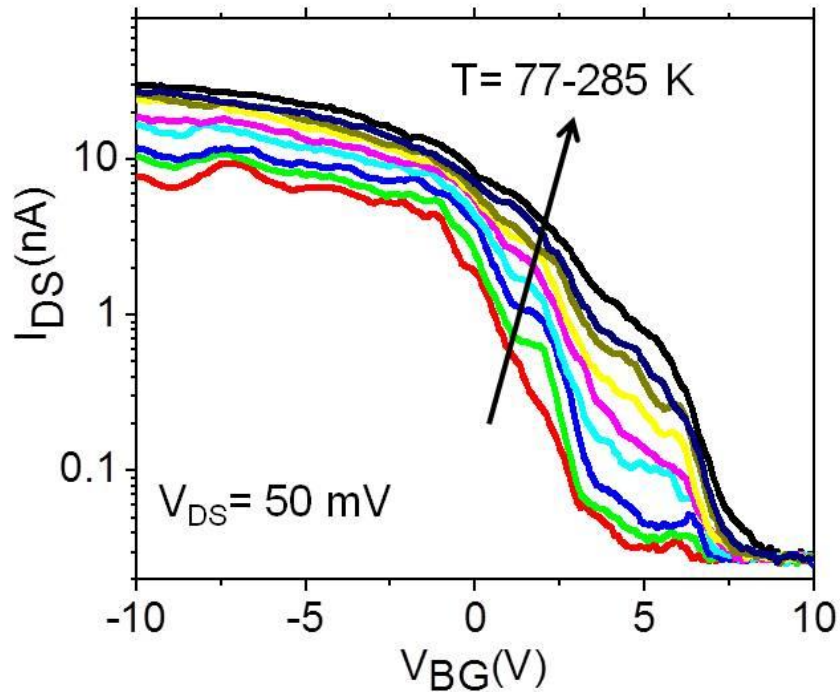


Figure 7.6 Drain current (I_{DS}) Plotted as a function of back gate voltage (V_{BG}) at different temperature (T) = 40, 50, 78, 125, 100, 150, 200, 250, 285 K). at fixed bias voltage (V_{DS})= 10, mV for a 300 nm back gated semiconducting SWNT device..

7.4 Conclusion

In conclusion, room-temperature-operating single electron transistor has been fabricated by mechanical templating of individual SWNT. Tunnel barriers are defined by the edge of the mechanical template and single quantum dots are defined. More importantly the SWNTs are assembled by dielectrophoresis which is compatible with conventional CMOS technology. This

controlled and CMOS compatible SWNT fabrication via mechanical templating should open a avenue for the commercialization of SWNT based SET devices

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CHAPTER 8: CONCLUSION

8.1 Summary

In this thesis, parallel fabrication of single electron transistors (SETs) using solution processed SWNTs in assembled by dielectrophoresis (DEP) and a comprehensive electronic transport properties were studied. The basic concepts of carbon nanotube and device fabrication techniques are discussed in chapters 1-3 and the relevant experiments were described in chapters 4-7.

In chapter 4, we showed approach for large scale assembly of SWNT devices and studied their transport properties. By optimizing the DEP parameter it possible to obtain 25% assembly yields for individual SWNT. A combination of DEP

In chapter 5, we showed that a method for scalable, and CMOS compatible fabrication of SWNT SET devices from carbon nanotube and investigated their electronic properties in detail. This method is based on assembly of individual SWNT via dielectrophoresis followed by metal top contact. Device fabricated by this technique give 75% SET yield and the transport study reveal a correlation between the room temperature resistance and the SET performance.

In chapter 6, we showed a different technique for the parallel fabrication of SET devices from carbon nanotube and investigated their electronic properties. A combination of DEP technique together with a mechanical template demonstrates the parallel fabrication of SET devices from SWNT.

In chapter 7 we showed an approach for the room temperature operating SET by scaling down the local gate width to sub 50 nm. Using low temperature transport we proved that the SET operation occurs due to the mechanical template and not due to the intrinsic structural defects.

8.2 Future Directions

8.2.1 SET fabrication via DEP assembly of ultra-short SWNT

Even though room temperature operating SET was fabricated using mechanical template but I was not able to show room temperature operation using top contact technique. This could be due to the inefficient gate coupling. Even though we use 30-40 nm channel length SWNT device however with a 250nm SiO₂ back gate. The gate coupling can be used by reducing the gate oxide thickness.

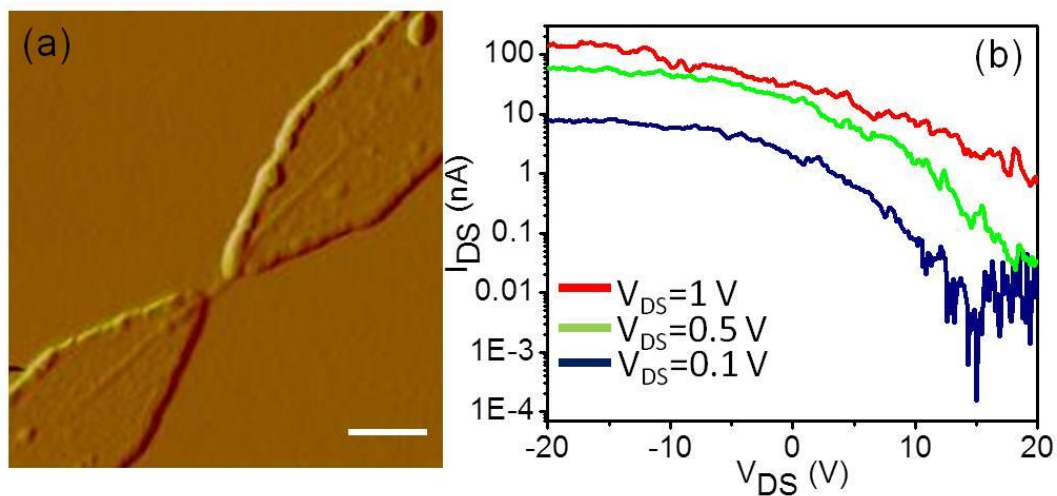


Figure 8.1 (a) Atomic force microscope (AFM) image of individual SWNT assemble between a 100 nm channel length electrode separation via dielectrophoresis. (b) Transfer characteristics of the device shows transistor operation.

Assembly of ultra-short SWNT between short electrodes with source-drain separation of 20-100 nm could be a easier approach to assemble SWNT SET. I have done some preliminary experiments in the assembly of ultrashort SWNT. We assemble individual SWNT between source-drain electrodes with separation 100nm and 40 nm. Although the assembly yield was extremely low, I was successful in assembling individual SWNT. Figure 8.1(a) shows SEM image of individual SWNT integrated between 100 nm electrodes. Figure 8.1(b) shows the I_{DS} vs V_G plot for the device. However most of the device does not show any FET behavior. Again this is due to the inefficient gate coupling. In order to increase the gate coupling we define Al_2O_3 oxide channel at the middle of between the source-drain electrodes. After that we assemble individual SWNT. The assembly yield is very low. The assembly yield can be increased by using ultra-short SWNT. Ultra-short SWNT can be made by aggressive sonication of SWNT solution.

8.2.2 SET fabrication using atomically thin MoS_2

Molybdenum disulfides (MoS_2) have recently gained lots of attention from both technological and physical point of view for their unique electrical, optical, mechanical and chemical properties [1-4]. MoS_2 belongs to the transition-metal dichalcogenide (TMD) family, bulk MoS_2 is a semiconductor with indirect band gap of 1.2 eV while the single layer has a gap of 1.8 eV [5]. Single and multilayer MoS_2 demonstrate excellent electronic properties including high current on-off switching ratio (10^8), steep subthreshold swing (~ 74 meV/dec) together with large carrier mobility (~ 200 cm^2/Vs for single layer MoS_2) depending on the thickness and dielectric used[6-10]. Different prototype devices including Field effect transistor, integrated circuit, phototransistor, solar cell, chemical sensor, memories have been widely demonstrated using single and multilayer MoS_2 [6, 11-17]. However fabrications of SET have never been

demonstrated using MoS₂. Very recently we have demonstrated that the electrical property of multilayered MoS₂ FET can be tuned from semiconductor in insulator by controlled exposure to oxygen plasma [18]. Thus by a selective exposure of MoS₂ flake to oxygen plasma it is possible to create MoS₂ QD.

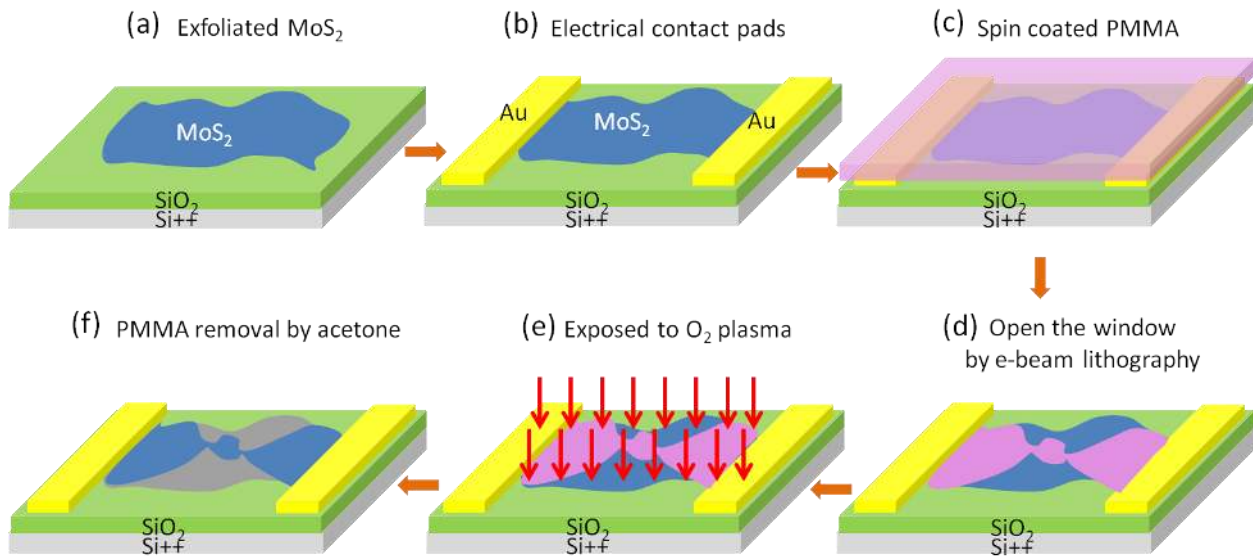


Figure 8.2 Schematics of the quantum dot fabrication on MoS₂. (a) Exfoliation of MoS₂ on Si/SiO₂ substrate (b) Metallization of gold (Au) electrode on the selected flake (c) spin-coating PMMA resist, (d) opening a window of nanoscale dimension on the MoS₂ flake via EBL (e) the sample is exposed to oxygen plasma (f) removing PMMA using acetone and nano-constriction is created at exposed portion of MoS₂.

Schematics for the steps involved in tunnel barrier fabrication in MoS₂ are shown in figure 8.2. To fabricate the devices, MoS₂ flakes were mechanically exfoliated from bulk crystal of molybdenite commercially available from SPI Supplies Brand. Single layer and few layer MoS₂ flakes will be transferred using adhesive tape micromechanical cleavage technique on a p-doped Si substrate with 250 nm thick SiO₂ on top was used as back gate. Following mechanical exfoliation, the location of MoS₂ flakes will be identified by an optical microscope and the

contrast of the optical microscope image give an idea about the thickness of the flake. Whereas tapping mode atomic force microscopy (AFM) is used to measure its thickness.

In order to fabricate electrode pattern on selected MoS₂ flakes at first a double layer electron beam resists, methyl methacrylate/poly(methyl methacrylate) (MMA/PMMA) need to be spin coated on the substrate and baked at 180 °C. Then electrodes are then defined using standard electron beam lithography (EBL). Following e-beam exposure the pattern will be developed in (1:3) methyl isobutyl ketone : isopropyl alcohol (MIBK:IPA). After defining the electrodes, Au will deposited by thermal evaporation, and lift off in acetone. After deposition of metal contact the flake will be spin coated by a PMMA layer. Electron beam (e-beam) lithography is used for the creation of constriction to define QD. Oxygen plasma will then be introduced to make the undesired region of the MoS₂ insulating. Finally the PMMA layer will be washed out using Acetone. Figure 8.2 shows a schematic for the MoS₂ QD device.

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