Parallel-Optical Interconnects >100 Gb/s

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***Abstract*—A parallel-optical interconnect with 12 channels operating at 8.5 Gb/s giving an aggregate data rate of 102 Gb/s is demonstrated, to the authors' knowledge, for the first time. The paper describes and demonstrates 13 × 16-mm cross-section 12-channel parallel-optic transmitter and receiver modules with each channel operating at a data rate of 8.5–10 Gb/s. This was achieved using bottom-emitting 990-nm vertical-cavity surface-emitting lasers and bottom-illuminated InGaAs–InP photodetectors flip-chip bonded directly to 12-channel transmitter and receiver integrated circuits, respectively. In addition, 102-Gb/s link results are demonstrated over 100 m of 50-μm-core standard multimode ribbon fiber. A bit-error ratio of $< 10^{-13}$ was measured on a single channel after transmission through 100 m of multimode fiber at a data rate of 8.5 Gb/s with all 12 channels operating simultaneously.**

***Index Terms*—Data communication, interconnections, optical arrays, optical fiber communication, parallel optics, surface-emitting lasers.**

I. Introduction

DATA RATES are continuing to increase for box-to-box, rack-to-rack, board-to-board, and chip-to-chip interconnects for terabit switches and routers, digital cross-connect systems, multiprocessor computers, and high-end servers. The increase in individual line rates and bandwidth density drives the need to replace copper interconnects with optical interconnects. The main advantages of optical interconnects for these applications are longer link lengths, increased bandwidth density, smaller cables and connectors, less susceptibility to electromagnetic interference (EMI), and potentially lower power dissipation, depending on the data rate and link length. Parallel-optical interconnects with 12 channels operating at a data rate of 2.5 Gb/s/ch over 600 m of multimode fiber (MMF) ribbon are commercially available today [1]. Agilent Technologies' commercial products are based on a module platform and components that were developed at Agilent Laboratories [2], [3].

Next-generation parallel-optical interconnects are aimed at 12 channels operating at a data rate up to 10 Gb/s/ch. Some components for next-generation parallel-optical interconnects have been previously published [4], [5]. In addition, a 12 × 10-Gb/s transmitter module using 850-nm vertical-cavity surface-emitting lasers (VCSELs) has been reported; however, a receiver module was not reported as part of that work [6]. In this paper, technologies to achieve parallel-optical interconnects with 12 channels operating at a maximum data rate of 10 Gb/s/ch giving a maximum aggregate data rate of 120 Gb/s are described. These technologies are being developed in an Agilent Laboratories' project called Parallel Optics for Super-Highways (POSH) [7]. The design and experimental results of both a POSH transmitter (TX) and receiver (RX) module with each channel operating at a data rate of 8.5–10 Gb/s will be described. This paper will describe the package design, flip-chip bonding, link budget, 990-nm bottom-emitting VCSELs, bottom-illuminated photodetectors (PDs), low-cost microoptics, multichannel integrated circuits (ICs), and the high-speed electrical design.

II. Package Design

The POSH package design leverages the patented electrical-turn design used in the Agilent Laboratories' PONI platform [2], [3], [8]. Major new features to achieve a maximum data rate of 10 Gb/s/ch include an optical subassembly (OSA) called the chip-mounted enclosure (CME), flip-chip bonding, advanced high-speed electrical design, and an advanced heat-pipe thermal management system. An exploded view of the POSH prototype module is shown in Fig. 1.

A. Chip-Mounted Enclosure

The heart of the POSH module is the CME, which was designed to be manufactured in wafer scale [7], [9]. Like its predecessor PONI, POSH leverages a common platform between TX and RX modules, using the same flex circuit, heat sink, and passive components. As shown in Fig. 1, the base of the CME is a 5.5 × 6-mm TX or RX IC. In preparation for flip-chip bonding of the optoelectronics (OEs), the wafer of ICs is solder bumped, and simultaneously a lower solder seal ring $(\mathrm{Pb}_{0.95}\mathrm{Sn}_{0.05})$ is deposited around the OE portion of the die. The next step is to attach the wall, which provides some EMI shielding for the OE devices and serves to set the height of the lens array relative to the OEs. Currently, the wall is made from KOH-etched highly doped Si, which is thermally matched to the IC and optics and

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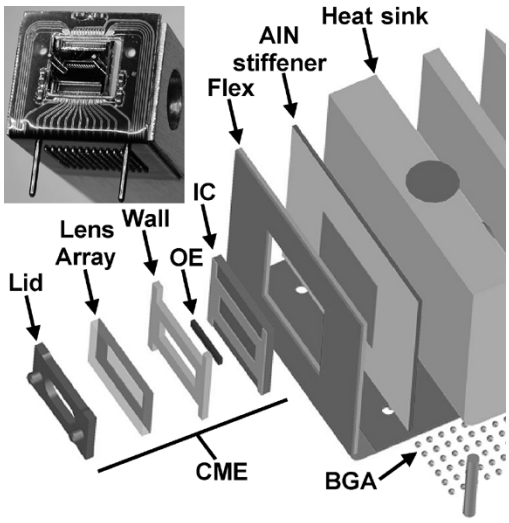

Fig. 1. Exploded view of the POSH module showing CME with an inset showing a photograph of a functional POSH RX module.

is very flat. At this point, an array of bottom-illuminated PDs or bottom-emitting 990-nm VCSELs is flip-chip-bonded onto the IC.

The next step is to attach the lens array, which may contain additional metallization to improve EMI protection. While we have demonstrated a solder seal in this step to produce a hermetic die-level package, most of the parts tested have a high-temperature epoxy bond instead. Next, the lid is actively aligned and attached to the CME, which provides mechanical alignment to an MMF ribbon with a multifiber-terminated (MT)-ferrule termination. This attach is currently done using a high-temperature epoxy bond but could be a solder bond if additional strength were required. For the current prototypes, we actively align the lid after the module has been assembled and placed on our test fixture. The current lid consists of a deep reactive-ion-etched (RIE) Si lid with glued stainless-steel MT pins. This lid design has not been tested for repeated connects/disconnects to show robustness.

B. Module Construction

A flex circuit is used to interface the CME to a ball-grid-array (BGA) interface. This provides an electrical turn while maintaining a low-loss, high-bandwidth 50-Ω signal transmission path. Assembly starts by attaching an aluminum nitride (AlN) stiffener to the back of the flex circuit in the CME area. This forms the bottom of a chip well to receive the CME and provides for a high thermal conductivity path to the heat sink, while isolating the CME electrically from the heat sink. The CME, not including the lid in the current prototypes, is then attached and wire-bonded to the flex.

Wire-bond pads along the upper edge of the IC are used for power supplies, and wire-bond pads along the lower edge of the IC are used for power supplies and the high-speed digital inputs/outputs (I/Os). Wire-bond pads are omitted from the side edges of the IC in order to accommodate 12 channels in the space between the MT-ferrule alignment pins. It is possible to place wire-bond pads on all four sides of the IC (if needed for higher channel count) by increasing the width of the IC and potentially increasing the cost of the CME. The lengths of the wire bonds for the high-speed I/Os are minimized by placing the CME in a chip well so that the wire-bond pads on the IC are approximately in the same plane as the bond pads on the flex, and the CME is positioned as low as possible in the well. The estimated inductance of a typical high-speed I/O wire-bond differential pair is $\sim$1 nH. Modeling has shown that these wire bonds do not limit the performance at a data rate of 10 Gb/s.

After the CME attach, the flex is attached to the heat sink using a high-temperature epoxy for the BGA area and a high-thermal-conductivity epoxy for the CME area. The 0.75-mm-pitch BGA is populated with $\mathrm{Pb_{0.9}Sn_{0.1}}$ balls with a diameter of 380 μm using a PbSn eutectic paste and reflowed at $\sim$ 230 °C. Note that after multiple reflows at $\sim$ 230 °C, no stress cracking of the wire bonds from the CME to the flex has been observed. The part is then ready for testing and active alignment of the lid. The inset of Fig. 1 shows a photograph of a functional POSH RX module with an evaluation heat sink. Functional POSH modules have also been built and tested with the heat-pipe heat sink.

C. Thermal Design and Results

POSH modules employ an advanced thermal management scheme to minimize card-edge area. The POSH heat sink has a heat-pipe core to evenly distribute heat over the entire length of the module, allowing for a much longer heat sink than would be effective using conventional technologies. The POSH heat sink is aluminum with a 3-mm-diameter copper internal heat pipe. The heat pipe uses water at reduced pressure for the working fluid due to its excellent thermal properties. A 75-mm version was designed to handle 6 W with an ambient temperature of 55 °C and 1-m/s air flow resulting in a $<$ 85 °C face temperature. The heat pipe works as a passive closed-loop cooling system, providing 100$\times$ better effective thermal conductivity than the best metals. In addition, the heat pipe becomes more efficient at higher ambient temperatures as the viscosity of the working fluid decreases. Heat pipes are an established cooling scheme in servers and laptops, but this is the first demonstration of their use in a fiber-optic communications module.

In [10], piggyback mounting of VCSELs is compared with a tandem configuration, which showed a small ($\sim$ 2 °C) penalty for placing the VCSEL die on top of the IC with the junction up. To validate the use of a flip-chip or junction-down approach, a series of models were made of the POSH CME to predict its thermal performance. The models predicted junction-to-case thermal resistance θ_{jc} to be $\sim$ 5 °C/W. θ_{jc} may be decomposed into two components, including the OE array junction-to-substrate thermal resistance θ_{js} and the substrate-to-case thermal resistance θ_{sc}, where the substrate is the Si–Ge IC. Under the assumption that θ_{js} sees only the power dissipated by the OE array and θ_{sc} sees the total power dissipation, the OE junction-to-case temperature T_{jc} may be expressed as

$$T_{\mathrm{jc}} = \theta_{\mathrm{jc}} P_{\mathrm{tot}} = \theta_{\mathrm{js}} P_{\mathrm{OE}} + \theta_{\mathrm{sc}} P_{\mathrm{tot}} \tag{1}$$

where P_{tot} is the total power dissipation and P_{OE} is the power dissipation of the OE array. θ_{sc} is estimated to be 0.25 °C/W, which includes the thermal resistance of the Si–Ge IC, the AlN stiffener, and the die attach materials between both the IC and

stiffener and the stiffener and heat sink. Further modeling of the heat sink was carried out and verified by an experiment that showed a case-to-ambient thermal resistance $\theta_{\rm ca}$ of $\sim$ 4 °C/W at an ambient temperature of 22 °C, which decreases by $\sim$10% as the ambient temperature is increased to 55 °C.

Thermal measurements were performed for both a TX and an RX module using a long-wavelength (3.5–5-μm) infrared camera and a wind tunnel. Since the substrate of the VCSEL and PD is reasonably transparent at these wavelengths, the junction temperature may be observed. The TX module used a 50-mm heat sink. With 1-m/s airflow, 25 °C ambient temperature, $P_{\rm tot}$ of 1.5 W, $P_{\rm OE}$ estimated to be $0.0624 \times P_{\rm tot}$, and $T_{\rm jc}$ of 7 °C, $\theta_{\rm ca}$ was 6 °C/W, which is in line with predictions, $\theta_{\rm jc}$ was 4.7 °C/W, and $\theta_{\rm js}$ was 70.8 °C/W. We would expect a higher $\theta_{\rm ca}$ for the shorter design. From our modeling, there is very little thermal crosstalk between devices; therefore, $\theta_{\rm js}$ for a single VCSEL is estimated to be 70.8 °C/W $\times$ 12 $\approx$ 850 °C/W when using the thermal camera measurements. The OE (VCSEL) junction temperature $T_{\rm OE}$ was 41 °C. Scaling up to 55 °C ambient temperature, we would expect the OE junction to be $<$ 70 °C, well below the specified temperature of 85 °C. Since the spatial resolution of the infrared camera may not be sufficient to measure the peak temperature in the VCSEL junction, we measured the spectral shift of the VCSEL versus bias current. Using this data, we obtain a $\theta_{\rm js}$ of $<$ 1720 °C/W for a single flip-chipped VCSEL. Using this $\theta_{\rm js}$, the VCSEL junction temperature is expected to be $<$ 77 °C with the ambient temperature at 55 °C, still well below the specified temperature of 85 °C. The RX module used a 75-mm heat sink. With 1-m/s airflow, 25 °C ambient temperature, and a $P_{\rm tot}$ of 4.5 W (worst-case RX IC power dissipation), $\theta_{\rm ca}$ was 4.2 °C/W, which agreed well with the model, and $\theta_{\rm jc}$ was 2.7 °C/W, which was slightly better than expected, and $T_{\rm OE}$ was 56 °C. At 55 °C ambient temperature, we would expect the junction to be $<$ 80 °C, well below the specified temperature of 95 °C.

III. Flip-Chip Bonding

Flip-chip bonding was chosen in order to minimize parasitics between the OE devices and the ICs. Specifically, the loop inductance and capacitance are estimated to be reduced by a factor of 4 as compared with wire bonds with an estimated loop inductance of $<$0.2 nH and capacitance of $<$50 fF. This will result in performance advantages including larger bandwidth, less overshoot and ringing, and lower EMI [11]. In addition, the use of flip-chip bonding enables the following:

1) VCSEL array construction;
2) the use of two-dimensional arrays;
3) integrated optical power monitors in the IC;
4) the use of the CME.

For ease of manufacturing, the solder balls were fabricated on the Si–Ge ICs. The pad pitch on the OE is 120 μm, which was approximately one half of the standard pitch used in state-of-the-art solder-bump technology. The high-Pb $(\rm Pb_{0.95}Sn_{0.05})$ solder balls had an average diameter and pitch of 60 and 120 μm. The PDs and VCSELs were prepared for flip-chip die attach by adding a passivation and underbump metallization step. The selected underbump metallurgy is a good diffusion barrier for Pb–Sn and other metals to the OE. In addition, a top metal of Au wets the Pb–Sn solder bumps to secure a strong bond.

The OEs were attached to the IC with a Karl Suss Flip Chip Bonder Model 150 (FC150). The FC150 enables control of planarity, z height, and x–y alignment to within ± 1 μm of the bonded chip. The alignment tolerance depends upon the thermal mismatch between the chip and substrate and the bonding process. During the flip-chip process, the parts are brought into contact with one another, a gas composed of 3% $\rm H_2$ and 97% $\rm N_2$ flows over the parts, the solder is heated to reflow, and the VCSEL or PD array is moved vertically into the solder. The entire bonding process takes several minutes. The selection of the $\rm Pb_{0.95}Sn_{0.05}$ solder combined with subsequent attaches at lower temperatures enables these modules to be built without an underfill material between the OE device and the IC.

IV. Link Budget

In order to specify the individual component requirements for a POSH module, the overall link requirements were modeled, which resulted in a link budget. The link budget for a single channel is calculated using a modified version of the Spreadsheet Link Model used extensively in the IEEE for the 802.3z (Gigabit Ethernet) and 802.3ae (10-Gigabit Ethernet) Standard [12]. In Table I, the link budget is shown for a wavelength of 990 nm over 100 m of standard 50-μm-core MMF (50MMF) and 160 m of enhanced-bandwidth 50MMF at a data rate of 10 Gb/s. The bandwidth–distance product of the fiber was determined by a series of measurements on enhanced-bandwidth fiber from several vendors [13].

The maximum power out of the TX module is set by the International Electrotechnical Commission (IEC) Class 1 (2000) eye-safety limits for a VCSEL array at this wavelength allowing for variations of the numerical aperture for these devices. The minimum TX power is set by allowing a margin for the temperature range, device uniformity, and degradation over life. Fiber and connector penalties include a 0.5-dB connector loss, fiber loss, and dispersion penalties. For these fibers, modal dispersion constitutes the primary dispersion contribution. The optical power at the PD is obtained by subtracting the connector loss, fiber loss and power penalties, and the RX coupling loss from the TX optical power. A POSH link, which meets these targets, should perform adequately at 10 Gb/s/ch over 160 m of enhanced-bandwidth 50MMF. In order to reach 100 m over standard 50MMF, a slightly better RX sensitivity is required. In practice, the bandwidth–distance product at 990 nm on standard 50MMF is estimated to be $\sim$1.5–2X better than the minimum specification of 500 MHz $\cdot$ km, easing the receiver sensitivity requirements.

V. Optoelectronics

A. Motivation for 990-nm VCSELs and PDs

990-nm VCSELs are well positioned to serve the 10-Gb/s parallel-optics market since they are compatible with flip-chip bonding (transparent substrate), and there is a high confidence level of their manufacturability. 850-nm VCSELs have been designed for flip-chip bonding; however, these require removal or replacement of the opaque GaAs substrate [14], [15].

TABLE I
POSH TARGET LINK BUDGET AT 10 Gb/s

Wavelength	990				nm
Fiber Bandwidth-Distance Product	1000		500 (min)		MHz-km
Link Length	160		100		m
Link Budget	Max	Min	Max	Min	
Transmitter Output Power	-1.80	-6.80	-1.80	-6.80	dBm
Fiber & Connector Loss, Dispersion	-0.50	-5.45	-0.50	-7.00	dB
Receiver Coupling Loss	-0.50	-2.00	-0.50	-2.00	dB
Optical Signal @ Photodetectors	-2.80	-14.25	-2.80	-15.80	dBm
RX Sensitivity @ Photodetectors (opt)	-15.50	-15.50	-16.00	-16.00	dBm
RX Sensitivity @ Photodetectors (elec)		16.91		15.07	μAavg
Link Margin @ Link Length		1.25		0.20	dB
Photodetector Responsivity	0.75	0.60	0.75	0.60	A/W
Electrical Signal @ Photodetectors	393.61	22.55	393.61	15.78	μAavg
Signal Dynamic Range		12.42		13.97	dBopt

There is also an estimated 3.4-dB link budget advantage for 990-nm VCSELs as compared with 850-nm VCSELs due to a higher eye-safety limit (∼2.8 dB higher) and a higher responsivity of the photodiodes (∼0.6 dB higher). The device advantages that 990-nm VCSELs have over 850-nm VCSELs include the following:

1) lower operating voltage;
2) higher differential gain;
3) lower threshold current;
4) higher speed;
5) improved reliability;
6) lower photon energy;
7) lower thermal resistance.

InGaAs PDs may be designed for 10-Gb/s operation and may have a transparent InP substrate, enabling flip-chip bonding. In order to guarantee the substrate is transparent over the entire operating temperature range, a minimum operating wavelength of 990 nm is chosen.

Since the majority of parallel-optical interconnects are proprietary links, there is no present requirement to continue to use 850-nm OEs, which are currently used in many of the standards-based single-channel transceiver modules and current 12 × 2.5-Gb/s parallel-optical interconnects. Due to the technical advantages of 990-nm OEs, we believe that 990-nm OEs are the preferred solution for one-dimensional and two-dimensional parallel optics operating at data rates of 10 Gb/s/ch and beyond. However, if 1310-nm VCSELs operating at a data rate of 10 Gb/s are proven to be reliable and manufacturable, then they would be a drop-in replacement for the 990-nm VCSELs. In this case, this would be the preferred solution since 1310-nm OEs are also currently used in many standards-based transceivers. The InGaAs PDs being used at 990 nm will also operate at 1310 nm with an improved responsivity.

B. 990-nm Bottom-Emitting VCSELs

The 990-nm bottom-emitting VCSEL structure comprises a one-wave cavity with multiple InGaAs quantum wells, 27 pairs of Si-doped n-type bottom AlGaAs distributed-Bragg reflectors (DBRs), and 40 pairs of carbon-doped p-type top AlGaAs DBRs. The DBR hetero-interfaces are graded with increased doping at the optical nulls of the standing-wave pattern to reduce the series resistance of the DBR mirrors.

The VCSEL structures were grown on semi-insulating GaAs substrates using a production-scale, low-pressure metal organic chemical vapor deposition (MOCVD) reactor. The device structure is an isolated mesa with a wet-oxidized AlO_x aperture for both current and optical confinement. The device mesa was etched down to the semi-insulating substrate to minimize the parasitic capacitance. The wafer surface was subsequently passivated, planarized, and metallized. The backside of the substrate was lapped, polished, and antireflection (AR) coated. The AR coating prevents reflection of the laser emission from the air–substrate interface back into the VCSEL cavity, which may cause ripples in the light-current characteristics and increase noise. The VCSEL pad-out consists of isolated p- and n-pads for each element of the array.

The continuous-wave light-current-voltage characteristics of a 1 × 12 array at 25 °C with a 7.5-μm current aperture are shown in Fig. 2. The average threshold current and average threshold voltage is 434 μA and 1.34 V with a standard deviation of 11 μA and 0.005 V, respectively. The additional contribution from both the p- and n- DBR hetero-interfaces to the threshold voltage is only 0.14 V. The average external quantum efficiency is 40.4% near threshold, and the average series resistance is 100 Ω at 1.5 mW of optical output power. From S11 measurements, we estimate the bond-pad capacitance to be only 35 fF. A 10-Gb/s eye diagram, measured at 25 °C, is shown in

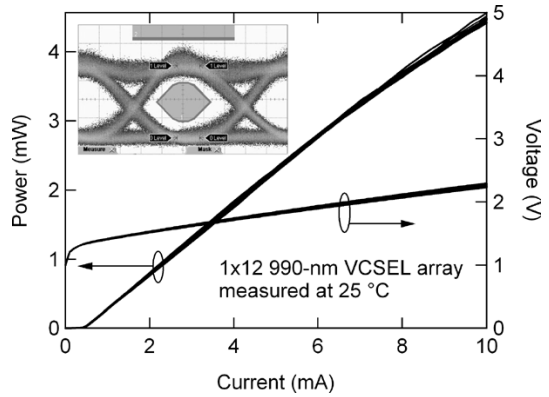

Fig. 2. Light-current-voltage measurements of a 1 × 12 990-nm VCSEL array with a 10-Gb/s eye diagram measured at 3-mA bias and ∼6-dB ER.

the inset of Fig. 2. The device was biased at an average current of 3 mA and modulated with a nonreturn-to-zero (NRZ) 2^7-1 pseudorandom bit sequence (PRBS) to achieve an extinction ratio (ER) of ∼6 dB. Using the 10-Gb Ethernet 9.953-Gb/s eye mask with a 10% mask margin, there were no hits in the eye mask margin after measuring 500 waveforms. A 2^7-1 PRBS is used since 8 B/10 B coding is typically used in data communications. Devices with a similar structure were measured for reliability and showed a predicted lifetime of >30 years at 80 °C.

C. Photodetectors

The p-i-n PD arrays used in POSH are designed to maintain a small capacitance at low bias voltage to enable low-power RX ICs. 2 × 12 arrays are constructed so that half of the PDs receive light from the link, and the others serve as bias points for the differential input of the RX IC front end.

The main features of the material structure are as follows: an Fe-doped semi-insulating InP substrate, a 1.0-μm Si-doped InP layer for an n^+ contact, a 1.8-μm background-doped InGaAs layer as the absorber layer (i-layer), a 1-μm n^- InP layer to facilitate low leakage, and, finally, a 0.2-μm n^- InGaAs layer for an ohmic p contact. The p^+ electrode in the semiconductor is created using zinc diffusion through the uppermost InGaAs and InP layers, which extends 0.1 μm into the InGaAs i-layer. The resulting InGaAs i-layer thickness is nominally 1.7 μm. Individual devices in the array have trenches etched around them through the n^+ contact layer to reduce crosstalk. Polyimide is used as passivation and to provide low capacitance support for the short trace from the top of the mesa to the p contact pad, which is on top of a column of undoped mesa material. The backside of the substrate was lapped, polished, and AR coated.

Arrays with a 34-μm active diameter are measured to have approximately 180-fF capacitance and open 10-Gb/s eye diagrams. 41-μm-diameter PDs with a modified structure have been designed, fabricated, and tested to have a capacitance of approximately 125 fF. No lifetime tests have been performed on these PDs.

VI. Microoptics

The POSH modules utilize low-cost double-sided polymer microoptics on a Pyrex substrate for both the TX and RX lens arrays. The TX lens array collects light emitted from the VCSEL

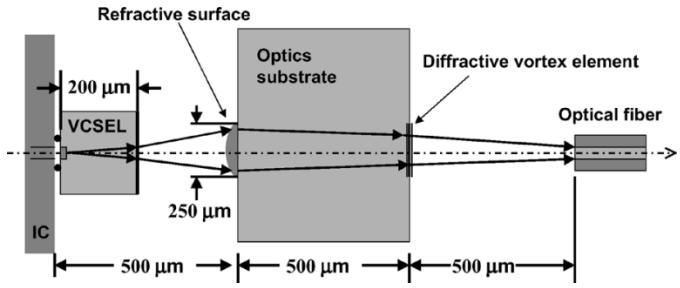

Fig. 3. Illustration of the transmitter optical system.

array and focuses this light onto a MMF ribbon. In turn, the RX lens array collects the light emitted out of the MMF ribbon and focuses it onto a PD array. Each module contains 12 identical parallel sets of optical elements. The TX uses a diffractive/refractive lens array, and the RX uses a refractive/refractive lens array. The TX optical system is illustrated in Fig. 3. A diffractive vortex element is used to minimize back reflection into the VCSEL (<0.01%) and to create a restricted-mode launch into the MMF, increasing the bandwidth–distance of the MMF [16]. A high-efficiency refractive surface is designed to achieve a throughput efficiency of ∼75%. The designed refractive surface is spherical in profile with diameter and lens height (sag) equal to 250 and 45 μm, respectively.

The RX geometry is similar to the TX geometry, with the diffractive element closest to the fiber replaced with a refractive lens. In addition, the distance from the IC to the optics substrate was reduced to 400 μm for the RX CME. Two refractive spherical surfaces are designed to enable high throughput efficiency of ∼95% for a 40-μm-diameter PD. This imaging system has a magnification factor of 0.6, allowing most of the light from the 50-μm-core MMF to be focused on to the PD. Since PDs are capable of accepting light at all angles, the spot-size reduction and corresponding increase in angular spread does not result in significant additional loss. The designed refractive surfaces for the RX are spherical in profile with lens heights of ∼ 35 μm.

Fabrication of the TX and RX lens arrays starts with a Pyrex (borosilicate glass) substrate, which has a well-matched thermal expansion coefficient to Si. In this application, Pyrex is used as a mechanical substrate and spherical lenses were fabricated using a droplet-dispensing process since Pyrex results in rough surfaces when etched [17]. One side of the Pyrex wafer is patterned with a metal layer, which creates both the contact layer for the CME seal and alignment fiducials for the optical elements. A hydrophobic surface is patterned to define circular apertures for the refractive lenses on the Pyrex surface. We used a piezoelectric droplet-dispensing unit to dispense small droplets of transparent UV-curable acrylate polymer, which produces lenses with sag up to 60 μm with a diameter of 200 μm. The diffractive optical element consists of eight different phase levels. The inverse phase profile is fabricated in a Si wafer using electron-beam (e-beam) lithography and RIE to create seven different etch depths. Arrays of the Si surface relief pattern are then cast into a thin film of UV-curable polymer on the Pyrex substrate. With careful alignment methods, we were able to control the sag of the lenses to within 0.5 μm of the designed sag with lens-to-lens uniformity better than 0.2 μm and 0.2-μm overlay registration.

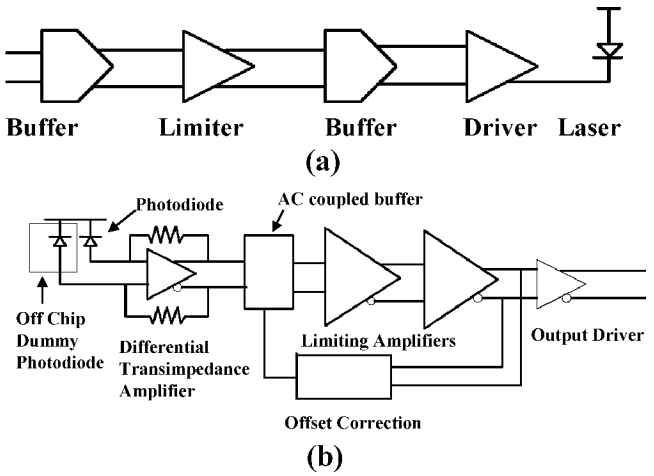

Fig. 4. Block diagram of the parallel-optics (a) transmitter and (b) receiver integrated circuits.

VII. Integrated Circuits

ICs for use in the POSH program have been designed to operate up to 10 Gb/s on 12 parallel channels. These circuits face stringent requirements in the areas of noise and crosstalk performance. These circuits have been designed in a standard Si–Ge BiCMOS process (i.e., a process that includes both CMOS and Si–Ge bipolar transistors) with a transition frequency (f_t) of 45 GHz. Both TX and RX circuits have been designed for a conventional 50-Ω electrical interface (100-Ω differential). The TX laser driver stage and RX input stage power supplies are separated into discrete supplies for each channel on the flexible circuit prior to delivery to the IC. The TX laser driver stage and RX input stage power supplies were designed as a distributed filter. The power supply busses, both on the IC and on the flexible circuit, were designed as controlled-impedance transmission lines. Shunt series resistance and capacitance elements were added on the IC and flexible circuit to complete the filter design. This power supply design resulted in low crosstalk penalties.

A. Transmitter

A block diagram of the TX circuit is shown in Fig. 4(a). The circuitry is maintained as symmetrical as possible to avoid the degradations caused by single-ended performance at high frequencies. The laser driver is a common differential output stage with the output connected directly to the n-side of the VCSEL. A set of diode-connected transistors is connected to the complementary output path to the laser. These serve the purpose of mimicking the laser behavior and sustaining symmetric current waveforms on the laser-driver supply. Output currents are designed to deliver a dc-bias current of 0–10 mA and a modulation current of 0–20 mA. This design uses a 3.3-V supply for the first three stages and a 3.3–5-V supply for the laser driver to accommodate the forward voltage of the VCSEL. With a 3.3-V supply on the laser driver, a forward voltage of 2.2 V may be accommodated. The 12-channel TX IC dissipates ∼1.5–2 W.

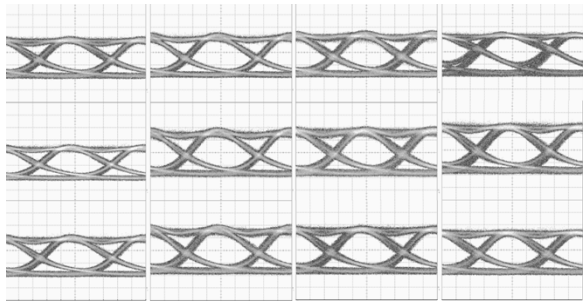

Fig. 5. POSH TX eye diagrams for all 12 channels at 10 Gb/s/ch with all channels operating simultaneously.

B. Receiver

A block diagram of the RX circuit is shown in Fig. 4(b). Minimization of crosstalk, noise, and jitter are the dominant challenges for a 10-Gb/s parallel RX circuit design. As shown in (2), the noise current of a typical RX front-end circuit can be derived [18] as:

$$i_{\rm eq}^2 = 2qi_b\Delta f + \frac{2qi_c\omega^2}{g_m^2}(C_{\rm pd}+C_\pi)^2\Delta f + 4kTR_b\omega^2C_{pd}^2\Delta f + \frac{4kT}{R_f}\Delta f \quad (2)$$

where $i_{\rm eq}$ is the input equivalent noise current, q is the electronic charge of an electron, i_b is the base current of the input transistors, i_c is the collector current of the input transistors, g_m is the transconductance of the input transistors, $C_{\rm pd}$ is the capacitance of the PD, ω is the angular frequency, C_π is the base emitter capacitance of the input transistor, Δf is the frequency range of the amplifier, k is Boltzman's constant, T is absolute temperature, R_b is the base resistance of the input pair, and R_f is the feedback resistance of the input stage.

For these circuits, the collector shot-noise term for the input pair tends to dominate. Base resistance noise and feedback resistor noise are also important. The best noise performance is obtained with the input differential pair operating well below f_t. The recommended f_t for multichannel TX and RX ICs operating at 10 Gb/s/ch is >75 GHz, where performance and power dissipation would both be improved.

Minimizing jitter requires isolating the channels as well as possible with channel stop diffusions, managing ground planes, and maximizing bandwidth. Parasitic capacitors between stages must be balanced to minimize jitter by avoiding mismatches in rise/fall times. A dummy photodiode is connected to the dark side of the input amplifier so that impedances are balanced. Separate biasing circuits are used in the three separate stages of the receive chain, and each of the three stages is bypassed on chip. The RX circuit in this paper uses three isolated 5-V supply voltages and dissipates ∼3.5 W.

VIII. Results

Fig. 5 shows measured optical eye diagrams at 10 Gb/s/ch of all 12 channels of a POSH TX module with all channels operating simultaneously and driven from independent NRZ 2^7-1 PRBS generators. A typical ER was 6.3 dB. Average optical power in each fiber was between −3.10 dBm and −4.67 dBm.

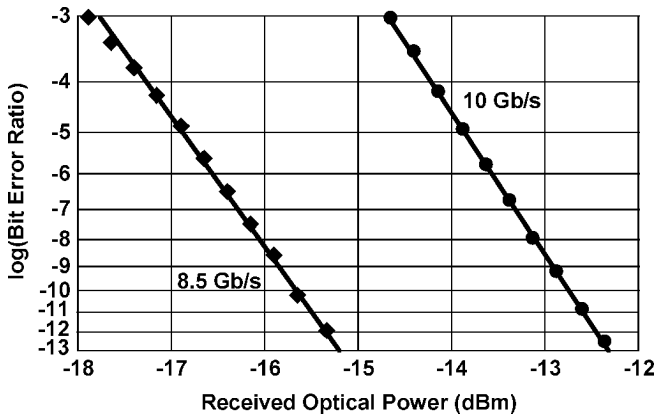

Fig. 6. Single-channel POSH RX BER measurements at 8.5 and 10 Gb/s with the RX optical power measured at the input to the PDs.

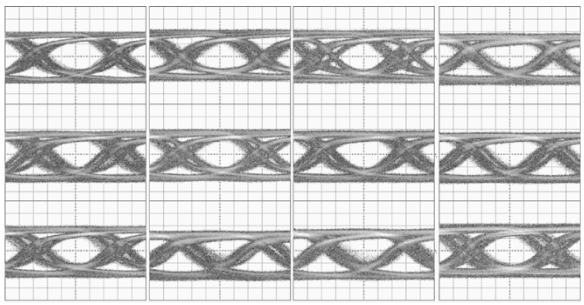

Fig. 7. Measured POSH RX eye diagrams for 12 channels at 8.5 Gb/s/ch after transmission through 100 m of standard 50-μm-core MMF ribbon with all channels operating simultaneously.

Typical rise and fall times were 36 and 84 ps, respectively. TX crosstalk power penalty was measured to be negligible.

Data rates up to 10 Gb/s/ch are demonstrated by a POSH RX module using 34-μm-diameter PDs. Fig. 6 shows a plot of the bit-error ratio (BER) versus RX optical power (measured at the PD) for single-channel operation at a data rate of 8.5 and 10 Gb/s while driven by a 990-nm VCSEL on a high-speed mount with an ER of 6 dB using a $2^7 - 1$ PRBS. The RX sensitivity (at the PD) for a BER of 10^{-12} is -15.3 dBm at 8.5 Gb/s and -12.4 dBm at 10 Gb/s. While some channels achieved open eyes at 10 Gb/s, open eyes on all 12 channels simultaneously at 10 Gb/s has not yet been demonstrated on the POSH RX module. Fig. 7 shows the measured eye diagrams at the output of a POSH RX after transmission through 100 m of standard 50MMF ribbon at 8.5 Gb/s/ch using the POSH TX module as the input to the link with all channels operating simultaneously using a $2^7 - 1$ PRBS. Therefore, an aggregate data rate of 102 Gb/s through 100 m of standard 50MMF ribbon was achieved. Fig. 8 shows a plot of BER versus RX optical power (into the lens array) for a POSH link with all channels operating and with only one channel operating showing that the RX crosstalk penalty is $\sim$1.3 dB. Fig. 9 shows a single-channel 10-Gb/s eye diagram at the output of a POSH link (TX and RX), including transmission through 100 m of standard 50MMF ribbon with all channels operating simultaneously at a data rate of 10 Gb/s using a $2^7 - 1$ PRBS. A BER $< 10^{-12}$ at 10 Gb/s and $< 10^{-13}$ at 8.5 Gb/s was measured on a single channel

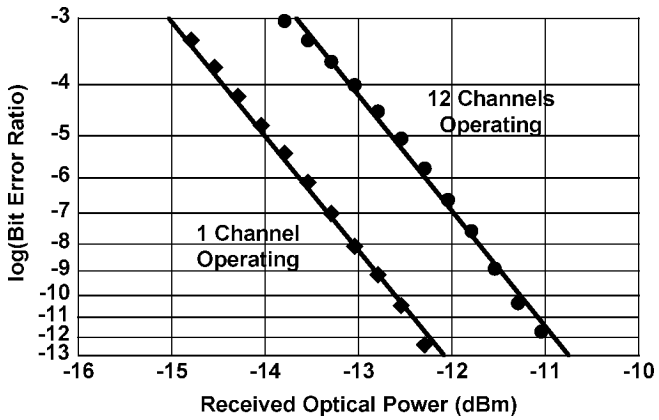

Fig. 8. BER measurements on a single channel of a POSH link at 8.5 Gb/s/ch after transmission through 100 m of standard 50-μm-core MMF ribbon with one channel versus 12 channels operating using a $2^7 - 1$ PRBS.

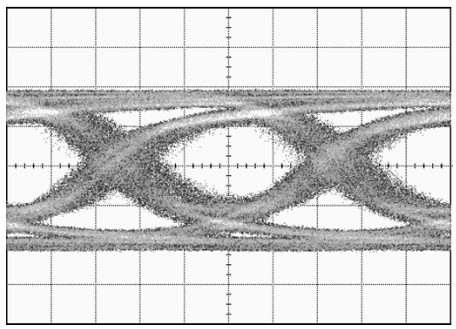

Fig. 9. 10-Gb/s eye diagram at the output of a POSH link after transmission through 100 m of standard 50-μm-core MMF ribbon with all channels operating simultaneously.

through this 12-channel link. Although all 12 channels are running simultaneously, we did not achieve open eyes on all 12 channels for a data rate of 10 Gb/s. In order to improve performance, a new version of the RX IC has been designed in a Si–Ge BiCMOS process with an f_t of 75 GHz.

IX. Conclusion

In conclusion, this paper has demonstrated 12-channel TX parallel-optic modules operating at 10 Gb/s/ch and RX parallel-optic modules operating at 8.5–10 Gb/s/ch. In a 12-channel parallel-optical interconnect, a BER $< 10^{-13}$ was measured on a single channel with all 12 channels operating simultaneously at a data rate of 8.5 Gb/s using a PRBS $2^7 - 1$ after transmission through 100 m of standard 50MMF ribbon. A parallel-optical interconnect with an aggregate data rate of 102 Gb/s was demonstrated. In addition, a BER $< 10^{-12}$ was measured on a single channel with all 12 channels operating simultaneously at a data rate of 10 Gb/s using a PRBS $2^7 - 1$ after transmission through 100 m of standard 50MMF ribbon.

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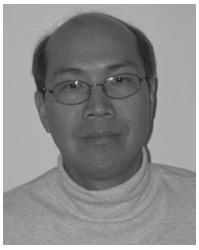

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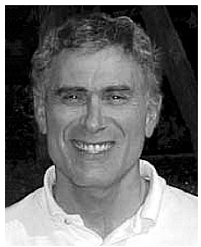

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