Parameter Design Oriented Analysis of the Current Control Stability of the Weak-Grid-Tied VSC

Guanglu Wu, Huadong Sun, *Senior Member, IEEE*, Xi Zhang, *Member, IEEE*, Agustí Egea-Àlvarez, *Member, IEEE*, Bing Zhao, Shiyun Xu, Shanshan Wang and Xiaoxin Zhou, *Fellow, IEEE*

Abstract—This paper studies the dynamic behaviors of weak-grid-tied VSCs with simplified transfer functions, which provides an accurate stability analysis and useful indications for tuning system parameters. A reduced-order multi-input multi-output (MIMO) transfer function that contains four single-input single-output (SISO) transfer functions for the weak-grid-tied VSC is first presented. It is found that the four SISO transfer functions share the same equivalent open-loop transfer function, i.e., the same stability conclusion. The Bode plots of the equivalent open-loop transfer function show that the inner current loop behaves as a band-pass filter whose maximum gain is approximately at the frequency of the PLL's bandwidth. By stability criterion, the harmonic amplification and instability occur when its maximum gain exceeds 0dB caused by high PLL's bandwidth, large grid impedance or high active power. It is also found that the target system is less stable when it works as an inverter than as a rectifier, due to the risk of the local positive feedback in the inverter mode. An effective criterion is further proposed to guide the selection of a proper PLL's bandwidth to ensure the stability of the VSC system. Simulation results validate the correctness of the analysis and the efficacy of the criterion.

Index Terms—Weak-grid-tied VSCs, MIMO transfer function, system parameter tuning, PLL's bandwidth, current control stability.

I. INTRODUCTION

THE increasing penetration of renewable energies and high voltage direct current transmission (HVDC) promotes the wide application of power electronics devices in the power system [1], [2]. Among various kinds of power electronics devices, the voltage-source converter (VSC) is the most commonly used. For example, almost all Photovoltaics (PVs) and direct-drive permanent magnet synchronous generators (PMSGs) for wind turbine applications are connected to the grid through VSCs [2].

Especially in China, the VSC-HVDC, whose two terminals are VSCs, has been widely used to interconnect AC grids and integrate large-scale renewable energy. That power electronics converters replacing traditional synchronous generators can decrease the strength of the grid, even resulting in weak grids [3], [4]. For instance, after the back-to-back VSC-HVDC

G. Wu, H. Sun, B. Zhao, S. Xu, S. Wang and X. Zhou are with State Key Laboratory of Power Grid Safety and Energy Conservation, China Electric Power Research Institute, Beijing, China, 100192.

X. Zhang is with the School of Automation and Key Laboratory for Intelligent Control and Decision on Complex Systems, Beijing Institute of Technology, Beijing 100081, China. (Email:xizhang@bit.edu.cn.)

A. Egea-Àlvarez is with Department of Electronic and Electrical Engineering, University of Strathclyde, 16 Richmond St, Glasgow G1 1XQ, U.K.

project (±420kV/1250MW) between Chongqing and Hubei province in China is put into operation, the minimum short circuit ratio (SCR) in Chongqing side can be decreased to 1.9 [5]. Weak grids can severely worsen the stability of the VSC system as well as bring great challenges to the control of the VSC [6]. The most commonly installed VSC converter is the two- and three-level used in wind and PV applications [7], [8], while the MMC-HVDC (modular multilevel converter based HVDC) converter is widely used in high voltage direct current transmission applications.

The stability analysis of weak-grid-tied VSCs has drawn much attention from both academic researchers and industrial engineers. Several models have been proposed for analyzing the small-signal stability of this system, including the impedance-based methods [9]–[14], the complex-torque-based method [15]–[17] and the eigenvalue analysis [3], [4], [18], [19]. It is reported that the impacts of the inner current loop and the outer loop on the small-signal stability of the VSC can be investigated separately, due to different time scales [17]. The outer loop of the VSC provides d and q current references for the inner loop, where one component is related to the AC active power control or DC voltage control and the other is related to the AC voltage or reactive power control [3], [4]. Following standard cascaded control tuning methodologies, the outer loops are designed much slower than the inner loop [20]. Thus, the current control stability is a precondition of the system stability for the design of the outer loops. In other words, the inner current loop's small-signal stability is a necessary condition for the small-signal stability of the overall system.

The phase-locked loop (PLL) plays an important role in determining the inner current loop's stability of the weak-grid-tied VSC according to [13], [15], [16]. From the viewpoint of impedance characteristics, the grid-tied inverter's impedance with the current control and the PLL was investigated in [13]. And it shows that a higher PLL bandwidth yields a wider frequency range of negative resistance behavior, which will deteriorate the small-signal stability. From the viewpoint of damping, eigenvalue analysis and complex torque analysis of the weak-grid-tied inverter with the current control and the PLL were carried out during deep voltage sag in [15], [16]. And it shows that the increase of PLL's bandwidth can decrease the total damping and deteriorate the small-signal stability. These methods are well applied for analyzing the stability considering the PLL and the current control, but are limited for providing more insights into the PLL's impacts on the stability from the viewpoint of classical control theory.

The transfer function is one classical method to investigate the stability of the weak-grid-tied voltage source converter
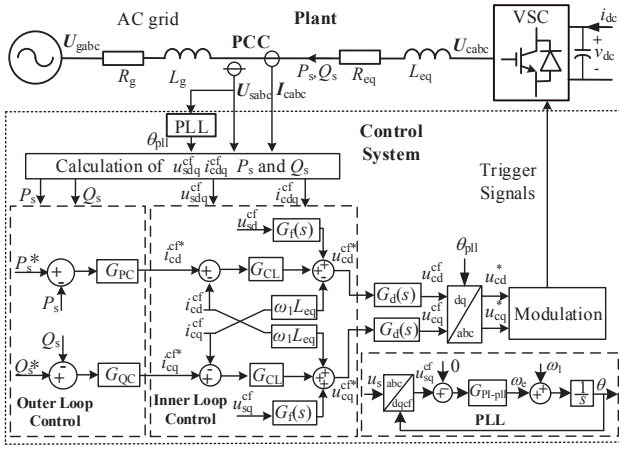
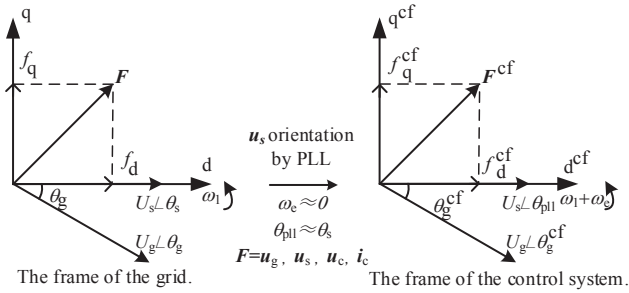Fig. 1.   The schematic of the weak-grid-tied two-level converter system.

Fig. 2.   The frames of the grid and the control system.

(VSC). However, its application is limited by the high dimension and complexity of the real system [6], [21], [22]. To overcome these limitations, the transfer function should be carefully simplified with appropriate dimension reduction methods. Then, the classical transfer function's advantages of explicitly displaying the influences of each part of the system on its stability and straightly guiding the parameter design and improvements can be well taken.

The rest of the paper is organized as follows. In Section II, a simplified MIMO transfer function of the VSC system is obtained by neglecting the high-frequency components like time delays and the voltage filters. A same equivalent open-loop transfer function for each input-output pair is obtained and used to indicate the stability. In Section III, the PLL's effect as a high-pass filter is revealed on the Bode plots of the open-loop transfer function. Its impacts on the stability of the inner current loop and the physical understandings are discussed. In Section IV, simulation results are presented to validate the proposed method. A criterion that guides the selection of the proper bandwidth for the PLL is provided to ensure the small-signal stability of the inner current loop of the target system in Section V.

II. REDUCED-ORDER MIMO TRANSFER FUNCTION

In this section, the transfer function of the target system is derived and properly simplified with reasonable assumptions. Fig. 1 shows the schematic of the typical scenario, where a VSC is connected to a weak power grid. The plant in Fig. 1 refers to the main circuit that is composed by the weak

grid and the electrical components of the VSC. The converter controller is composed by a current control and a PLL. The PLL provides the synchronization with the grid, the inner loop controls the active and reactive current through the converter line reactor. And u_g, u_s, u_c are the voltage phasers of the grid, the PCC (point of common coupling) and the VSC, i_c is the phaser of the current injecting to the grid. One can refer to the Appendix for the mathematical descriptions for the physical part and control part of the target system.

A. Model Linearization

The mapping relations of one small perturbation in the two different frames shown in Fig. 2 can be described by

$$
\begin{bmatrix} \Delta f_d \\ \Delta f_q \end{bmatrix} = T_{dqcf2dq0} \begin{bmatrix} \Delta f_d^{cf} \\ \Delta f_q^{cf} \\ \Delta \theta_{pll} \end{bmatrix}, \begin{bmatrix} \Delta f_d^{cf} \\ \Delta f_q^{cf} \end{bmatrix} = T_{dq2dqcf0} \begin{bmatrix} \Delta f_d \\ \Delta f_q \\ \Delta \theta_{pll} \end{bmatrix},
\tag{1}
$$

where f denotes u_s, u_c, u_g or i_c, the superscript "cf" denotes that the variable is in the the control system's dq frame, θ_{pll} is the initial phase of the PCC voltage observed by PLL, the ω_1 in Fig. 2 is $2\pi 50$rad/s, and the matrix of $T_{dqcf2dq0}$ and $T_{dq2dqcf0}$ are as follows,

$$
T_{dqcf2dq0} = \begin{bmatrix} 1 & 0 & -f_{q0}^{cf} \\ 0 & 1 & f_{d0}^{cf} \end{bmatrix}, T_{dq2dqcf0} = \begin{bmatrix} 1 & 0 & f_{q0} \\ 0 & 1 & -f_{d0} \end{bmatrix}.
\tag{2}
$$

Fig. 3(a) shows the linearized model of each component of the inner current loop of the target system. Specifically, the linearized representation of the plant can be written as

$$
\begin{cases} sL_g\Delta i_{cd} = -R_g\Delta i_{cd} + \omega_1 L_g\Delta i_{cq} + \Delta u_{sd} - \Delta u_{gd} \\ sL_g\Delta i_{cq} = -\omega_1 L_g\Delta i_{cd} - R_g\Delta i_{cq} + \Delta u_{sq} - \Delta u_{gq} \end{cases},
\tag{3}
$$

$$
\begin{cases} sL_{eq}\Delta i_{cd} = -R_{eq}\Delta i_{cd} + \omega_1 L_{eq}\Delta i_{cq} + \Delta u_{cd} - \Delta u_{sd} \\ sL_{eq}\Delta i_{cq} = -\omega_1 L_{eq}\Delta i_{cd} - R_{eq}\Delta i_{cq} + \Delta u_{cq} - \Delta u_{sq} \end{cases},
\tag{4}
$$

where s is the Laplace variable, and the subscripts d and q indicate d- and q-axis components of a variable in the grid's dq frame; i_c is the current across the PCC; u_s is the PCC voltage; u_g is the voltage of the equivalent grid voltage source; u_c is the output voltage of the VSC; R_g and L_g are the equivalent resistance and inductance of the AC grid, respectively; R_{eq} and L_{eq} are the equivalent resistance and inductance between the VSC and the PCC, respectively.

The linearized representation of the PLL can be written as $\Delta\theta_{pll} = G_{pll}\Delta u_{sq}$, where G_{pll} is the transfer function of the PLL and can be represented as

$$
G_{pll} = \frac{\left(2\xi\omega_{pll}s + \omega_{pll}^2\right)/u_{sd0}}{s^2 + 2\xi\omega_{pll}s + \omega_{pll}^2},
\tag{5}
$$

where ξ is the damping ratio, ω_{pll} is the bandwidth of the PLL, and the subscript 0 denotes steady-state values. Combing $\Delta u_{gd} = 0$, $\Delta u_{gq} = 0$ and (3), the final linear representation of the PLL can be described as

$$
\Delta\theta_{pll} = G_{pll}\left[\omega_1 L_g\Delta i_{cd} + (sL_g + R_g)\Delta i_{cq}\right].
\tag{6}
$$

By substituting the linear representations of the current control and the PLL into that of the plant in (4), the small-signal current outputs of Δi_{cd}, Δi_{cq} can be presented as the
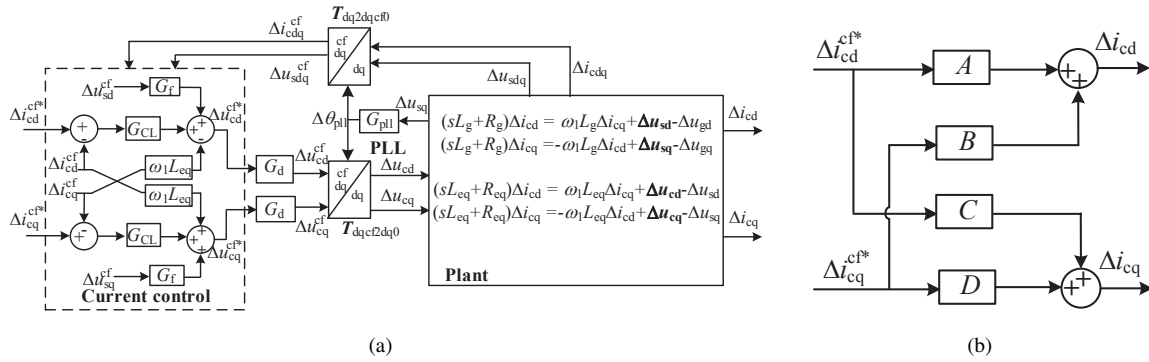
Fig. 3. (a): The linearized representation of the inner current loop. (b): The simple small-signal block diagram of the inner current loop.
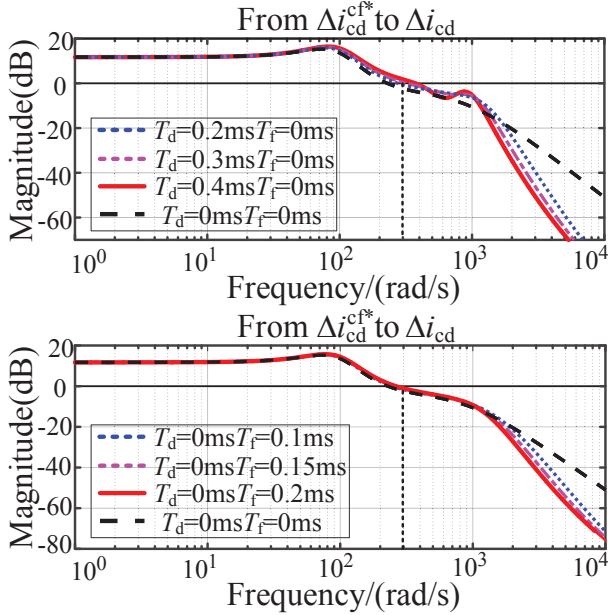

Fig. 4. Magnitude response of the system with different time delays and measurement filters.

Fig. 5. Magnitude-frequency responses of the outer active power loop.

functions of other small-signals including Δu_{sd}, Δu_{sq}, Δi_{cd}, Δi_{cq}, Δi_{cd}^{cf*}, Δi_{cq}^{cf*}, $\Delta \theta_{pll}$ and Δv_{dc}, which is explicitly shown in (7). Equation (7) is too complicated and further proper simplifications should be carried out for effective analysis.

B. Impact of the Time Delays and Measurement Filters

To study the impact of the time delays and the measurement filters, the magnitude responses with different time delays and measurement filters are compared, as shown in Fig. 4. The other parameters are presented in Table I. It can be seen that the time delays and the measurement filters mainly play a role in the high-frequency range $\omega > 1500$rad/s (200Hz), which is much higher than the cut-off frequency of the inner current loop (about 300rad/s) and the bandwidth of the PLL (around 10Hz). The high frequency stability issues also exist in the weak-grid-tied VSC, however it is out of the scope of this paper which focuses on the medium-frequency stability.

C. Impact of the Outer Loop

Fig. 5 shows the magnitude response of the outer loop of the active power control, where the cut-off frequency of outer loop
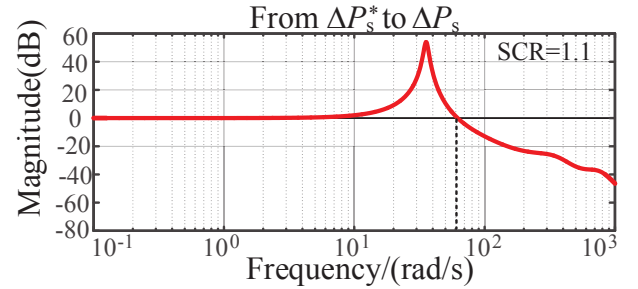
is around 60rad/s. Fig. 4 shows that the cut-off frequency of the inner loop is around 300rad/s. It can be seen that the outer loop is much slower than the current loop. Thus, it is reasonable to simply the outer loop when analyzing the stability for the medium frequency ranges.

D. Reduced-order MIMO Transfer Function

To obtain the reduced-order as well as valid MIMO transfer function of the inner loop, the following reasonable assumptions are adopted.

1) The time delay usually plays a role in high frequency stability issues [23], but this paper focuses on the medium frequency stability. For the sake of simplifying, the delays of the control system, voltage modulation and the voltage measurement filter are neglected, thus $G_d=1$, $G_f=1$.

2) The perturbation of the voltage on the DC side is small enough to be neglected, i.e., $\Delta v_{dc}=0$.

TABLE I
PARAMETERS OF THE TEST CASE IN MODEL VALIDATION

Parameters	Unit	Value
Rated/Base power	MW	1500
Rated/Base voltage	kV	525
Rated frequency	Hz	50
SCR	1	1.1
R_g, L_g	Ω, mH	1.67, 531.7
R_{eq}, L_{eq}	Ω, mH	0.58, 184.8
ξ	1	0.707
ω_{pll}, k_{p_pll}, T_{i_pll}	Hz, rad/(V·s), s	16, 3.32×10^{-4}, 0.0141
ω_{CL}, k_{p_cl}, T_{i_cl}	Hz, V/A, s	125, 145.16, 0.3183
ω_{OL_PC},k_{p_PC},k_{i_PC}	Hz, A/W, A/(Ws)	6, 3.56×10^{-7}, 2.80×10^{-4}
ω_{OL_QC},k_{p_QC},k_{i_QC}	Hz, A/W, A/(Ws)	6, 3.56×10^{-7}, 2.80×10^{-4}
P_s,Q_s	p.u.	1, 0.8

$$
\begin{bmatrix} \Delta i_{cd} \\ \Delta i_{cq} \end{bmatrix}^T = \begin{bmatrix} \Delta i_{cd}^{cf*} \\ \Delta i_{cq}^{cf*} \end{bmatrix}^T \begin{bmatrix} \frac{G_d G_{CL}}{sL_{eq}+R_{eq}+G_d G_{CL}} & 0 \\ 0 & \frac{G_d G_{CL}}{sL_{eq}+R_{eq}+G_d G_{CL}} \end{bmatrix} + \begin{bmatrix} \Delta u_{sd} \\ \Delta u_{sq} \\ \Delta i_{cd} \\ \Delta i_{cq} \\ \Delta \theta_{pll} \\ \Delta v_{dc} \end{bmatrix}^T \begin{bmatrix} \frac{(G_d G_f - 1)}{sL_{eq}+R_{eq}+G_d G_{CL}} & 0 \\ 0 & \frac{(G_d G_f - 1)}{sL_{eq}+R_{eq}+G_d G_{CL}} \\ 0 & \frac{(G_d - 1)\omega_1 L_{eq}}{sL_{eq}+R_{eq}+G_d G_{CL}} \\ \frac{(1-G_d)\omega_1 L_{eq}}{sL_{eq}+R_{eq}+G_d G_{CL}} & 0 \\ \frac{G_d[G_f u_{sq0}-G_{CL}I_{cq0}+\omega_1 L_{eq}i_{cd0}]-u_{cq0}}{sL_{eq}+R_{eq}+G_d G_{CL}} & \frac{G_d[-G_f u_{sd0}+G_{CL}i_{cd0}+\omega_1 L_{eq}i_{cq0}]+u_{cd0}}{sL_{eq}+R_{eq}+G_d G_{CL}} \\ \frac{u_{cd0}}{(sL_{eq}+R_{eq}+G_d G_{CL})v_{dc0}} & \frac{u_{cq0}}{(sL_{eq}+R_{eq}+G_d G_{CL})v_{dc0}} \end{bmatrix}
\tag{7}
$$

$$
\begin{bmatrix} \Delta i_{cd} \\ \Delta i_{cq} \end{bmatrix} = \begin{bmatrix} \frac{G_{CL}}{Z_{ic}} & 0 \\ 0 & \frac{G_{CL}}{Z_{ic}} \end{bmatrix} \begin{bmatrix} \Delta i_{cd}^{cf*} \\ \Delta i_{cq}^{cf*} \end{bmatrix} + \begin{bmatrix} -\frac{[G_{CL}+R_{eq}]i_{cq0}}{Z_{ic}}G_{pll}\omega_1 L_g & -\frac{[G_{CL}+R_{eq}]i_{cq0}}{Z_{ic}}G_{pll}(sL_g + R_g) \\ \frac{[G_{CL}+R_{eq}]i_{cd0}}{Z_{ic}}G_{pll}\omega_1 L_g & \frac{[G_{CL}+R_{eq}]i_{cd0}}{Z_{ic}}G_{pll}(sL_g + R_g) \end{bmatrix} \begin{bmatrix} \Delta i_{cd} \\ \Delta i_{cq} \end{bmatrix}
\tag{8}
$$

By substituting $G_d=1$, $G_f=1$, $\Delta v_{dc}=0$ and (6) into (7), we get a simplified MIMO linearized mathematical representation of (7) as shown in (8), where $Z_{ic}=sL_{eq}+R_{eq}+G_{CL}$, and G_{CL} is the PI controller in the current control. Based on (8), the reduced-order MIMO transfer function with Δi_{cd}^{cf*}, Δi_{cq}^{cf*} as inputs and Δi_{cd}, Δi_{cq} as outputs, can be obtained as

$$
\begin{bmatrix} \Delta i_{cd} \\ \Delta i_{cq} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} \Delta i_{cd}^{cf*} \\ \Delta i_{cq}^{cf*} \end{bmatrix}.
\tag{9}
$$

Fig. 3(b) shows a simplified block diagram of the inner current loop according to (9). And the A, B, C and D in (9) can be represented as

$$
\begin{cases} A = \frac{G_{CL}}{Z_{ic}}\frac{1-G_{qq}}{1+G_{dd}-G_{qq}}, B = \frac{G_{CL}}{Z_{ic}}\frac{-G_{dq}}{1+G_{dd}-G_{qq}} \\ C = \frac{G_{CL}}{Z_{ic}}\frac{G_{qd}}{1+G_{dd}-G_{qq}}, D = \frac{G_{CL}}{Z_{ic}}\frac{1+G_{dd}}{1+G_{dd}-G_{qq}} \end{cases},
\tag{10}
$$

where G_{dd}, G_{dq}, G_{qd} and G_{qq} can be written as

$$
\begin{cases} G_{dd} = \frac{G_{CL}}{Z_{ic}}G_{pll}\omega_1 L_g i_{cq0}, G_{dq} = \frac{G_{CL}}{Z_{ic}}G_{pll}(sL_g + R_g)i_{cq0} \\ G_{qd} = \frac{G_{CL}}{Z_{ic}}G_{pll}\omega_1 L_g i_{cd0}, G_{qq} = \frac{G_{CL}}{Z_{ic}}G_{pll}(sL_g + R_g)i_{cd0} \end{cases}.
\tag{11}
$$

And according to (26), G_{CL}/Z_{ic} in (10) and (11) is written as

$$
\frac{G_{CL}}{Z_{ic}} = \frac{\omega_{CL}\left(L_{eq}+\frac{R_{eq}}{s}\right)}{sL_{eq}+R_{eq}+\omega_{CL}\left(L_{eq}+\frac{R_{eq}}{s}\right)} = \frac{1}{(s/\omega_{CL}+1)},
\tag{12}
$$

which is a first-order lag with a time constant of $1/\omega_{CL}$, and ω_{CL} is the bandwidth of the inner loop.

E. Equivalent Open Loop Transfer Function

The MIMO transfer function (9) is stable if and only if all elements in the transfer function matrix are stable. As shown in (10), each A, B, C and D has two multiplying terms: the first term on the right hand side of each equation of (10) is G_{CL}/Z_{ic}, which is a common term; the second term on the right hand side of each equation of (10) has the same denominator $(1+G_{dd}-G_{qq})$. From (12), G_{CL}/Z_{ic} is table as it has a negative root $-\omega_{CL}$. Thus, the stability of the current loop depends on the second terms of A, B, C and D.

By linear control theory, the second terms of A, B, C, and D are stable if and only if all the poles of each second term are on the left half plane (LHP). Also, as the denominators of G_{dd}, G_{qq}, G_{dq} and G_{qd} are the same according to (11), the second terms of A, B, C, and D have the same characteristic equation $1+G_{dd}-G_{qq} = 0$. In other words, they have the same poles.

From the above analysis, we draw the conclusion that the small-signal stability of the inner loop of the VSC can be transformed to computing the roots of the characteristic equation $1 + G_{dd} - G_{qq} = 0$. Furthermore, the complex root computation can be replaced by the analysis on the Bode plots of $G_{dd}-G_{qq}$, which is quite mature in classical control theory. Therefore, we define $G_0 = G_{dd} - G_{qq}$ as the equivalent open-loop transfer function that can be expressed as

$$
G_0 = \frac{G_{CL}}{Z_{ic}}G_{pll}\left[\omega_1 L_g i_{cq0} - (sL_g + R_g)i_{cd0}\right].
\tag{13}
$$

When $i_{cd0} \neq 0$ and $R_g = 0$, (13) can be rewritten as

$$
G_0 = \frac{G_{CL}}{Z_{ic}}G_{pll}\left[-L_g i_{cd0}\left(s + \frac{-\omega_1 i_{cq0}}{i_{cd0}}\right)\right](i_{cd0} \neq 0).
\tag{14}
$$

Then, in the condition that $i_{cq0}=0$ (unit power factor), by substituting (5) and (12) into (14), the equivalent open loop transfer function G_0 in the form of the multiplication of factors can be obtained as

$$
G_0 = \frac{-L_g i_{cd0}s\left[1 + s\left(2\xi/\omega_{pll}\right)\right]}{u_{sd0}(1 + s/\omega_{CL})\left[1 + s\left(2\xi/\omega_{pll}\right) + s^2/\omega_{pll}^2\right]}.
\tag{15}
$$

Equation (15) has five factors including one proportional factor, one differential factor, one first-order lead factor, one first-order lag factor and one second-order lag factor.

III. PLL's High-pass Filter Effect in Weak-grid-tied VSCs and Stability Analysis

In this section, the PLL's effect as a high-pass filter in the weak-grid-tied VSC is revealed and the current control stability of the weak-grid-tied VSC is investigated based on the equivalent open-loop transfer function obtained.

TABLE II
THE CHARACTERISTICS OF EACH FACTOR IN G_0 ($i_{cq0}=0$, $i_{cd0}>0$)

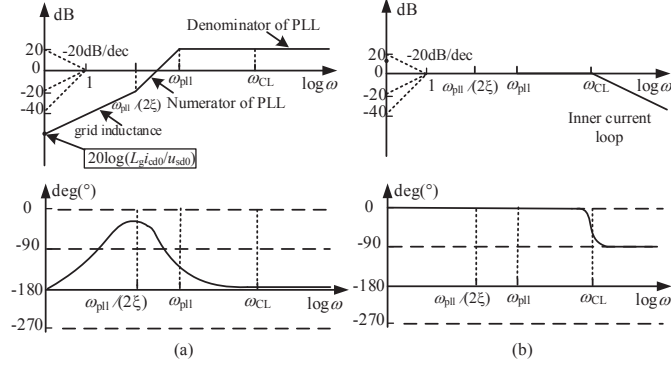| No.	Factor	Corner frequency (rad/s)	Gain slope (dB/dec)	Phase (deg)	Cumulative slope (dB/dec)	Cumulative phase (deg)
1	$-L_g i_{cd0}/u_{sd0}$	—-	0	-180	0	-180
2	s	—-	+20	90	+20	-90
3	$1+2s\xi/\omega_{pll}$	$\omega_{pll}/(2\xi)$	+20	90	+40	0
4	$(1+2s\xi/\omega_{pll}+s^2/\omega_{pll}^2)^{-1}$	ω_{pll}	-40	-180	0	-180
5	$(1+s/\omega_{CL})^{-1}$	ω_{CL}	-20	-90	-20	-270

Fig. 6. (a): The PLL's high-pass filter effect in weak-grid condition.(b): The current control's low-pass filter effect.

Fig. 7. The band-pass filter effect of G_0 in inverter mode ($i_{cd0}>0$, $i_{cq0}=0$).

Fig. 8. Impacts of different factors on the band-pass filter effect of G_0 in inverter mode ($i_{cd0}>0$, $i_{cq0}=0$).

A. PLL's High-pass Filter Effect in Weak-grid-tied VSCs

The corner frequency, the gain slope and the phase of each factor at its corner frequency in (15) are listed in Table II and sorted by their corner frequency when the VSC works as an inverter that injects active power to the AC power grid with $i_{cd0}>0$. And the cumulative gain slope and phase at each corner frequency are also obtained. Based on Table II, the Bode plots of the equivalent open loop transfer function can be drawn by hand. According to (15) and Table II, four factors' corner frequencies are below the frequency of the PLL's bandwidth and they are listed as follows.

1) $-L_g i_{cd0}/u_{sd0}$ is the proportional factor, in which the e-quivalent grid inductance L_g indicates the AC system strength, and the active power current i_{cd0} represents the active power injected to the grid. This proportional factor contributes a value added to the amplitude-frequency curve of G_0 for the entire frequency range $(0,\infty)$.

2) The differential factor s contributes a 20dB/dec gain slope for the entire frequency range $(0,\infty)$.

3) The first-order lead factor $(1+2s\xi/\omega_{pll})$ comes from the numerator of G_{pll} and contributes a 20dB/dec gain slope in the frequency range $(\omega_{pll}/(2\xi),\infty)$. Thus, the cumulative gain slope becomes 40dB/dec at $\omega=\omega_{pll}/(2\xi)$.

4) The second-order lag factor $(1+2s\xi/\omega_{pll}+s^2/\omega_{pll}^2)^{-1}$ comes from the denominator of G_{pll} and contributes a -40dB/dec gain slope in the frequency range (ω_{pll},∞). Thus, the cumulative gain slope becomes 0dB/dec at $\omega=\omega_{pll}$, which means that the largest value of G_0's gain appears at $\omega=\omega_{pll}$ and a larger ω_{pll} results in a larger gain at $\omega=\omega_{pll}$. Obviously, a larger L_g or i_{cd0} also means a larger gain at the frequency $\omega=\omega_{pll}$.

Fig. 6(a) shows the Bode plots of G_0 considering the PLL, the grid impedance, and the active power. It shows that the
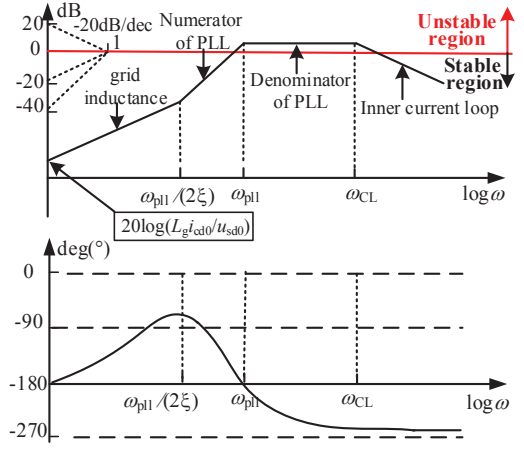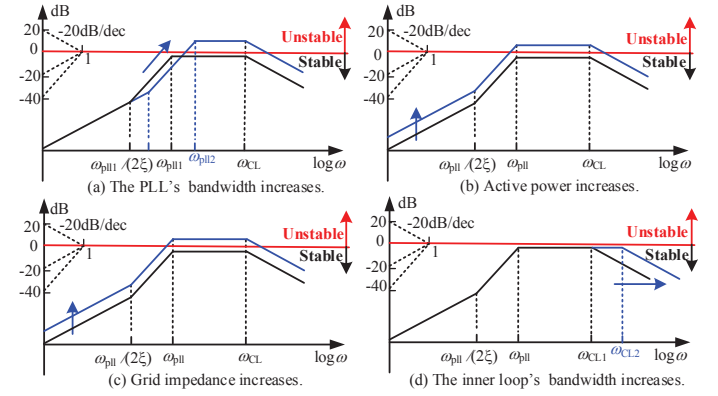
PLL can behave as a high-pass filter in the weak-grid-tied VSC when $-\mathrm{Lm}\left|G_0\left(j\omega_{pll}\right)\right|>-3$dB, which will let the high frequency harmonics pass.

B. Total Band-pass Filter Effect and Stability Analysis

The first-order lag factor $(1+s/\omega_{CL})^{-1}$ stems from the current control and contributes a -20dB/dec gain slope in the frequency range (ω_{CL},∞). Thus, the current control behaves as a low-pass filter as shown in Fig. 6(b). And the cumulative gain slope becomes -20dB/dec in the frequency range (ω_{CL},∞) due to the current control. Therefore, the equivalent open-loop transfer function of the weak-grid-tied VSC can behave as a band-pass filter as shown in Fig. 7. From the Bode plots in Fig. 7, we can see that the amplitude-frequency curve begins to decline after the frequency reaches the current control's bandwidth.

The stability criterion based on the Bode plots is

$$k_g=-\mathrm{Lm}\left|G_0\left(j\omega_g\right)\right|>0, \qquad (16)$$

where ω_g is the phase-crossover frequency, and k_g is the gain margin at ω_g. By the stability criterion (16), the inner current loop is stable if and only if G_0's gain at the phase-crossover frequency is smaller than 0dB. According to Table II, G_0's phase-crossover frequency approximately equals to the PLL's bandwidth ω_{pll}, as the cumulative phase equals to 180° at ω_{pll}.

Thus, the impact of each factor on the current control stability can be transformed to investigating how each factor in G_0 impacts the gain at the phase-crossover frequency $\omega = \omega_{pll}$. The detailed analysis on the impacts of each factor as well as their corresponding physical meanings on the small-signal stability of the current control are listed as follows.

1) Fig. 8(a)-Fig. 8(c) show that, a larger L_g, $i_{cd0}(i_{cd0} > 0)$, or PLL's bandwidth ω_{pll} can all result in a larger value of G_0's gain at the phase-crossover frequency ω_{pll}, thus decreasing the gain margin. Because the largest value of G_0's gain appears at the phase-crossover frequency $\omega = \omega_{pll}$ as shown in Fig. 7. And the gain margin is defined as the amplitude difference between the 0dB line and the amplitude-frequency line of G_0 at ω_{pll}, i.e., $0dB - 20\log|G_0(\omega = \omega_{pll})|dB$.

2) Fig. 8(d) presents that the current control doesn't have impact on the maximum value of the magnitude response, i.e., the current control stability of the VSC system. One important function of the current control is to suppress the high-frequency harmonics. As a general rule-of-thumb, its bandwidth is chosen to be 0.1 to 0.2 times of the power converter switching frequency [4]. As the PLL is usually designed to be much slower than the current control to avoid control resonance and provide enough time for current damping in engineering practice. Thus, $\omega_{pll} < \omega_{CL}$ is satisfied, Therefore, the inner loop current control's bandwidth doesn't change $20\log|G_0(\omega = \omega_{pll})|dB$, and doesn't impact the current control stability.

3) The current control always has a positive stability margin when the VSC works as a rectifier ($i_{cd0} < 0$). Because the phase of the proportional factor is $0°$ and the Bode phase-frequency curve of G_0 doesn't have any intersection points with the line of $-180°$ when $i_{cd0} < 0$. Thus,the phase of G_0 is always in the range of $(-90°, 90°)$ and there is no phase-crossover frequency on G_0's Bode plots when $i_{cd0} < 0$. However, the phase of the proportional factor is $-180°$ when $i_{cd0} > 0$ and there is a phase-crossover frequency on G_0's Bode plots. Once the gain margin is negative, there is a risk of the local positive feedback in the inverter mode.

C. Physical Understandings of the PLL's High-pass Filter Effect

Fig. 9 presents the small-signal block diagram of the current control of the weak-grid-tied VSC according to equation (8). It shows that there are four feedback loops in the weak-grid-tied VSC, where feedback loops 1 and 2 are the d and q current feedback control, feedback loops 3 and 4 are introduced by the voltage drop on the grid impedance through the PLL. In strong-grid conditions, $L_g \approx 0$, $R_g \approx 0$, feedback loop 3 and 4 disappear. However, in weak-grid condition, $L_g \approx 0$ doesn't satisfy, and feedback loop 3 and 4 exist.

In weak-grid condition, the d-axis and q-axis current controls are tightly coupled because of the large grid impedance, see loop 3 and 4. In loop 4, the grid inductance can amplify the disturbance, the current control suppresses the disturbance, the PLL's denominator suppresses and PLL's numerator amplifies the disturbance. If the disturbance suppression effect is smaller than the disturbance amplification effect, the harmonics in the
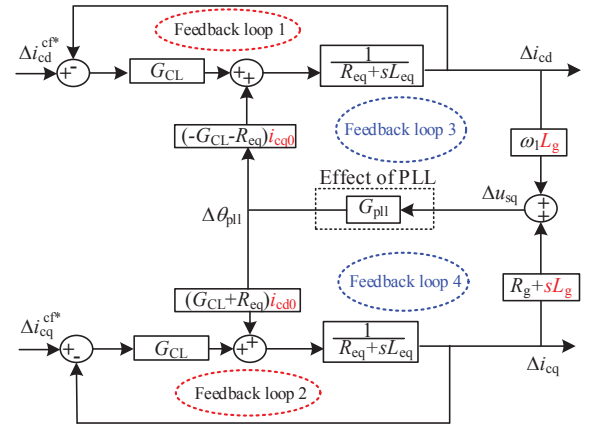

Fig. 9. Four feedback loops in the weak-grid-tied VSC.

q-axis current disturbance can be amplified by the feedback loop 4. And the PLL's high-pass dynamics emerges. The large grid inductance is the main factor that can lead to the PLL's high-pass dynamics. Theoretically, a larger grid inductance (L_g) in feedback loop 4 can move the gain-frequency curve in Fig. 8(c) upward till above 0dB, which results in the high-pass filter effect of the PLL.

D. Impact of the Reactive Current

In Section III-B, it is assumed that $i_{cq0}=0$ (unit power factor). When $i_{cq0} \neq 0$, by substituting (5) and (12) into (14), the equivalent open loop transfer function G_0 in the form of the multiplication of factors can be obtained as

$$G_0 = \frac{\omega_1 L_g i_{cq0}\left[1 + s\left(i_{cd0}/(-\omega_1 i_{cq0})\right)\right]\left[1 + s\left(2\xi/\omega_{pll}\right)\right]}{u_{sd0}\left(1 + s/\omega_{CL}\right)\left[1 + s\left(2\xi/\omega_{pll}\right) + s^2/\omega_{pll}^2\right]}. \quad (17)$$

Equation (17) also has five factors including one proportional factor, two first-order lead factor, one first-order lag factor and one second-order lag factor.

The Bode plots of G_0 when ($i_{cq0} \neq 0$) can also be drawn according to (17). Differing from (15), the proportional factor in (15) is replaced by a first-order lead factor in (17) with a corner frequency of $(-\omega_1 i_{cq0}/i_{cd0})$. The value of $(-\omega_1 i_{cq0}/i_{cd0})$ depends on i_{cd0} and i_{cq0}, and has three cases of below $\omega_{pll}/(2\xi)$, above ω_{pll}, or in the interval of $[\omega_{pll}/(2\xi), \omega_{pll}]$. For the three cases, Table III, Table IV and Table V present the corner frequency, the gain slope and the phase of the factors in G_0 at its corner frequency, and is sorted by their corner frequency. And the cumulative gain slope and phase at each corner frequency are also presented. The Bode plots of G_0 is presented in Fig. 10 when $(-\omega_1 i_{cq0}/i_{cd0})$ is below $\omega_{pll}/(2\xi)$, above ω_{pll}.

When $[(-\omega_1 i_{cq0}/i_{cd0}) < \omega_{pll}/(2\xi)]$ and $[\omega_{pll}/(2\xi) < (-\omega_1 i_{cq0}/i_{cd0}) < \omega_{pll}]$, Table III and Table IV show that the maximum gain of G_0 is also approximately at the frequency of the PLL's bandwidth . When $[(-\omega_1 i_{cq0}/i_{cd0}) > \omega_{pll}]$, Table V shows that the maximum gain of G_0 is in the interval of $[\omega_{pll}/(2\xi), \omega_{pll}]$, which is near PLL's bandwidth. Thus, the Bode plots of G_0 presented in Fig. 10 when ($i_{cq0} \neq 0$) have a similar form as Fig. 7. Impacts of different factors on the
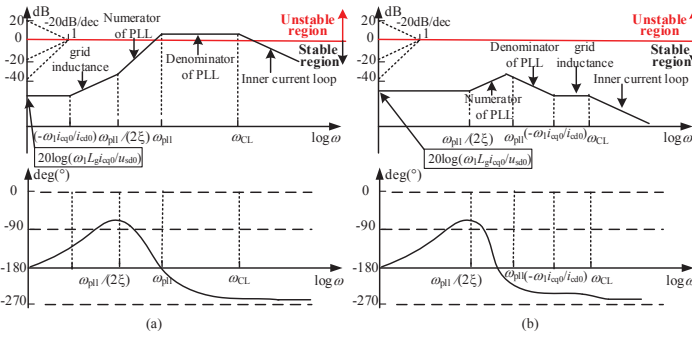
Fig. 10. The Bode plots of G_0: (a) when $[(-\omega_1 i_{cq0}/i_{cd0})< \omega_{pll}/(2\xi)]$; (b) when $[(-\omega_1 i_{cq0}/i_{cd0})> \omega_{pll}]$. ($i_{cd0} > 0$, $i_{cq0} < 0$).

TABLE III
THE FACTORS IN G_0 WHEN $[(-\omega_1 i_{cq0}/i_{cd0})<\omega_{pll}/(2\xi)]$, ($i_{cq0} < 0$, $i_{cd0} > 0$)

No.	Factor	Corner frequency (rad/s)	Gain slope (dB/dec)	Phase (deg)	Cumulative slope (dB/dec)	Cumulative phase (deg)
1	$\omega_1 L_g i_{cq0}/u_{sd0}$	——	0	-180	0	-180
2	$1 + s i_{cd0}/(-\omega_1 i_{cq0})$	$-\omega_1 i_{cq0}/i_{cd0}$	+20	90	+20	-90
3	$1 + 2s\xi/\omega_{pll}$	$\omega_{pll}/(2\xi)$	+20	90	+40	0
4	$(1+2s\xi/\omega_{pll}+s^2/\omega_{pll}^2)^{-1}$	ω_{pll}	-40	-180	0	-180
5	$(1 + s/\omega_{CL})^{-1}$	ω_{CL}	-20	-90	-20	-270

TABLE IV
THE FACTORS IN G_0 WHEN $[\omega_{pll}/(2\xi)<(-\omega_1 i_{cq0}/i_{cd0})<\omega_{pll}]$, ($i_{cq0} < 0$, $i_{cd0} > 0$)

No.	Factor	Corner frequency (rad/s)	Gain slope (dB/dec)	Phase (deg)	Cumulative slope (dB/dec)	Cumulative phase (deg)
1	$\omega_1 L_g i_{cq0}/u_{sd0}$	——	0	-180	0	-180
2	$1 + 2s\xi/\omega_{pll}$	$\omega_{pll}/(2\xi)$	+20	90	+20	-90
3	$1 + s i_{cd0}/(-\omega_1 i_{cq0})$	$-\omega_1 i_{cq0}/i_{cd0}$	+20	90	+40	0
4	$(1+2s\xi/\omega_{pll}+s^2/\omega_{pll}^2)^{-1}$	ω_{pll}	-40	-180	0	-180
5	$(1 + s/\omega_{CL})^{-1}$	ω_{CL}	-20	-90	-20	-270

TABLE V
THE FACTORS IN G_0 WHEN $[(-\omega_1 i_{cq0}/i_{cd0})>\omega_{pll}]$, ($i_{cq0} < 0$, $i_{cd0} > 0$)

No.	Factor	Corner frequency (rad/s)	Gain slope (dB/dec)	Phase (deg)	Cumulative slope (dB/dec)	Cumulative phase (deg)
1	$\omega_1 L_g i_{cq0}/u_{sd0}$	——	0	-180	0	-180
2	$1 + 2s\xi/\omega_{pll}$	$\omega_{pll}/(2\xi)$	+20	90	+20	-90
3	$(1+2s\xi/\omega_{pll}+s^2/\omega_{pll}^2)^{-1}$	ω_{pll}	-40	-180	-20	-270
4	$1 + s i_{cd0}/(-\omega_1 i_{cq0})$	$-\omega_1 i_{cq0}/i_{cd0}$	+20	90	0	-180
5	$(1 + s/\omega_{CL})^{-1}$	ω_{CL}	-20	-90	-20	-270

band-pass filter effect of G_0 can also be analyzed in a similar way shown in Fig. 8 when ($i_{cq0} \neq 0$) and similar conclusions can be drawn.

IV. SIMULATION RESULTS

To validate the proposed method and the impacts of different impacting factors on the stability, three cases with the varying PLL bandwidth, current control bandwidth and the active power and are studied. The d-axis and q-axis current step from the initial value to a higher value at t=0.8s. The weak system defined in the paper is a weak grid with SCR=1.1. The SCR is defined as the ratio of the short circuit capacity over the rated power.

A. Impact of the Bandwidth of the PLL

From the analysis in Section III-B, we can see that the increase of the bandwidth of the PLL enlarges the value of G_0's gain at the phase-crossover frequency $\omega=\omega_{pll}$, which results in G_0's effect as a band-pass filter and deteriorates the the current control stability.

In this section, four cases with the PLL's bandwidth being 6Hz, 16Hz, 50Hz and 80Hz are chosen for the simulation to verify the above conclusion. The other parameters are the same with those in Table I. The Bode plots of the four cases are presented in Fig. 11(a). It can be seen that the gain at the phase-crossover frequency increases when the PLL has a larger bandwidth. The value of the gain is larger than 0dB at its phase-crossover frequency of 600rad/s(95.5Hz) when ω_{pll}=80Hz, which means that the current control is unstable.

The time domain simulation results of the cases with ω_{pll}=50Hz and ω_{pll}=80Hz are shown in Fig. 11(b) and Fig. 11(c). It shows that oscillations occur when ω_{pll}=80Hz and the oscillation frequency is about 95Hz.

B. Impact of the Active Power

From the analysis in Section III-B, we can see that when the active power P_s increases, the gain at the phase-crossover frequency ω_{pll} will increase and be closer to the stability boundary of 0dB. In this section, we do simulations to verify the conclusion that large P_s worsens the small-signal stability of the current control.

Four cases with active power P_s being 0.5p.u., 0.4p.u. (inverter), −0.4p.u., and −0.5p.u. (rectifier) are chosen. In these cases, ω_{pll}=80Hz, and the other parameters are the same with those in Table I. The Bode plots of the four cases are presented in Fig. 12(a). It can be seen that the amplitude-frequency curve moves upward when the active power P_s increases. The value of G_0's gain at the phase-crossover frequency exceeds 0dB when P_s equals to 0.5p.u., indicating that the current control is unstable. Note that, when P_s = −0.4p.u. and −0.5p.u., the VSC operates as a rectifier whose small-signal stability is excellent.

Fig. 12(b) and Fig. 12(c) show the time domain simulation results in the cases of P_s=0.5p.u. and −0.5p.u. It can be seen that the current control is unstable when P_s=0.5p.u., with oscillations observed.

C. Impact of the Bandwidth of the Current Control

As demonstrated in Section III-B, $\omega_{pll} < \omega_{CL}$. Thus, the bandwidth of the current control doesn't influence the value of the gain of G_0 at the phase-crossover frequency $\omega=\omega_{pll}$, i.e., it doesn't influence the current control stability. In this subsection, we do simulations to verify this conclusion.

Four cases with the current control's bandwidth being 125Hz, 250Hz, 375Hz and 500Hz are selected. The other parameters in the test cases are the same with those in Table I. Fig. 13(a) shows the Bode plots of the four cases. It can be seen that G_0's gain at the phase-crossover frequency remains almost unchanged as the current control's bandwidth increases.

The time domain simulation results of the cases with ω_{CL}=125Hz and ω_{CL}=500Hz are presented in Fig. 13(b) and Fig. 13(c). It can be seen that both cases are stable, and that the d-axis current response is faster when ω_{CL}=500Hz than that when ω_{CL}=125Hz.
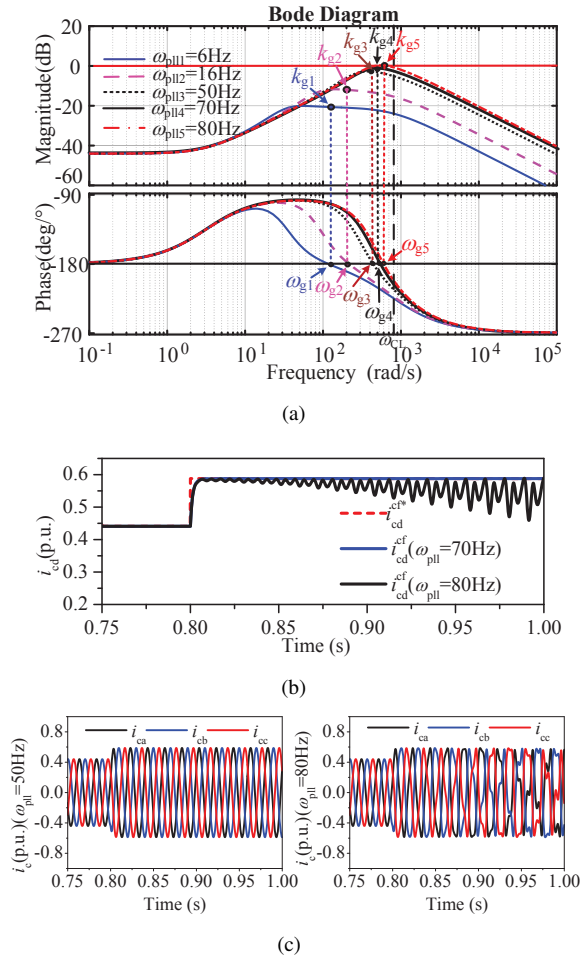
(a)

(b)

(c)

Fig. 11. Results with different PLL bandwidth.(a): The Bode plots of G_0. (b): The d-axis current responses. (c): Time-domain current responses.

D. Impact of the Reactive Power

As demonstrated in Section III-D, the absolute value of the reactive power Q_s increases, the gain at the phase-crossover frequency ω_{pll} will increase. In this subsection, we do simulations to verify this conclusion. Two cases with the reactive power being -0.62p.u.and -0.31p.u. are selected. The other parameters in the test cases are the same with those in Table I. Fig. 14(a) shows the Bode plots of the two cases. It can be seen that G_0's gain at the phase-crossover frequency increases as the absolute value of the reactive power increases. The time domain simulation results of the cases with Q_s=-0.62p.u. and Q_s=-0.31p.u. are presented in Fig. 14(b) and Fig. 14(c). It can be seen that both cases are stable, as the G_0's gain increases when Q_s=-0.62p.u. but is still below 0dB.

V. A CRITERION FOR THE BANDWIDTH DESIGN OF THE PLL

In engineering practice, some system parameters are given and can't be adjusted readily or economically, like L_g and i_{cd0}. Up to now, to select a proper bandwidth for the PLL is one of the most feasible ways to ensure the stability of the VSC system's current control.

A. The Criterion For the Bandwidth Design of the PLL

In this section, we propose a criterion to select proper bandwidth for the PLL based on the transfer function derived.
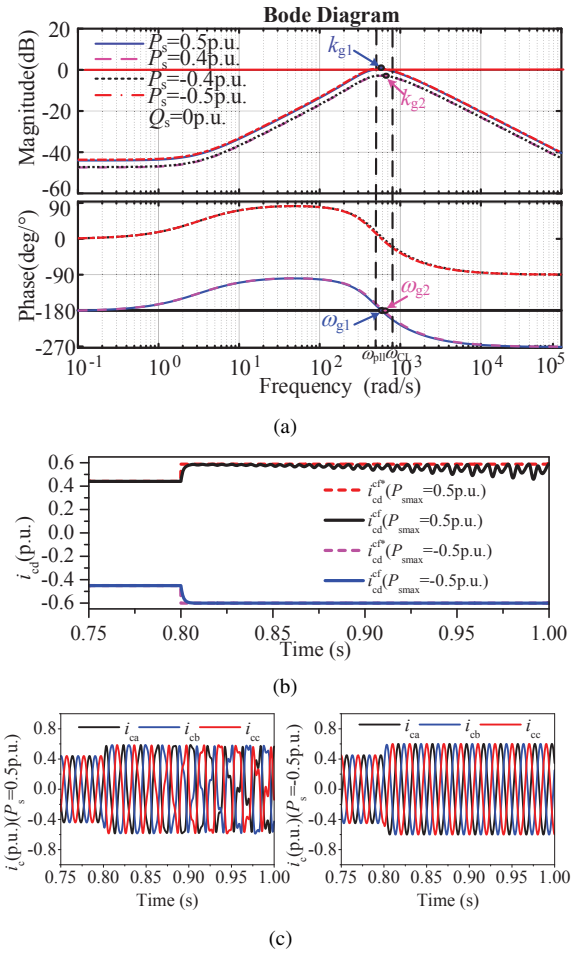

(a)

(b)

(c)

Fig. 12. Results with different real power.(a): The Bode plots of G_0 . (b): The d-axis current responses . (c): Time-domain current responses .

The key idea is that if G_0's gain at the phase-crossover frequency ω_{pll} is smaller than 0dB, the current control will always be stable under the condition that $i_{cq0}=0$, $i_{cd0} \neq 0$ (unit power factor). And this can be described as

$$|G_0|_{s=j\omega_{pll}} = \left| \frac{-L_g i_{cd0} s \left[1 + s \left(2\xi / \omega_{pll} \right) \right]}{u_{sd0} \left(1 + s/\omega_{CL} \right) \left[1 + s \left(2\xi / \omega_{pll} \right) + s^2 / \omega_{pll}^2 \right]} \right|_{s=j\omega_{pll}} < 1. \tag{18}$$

From (18), ω_{pll} should satisfy the following constraint,

$$\frac{\omega_{pll}}{\sqrt{\left(\omega_{pll} / \omega_{CL} \right)^2 + 1}} < \frac{u_{sd0} \left(2\xi \right)}{L_g i_{cd0} \sqrt{\left(2\xi \right)^2 + 1}}, \tag{19}$$

which demonstrates that the PLL's bandwidth has an upper limit when the other system parameters are given. And the upper limit is inversely proportional to the grid's equivalent inductance L_g and the injected active current i_{cd0}. Taking the test case whose parameters are shown in Table I as an example, by substituting u_{sd0}, i_{cd0}, L_g and ξ into (19), we can get $\omega_{pll} / \sqrt{\left(\omega_{pll} / \omega_{CL} \right)^2 + 1} < 408$rad/s(65Hz), and $\omega_{pll} < 75$Hz. In order to ensure the small-signal stability of the current control of the test cases in this paper, the bandwidth of the PLL should not exceed 75Hz, otherwise, the current control will be unstable. The simulation results in Fig. 11(b) show that the current control is small-signal stable when ω_{pll}=50Hz
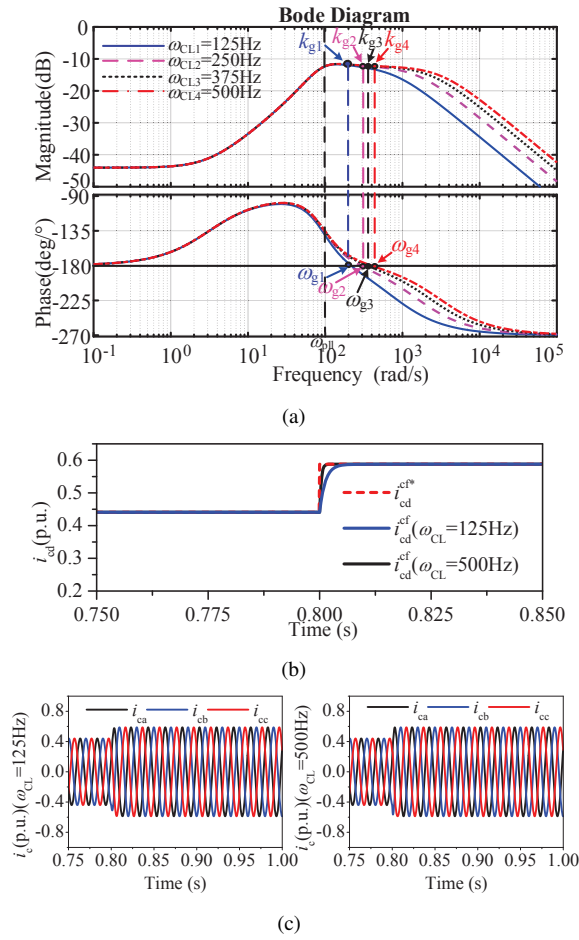
Fig. 13.   Results with different current control bandwidth. (a): The Bode plots of G_0 . (b): The d-axis current responses. (c): Time-domain current responses.

while unstable when ω_{pll}=80Hz, which matches well with this criterion.

B. Simulation Results with the Two-level Converter Considering the Outer Loops

The simulation results of the cases considering the outer loop are presented in Fig. 15 (the PLL's bandwidth is 70 Hz) and Fig. 16 (the PLL's bandwidth is 80 Hz). The parameters of the outer loop in Table I are used. In the two cases, the real power is increased to 0.8p.u. and the reactive power is increased to 0.5p.u.. The system is stable when the PLL's bandwidth is 70 Hz. However, it loses stability when the PLL's bandwidth is 80 Hz and the oscillations can be observed in the real/reactive power and the d-axis and q-axis current. This verifies the analysis in Section III that a smaller PLL's bandwidth is helpful to improve the current control stability.

The two-level converter is analyzed in this paper as integrating the wind farms and PVs to the weak grid is really a big challenge. The MMCs are usually connected to the high voltage system which might also be a weak grid, however it is not normal. Also, if the MMC internal loops of the balancing and circulating energy loops are properly tuned, a two level and an MMC have similar performance [24]. Then, the weak grid-tied MMC can be studied with our methodology.
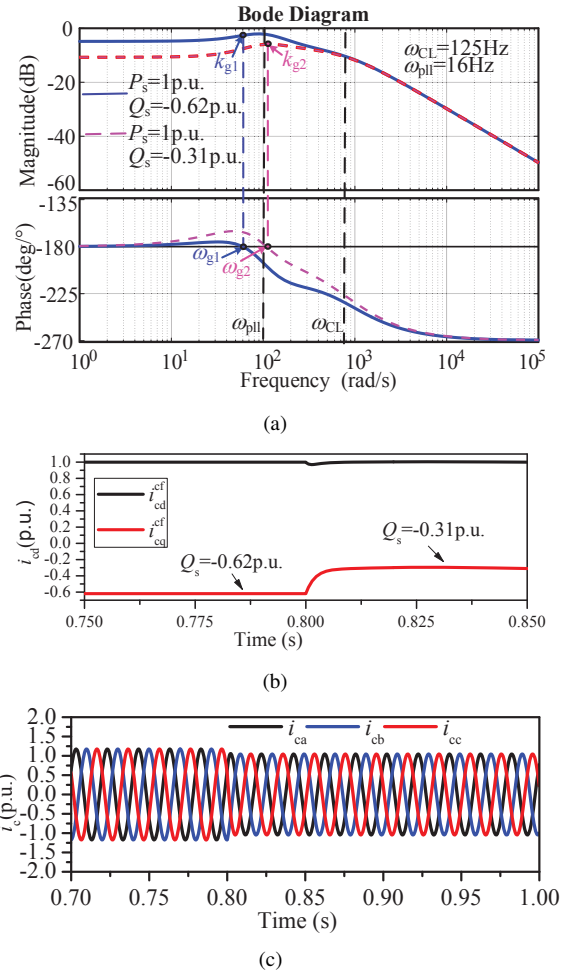

Fig. 14.   Results with different reactive power.(a): The Bode plots of G_0 . (b): The d-axis current responses. (c): Time-domain current responses.

VI. CONCLUSION

In this paper, the PLL's effect as a high-pass filter and its impact on the current control stability of the weak-grid-tied VSC is revealed based on simplified transfer functions. By neglecting time delay components and the high-frequency voltage filters, a reduced-order MIMO transfer function and its equivalent open-loop transfer function is obtained. The analysis based on the equivalent open-loop transfer function shows that: The PLL can behave as a high-pass filter in weak-grid conditions due to the large grid impedance, whereas current control behaves as a low-pass filter, making the inner loop of the weak-grid-tied VSC a band-pass filter; A higher PLL's bandwidth will increase the open-loop transfer function's maximum gain and the risk of harmonic amplification or system instability; The VSC system is less stable when it works as an inverter than as a rectifier, due to the risk of the local positive feedback in inverter mode; The current controller has slight impacts on the stability of the inner loop when its bandwidth is 0.1 to 0.2 times of the switching frequency of the power electronic switches. Based on the equivalent open-loop transfer function, an effective criterion that provides straightforward guidance for selecting a proper bandwidth of the PLL to secure the gain stability margin of the inner loop is further proposed and validated. Future work will discuss the small-signal stability of the outer loop and the design of the
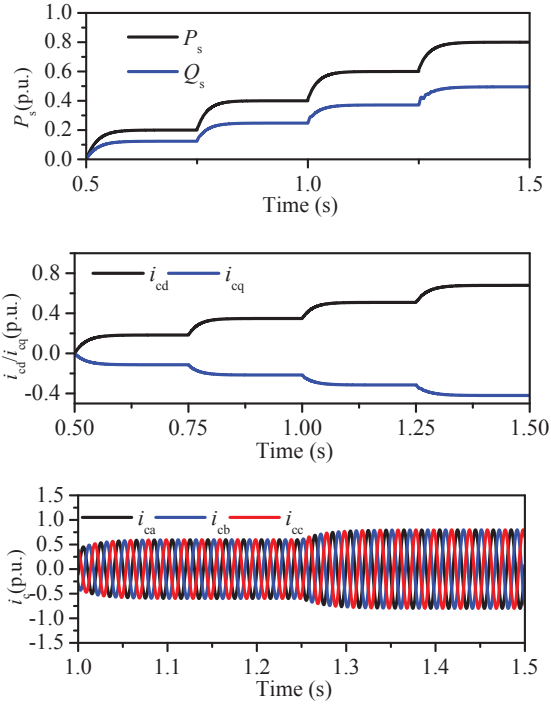
Fig. 15.   Simulation results considering the outer loop when the PLL's bandwidth is 70 Hz.
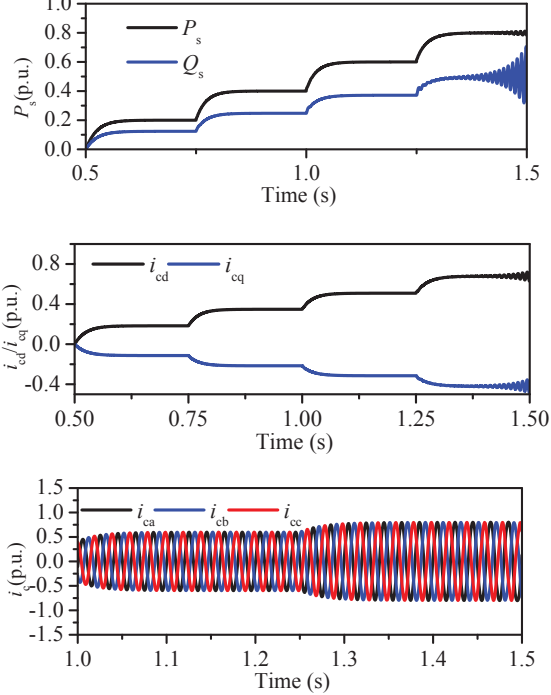

Fig. 16.   Simulation results considering the outer loop when the PLL's bandwidth is 80 Hz.

control correction parts.

APPENDIX

A. Modelling of the Plant

For simplicity, the AC filter is not considered as it is for filtering high-frequency harmonics [25]. By applying KVL across the grid equivalent impedance $R_g + j\omega_1 L_g$, we can get

$$\begin{bmatrix} si_{cd} \\ si_{cq} \end{bmatrix} = \begin{bmatrix} \frac{-R_g}{L_g} & \omega_1 \\ -\omega_1 & \frac{-R_g}{L_g} \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \frac{1}{L_g} \begin{bmatrix} u_{sd} - u_{gd} \\ u_{sq} - u_{gq} \end{bmatrix}, \quad (20)$$

Similarly, by applying KVL across the equivalent impedance $R_{eq} + j\omega_1 L_{eq}$ between the VSC and the PCC, we can get

$$\begin{bmatrix} si_{cd} \\ si_{cq} \end{bmatrix} = \begin{bmatrix} \frac{-R_{eq}}{L_{eq}} & \omega_1 \\ -\omega_1 & \frac{-R_{eq}}{L_{eq}} \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \frac{1}{L_{eq}} \begin{bmatrix} u_{cd} - u_{sd} \\ u_{cq} - u_{sq} \end{bmatrix}, \quad (21)$$

B. Modelling of the VSC Control System

As shown in Fig. 2, the PLL synchronizes the control system's frame to the grid's frame with u_s orientation. The mapping relation of one variable in the two different frames is $F_{dq}^{cf} = \boldsymbol{T}_{dq2dqcf} F_{dq}$, where F denotes u_s, u_c, u_g or i_c, the superscript "cf" denotes that the variable is in the the control system's dq frame, and $\boldsymbol{T}_{dq2dqcf}$ is written as

$$\boldsymbol{T}_{dq2dqcf} = \begin{bmatrix} \cos\theta_{pll} & \sin\theta_{pll} \\ -\sin\theta_{pll} & \cos\theta_{pll} \end{bmatrix}, \quad (22)$$

where θ_{pll} is the initial phase of the PCC voltage observed by PLL. In the following, we explain each part of the control system in Fig. 1 in detail.

1) *PLL*: The representation of the PLL shown in Fig. 1 is as follows,

$$\theta = \left(G_{PI-pll} u_{sq}^{cf} + \omega_1 \right) \frac{1}{s}, \quad (23)$$

where G_{PI-pll} is the transfer function of the PI controller in the PLL, and can be written as

$$G_{PI-pll} = k_{p\_pll} \left(1 + \frac{1}{sT_{i\_pll}} \right), \quad (24)$$

where k_{p_pll} and T_{i_pll} are the proportional coefficient and the integral time constant of G_{PI-pll}, and can be obtained by $k_{p\_pll} = 2\xi\omega_{pll}/u_{sd0}$, $T_{i\_pll} = 2\xi/\omega_{pll}$. And $\omega_e = G_{PI-pll}(s)u_{sq}^{cf}$.

2) *Current Control*: The current control can be described as

$$\begin{cases} u_{cd}^{cf*} = G_f u_{sd}^{cf} + G_{CL}(i_{cd}^{cf*} - i_{cd}^{cf}) - \omega_1 L_{eq} i_{cq}^{cf} \\ u_{cq}^{cf*} = G_f u_{sq}^{cf} + G_{CL}(i_{cq}^{cf*} - i_{cq}^{cf}) + \omega_1 L_{eq} i_{cd}^{cf} \end{cases}, \quad (25)$$

where G_f is the voltage filter, and G_{CL} is the PI controller in the inner loop. G_f and G_{CL} can be expressed as

$$\begin{cases} G_f = \dfrac{\omega_f}{s + \omega_f} = \dfrac{1}{1 + sT_f} \\ G_{CL} = k_{p\_cl} \left(1 + \dfrac{1}{sT_{i\_cl}} \right) \end{cases}, \quad (26)$$

where ω_f is the bandwidth of the voltage filter, T_f is the time constant of the voltage filter, k_{p_cl} and T_{i_cl} are the proportional coefficient and the integral time constant of G_{CL}, respectively, and they can be obtained by $k_{p\_cl} = \omega_{CL} L_{eq}$, $k_{i\_cl} = \omega_{CL} R_{eq} = k_{p\_cl}/T_{i\_cl}$, where ω_{CL} is the bandwidth of the inner loop.

The time delay caused by the signal processing and transmission in the VSC's control system can be modelled as a lumped time delay from u_c^{cf*} to u_c^{cf}, and can be described by

$$u_{cd}^{cf} = G_d u_{cd}^{cf*}, \quad u_{cq}^{cf} = G_d u_{cq}^{cf*}, \quad (27)$$

where G_d is the time delay function and can be described as

$$G_d = \frac{1}{1 + sT_d}, \quad (28)$$

where T_d is the delayed time of the PWM, the measurement and the control communication. The voltage signal u_c^{cf} is in the dq frame of the control system and needs to be transformed to the dq frame of the grid by

$$\begin{bmatrix} u_{cd}^* \\ u_{cq}^* \end{bmatrix} = \boldsymbol{T}_{dq2dqcf}^{-1} \begin{bmatrix} u_{cd}^{cf} \\ u_{cq}^{cf} \end{bmatrix}. \tag{29}$$

The VSC generates the voltage u_c by modulating the DC voltage through the on-off actions of the switches in the VSC, which is described by

$$u_{cd} = \frac{u_{cd}^*}{v_{dc0}} v_{dc}, u_{cq} = \frac{u_{cq}^*}{v_{dc0}} v_{dc}, \tag{30}$$

where v_{dc} is the DC voltage, and v_{dc0} is its steady-state value.

3) Outer Loop Control: The outer loop can be described by

$$i_{cd}^{cf*} = G_{PC}(P_s^* - P_s^{cf}), i_{cq}^{cf*} = G_{AC}(U_s^* - U_s^{cf}), \tag{31}$$

where G_{PC} and G_{AC} can be described by

$$G_{PC} = k_{p\_PC}\left(1 + \frac{1}{sT_{i\_PC}}\right), G_{QC} = -k_{p\_QC}\left(1 + \frac{1}{sT_{i\_QC}}\right), \tag{32}$$

where k_{p_PC} and T_{i_PC} are the proportional coefficient and integral time constant of G_{PC} respectively, and k_{p_QC} and T_{i_QC} are the proportional coefficient and integral time constant of G_{QC} respectively. They can be obtained by $T_{i\_PC} = T_{i\_QC} = 1/\omega_{CL}$, $k_{p\_PC} = \omega_{OL\_PC}T_{i\_PC}/(1.5u_{sm})$, $k_{p\_QC} = -\omega_{OL\_QC}T_{i\_QC}/(1.5u_{sm})$, where u_{sm} is the magnitude of the grid's phase voltage.

REFERENCES

[1] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444–2453, 2018.

[2] A. Egea-Alvarez, F. Bianchi, A. Junyent-Ferré, G. Gross, and O. Gomis-Bellmunt, "Voltage control of multiterminal VSC-HVDC transmission systems for offshore wind power plants: Design and implementation in a scaled platform," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2381–2391, 2012.

[3] J. Z. Zhou, H. Ding, S. Fan, Y. Zhang, and A. M. Gole, "Impact of Short-Circuit Ratio and Phase-Locked-Loop Parameters on the Small-Signal Behavior of a VSC-HVDC Converter," *IEEE Trans. Power Del.*, vol. 29, no. 5, pp. 2287–2296, 2014.

[4] A. Egea-Alvarez, S. Fekriasl, F. Hassan, and O. Gomis-Bellmunt, "Advanced vector control for voltage source converters connected to weak grids," *IEEE Trans. Power Sys.*, vol. 30, no. 6, pp. 3072–3081, 2015.

[5] Y. Li, G. Tang, T. An, H. Pang, P. Wang, J. Yang, Y. Wu, and Z. He, "Power compensation control for interconnection of weak power systems by VSC-HVDC," *IEEE Trans. Power Del.*, vol. 32, no. 4, pp. 1964–1974, 2016.

[6] L. Zhang, L. Harnefors, and H.-P. Nee, "Interconnection of two very weak AC systems by VSC-HVDC links using power-synchronization control," *IEEE Trans. Power Sys.*, vol. 26, no. 1, pp. 344–355, 2010.

[7] Y. Li, L. Fan, and Z. Miao, "Wind in Weak Grids: Low-Frequency Oscillations, Subsynchronous Oscillations, and Torsional Interactions," *IEEE Trans. Power Sys.*, vol. 35, no. 1, pp. 109–118, 2019.

[8] S.-H. Huang, J. Schmall, J. Conto, J. Adams, Y. Zhang, and C. Carter, "Voltage control challenges on weak grids with high penetration of wind generation: ERCOT experience," in *2012 IEEE Power and Energy Society General Meeting*, pp. 1–7, IEEE, 2012.

[9] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, 2007.

[10] L. Harnefors, "Proof and application of the positive-net-damping stability criterion," *IEEE Trans. Power Sys.*, vol. 26, no. 1, pp. 481–482, 2010.

[11] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3075–3078, 2011.

[12] M. Cespedes and J. Sun, "Impedance modeling and analysis of grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1254–1261, 2013.

[13] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Analysis of DQ small-signal impedance of grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 675–687, 2015.

[14] L. Xu and L. Fan, "Impedance-based resonance analysis in a VSC-HVDC system," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2209–2216, 2013.

[15] J. Hu, Q. Hu, B. Wang, H. Tang, and Y. Chi, "Small signal instability of PLL-synchronized type-4 wind turbines connected to high-impedance AC grid during LVRT," *IEEE Trans. Energy Convers.*, vol. 31, no. 4, pp. 1676–1687, 2016.

[16] J. Hu, B. Wang, W. Wang, H. Tang, Y. Chi, and Q. Hu, "On small signal dynamic behavior of DFIG-based wind turbines during riding through symmetrical faults in weak AC grid," *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 720–730, 2017.

[17] J. Hu, Y. Huang, D. Wang, H. Yuan, and X. Yuan, "Modeling of grid-connected DFIG-based wind turbines for DC-link voltage stability analysis," *IEEE Trans. Sustain. Energy*, vol. 6, no. 4, pp. 1325–1336, 2015.

[18] C. Guo, W. Liu, C. Zhao, and R. Iravani, "A frequency-based synchronization approach for the VSC-HVDC station connected to a weak AC grid," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1460–1470, 2017.

[19] G. Wu, J. Liang, X. Zhou, Y. Li, A. Egea-Alvarez, G. Li, H. Peng, and X. Zhang, "Analysis and design of vector control for VSC-HVDC connected to weak grids," *CSEE J. Power and Energy Sys.*, vol. 3, no. 2, pp. 115–124, 2017.

[20] M. Zhao, X. Yuan, J. Hu, and Y. Yan, "Voltage dynamics of current control time-scale in a VSC-connected weak grid," *IEEE Trans. Power Sys.*, vol. 31, no. 4, pp. 2925–2937, 2015.

[21] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2239–2248, 2007.

[22] H. Zhang, L. Harnefors, X. Wang, H. Gong, and J.-P. Hasler, "Stability analysis of grid-connected voltage-source converters using SISO modeling," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8104–8117, 2018.

[23] C. Zou, B. Liu, S. Duan, and R. Li, "Influence of delay on system stability and delay optimization of grid-connected inverters with LCL filter," *IEEE Trans. Ind. Informat.*, vol. 10, no. 3, pp. 1775–1784, 2014.

[24] J. Beerten, G. B. Diaz, S. D'Arco, and J. A. Suul, "Comparison of small-signal dynamics in MMC and two-level VSC HVDC transmission schemes," in *2016 IEEE International Energy Conference (ENERGY-CON)*, pp. 1–6, IEEE, 2016.

[25] C. Guo, J. Yang, and C. Zhao, "Investigation of small-signal dynamics of modular multilevel converter under unbalanced grid conditions," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2269–2279, 2019.

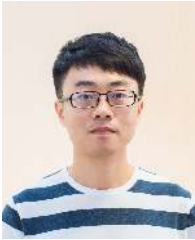**Guanglu Wu** received the B.Eng. degree from North China Electric Power University, Beijing, China, in 2012 and the Ph.D. degree from China Electric Power Research Institute, Beijing, China, in 2018, both in electrical engineering. He is currently working as an engineer in the Power System Department of China Electric Power Research Institute, Beijing, China.

His current research interests include VSC-HVDC, DC grid, power converter control and stability analysis of the power system with power electronic devices.

Huadong Sun received the B.Eng. and Master degree from Shandong University, Jinan, China, in 1999 and 2002, respectively, both in electrical engineering. He received the Ph.D. degree from China Electric Power Research Institute (CEPRI), Beijing, China, in 2005, in electrical engineering. He is currently a professor of electrical engineering with CEPRI. Also, he is the Vice President of CEPRI.

His research interests include power system analysis and control, stability of power-electronic-based power system, and large scale renewable power generation and integration.

Xi Zhang received the B.Eng. degree from Beijing Jiaotong University, Beijing, China, in 2013 and the Ph.D. degree from Hong Kong Polytechnic University, Hong Kong, in 2017, both in electrical engineering. He worked as a postdoc in the Power System Department of China Electric Power Research Institute, Beijing, China from 2018 to 2019. Currently, he is an assisant professor in School of Automation, Beijing Institute of Technology, Beijing, China since 2020.

His research interests include complexity, resilience and stability analysis of the power system with high penetrations of power electronic devices.

Agustí Egea-Àlvarez (S'12–M'14) obtained his B-Sc, MSc and Ph.D. from the Technical University of Catalonia in Barcelona in 2008, 2010 and 2014 respectively. In 2015 he was a Marie Curie fellow in the China Electric Power Research Institute (CEPRI). In 2016 he joined Siemens Gamesa as converter control engineer working on grid forming controllers and alternative HVDC schemes for offshore wind farms. He is a member of IEEE, IET and has been involved in several CIGRE and ENTSO-E working groups. Currently, Dr Agust Egea-lvarez is Strathclyde Chancellors fellow (Lecturer) at the electronic & electrical engineering department and member of the PEDEC (Power Electronics, Drives and Energy Conversion) group since 2018.

His current research interests include control and operation of high-voltage direct current systems, renewable generation systems, electrical machines and power converter control.

Bing Zhao received the B.Eng. and Master degree from Xi'an university of technology, Xi'an, China, in 2003 and 2006, respectively, both in electrical engineering. He received the Ph.D. degree from China Electric Power Research Institute (CEPRI), Beijing, China, in 2009, in electrical engineering. He is currently working as a professor of electrical engineering in the Power System Department of CEPRI, Beijing, China.

His research interests include power system stability analysis and control, load modelling, renewable power generation and integration, and operation and control of the DC grid.

Shiyun Xu received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2005 and the Ph.D. degree in mechanical systems and control from Peking University, Beijing, China, in 2010. Then, she worked as a postdoctoral fellow with the China Electric Power Research Institute, Beijing, China, till 2012. From 2007 to 2008, she was a visiting scholar of Polytechnic Institute, New York University, USA. Currently, she is a senior engineer at China Electric Power Research Institute, Beijing, China. Dr. Xu is a recipient of the Young Elite Scientists Sponsorship Program from the China Association for Science and Technology (2016), and the China Electric Power Young Elite Scientists from the Chinese Society for Electrical Engineering (2018).

Her research interests include power systems dynamic stability analysis and control with high penetration of renewable energies.

Shanshan Wang received the B.Eng. and Master degree from Shandong university, Jinan, China, in 2003 and 2006, respectively, both in electrical engineering. She received the Ph.D. degree from China Electric Power Research Institute (CEPRI), Beijing, China, in 2011, in electrical engineering. She is currently working as a senior engineer in the Power System Department of CEPRI, Beijing, China.

Her research interests include analysis and design of VSC-HVDC, power system stability analysis and control and operation and control of the DC grid.

Xiaoxin Zhou (F'96–LF'10) graduated from Tsinghua University, Beijing, China, in 1965. He is the Honorary President of China Electric Power Research Institute (CEPRI), academician of Chinese Academy of Sciences, and Fellow of IEEE. In 2008, he received the IEEE Power & Energy Society Nari Hingorani FACTS Award.

Currently, he serves as the Editor-in-Chief for the *CSEE Journal of Power and Energy Systems* since 2015. His main research interests include power system analysis and control, power system digital simulation, Flexible AC Transmission System (FACTS), and integration of large scale renewable power generation.