PARYLENE TO SILICON-NITRIDE BONDING FOR EASY POST-INTEGRATION OF HIGH-PRESSURE MICROFLUIDICS TO CMOS DEVICES

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ABSTRACT

We report a new low-temperature (280°C) parylene-C wafer bonding technique, where O_2 plasma-treated parylene-C bonds directly to Si_3N_4 with an average bonding strength of 23 MPa. The technique works for silicon wafers with nitride surface and uses a single layer of parylene-C deposited only on one wafer. Microfluidic devices fabricated with this technology demonstrate a burst pressure as high as 16 MPa, while electrode structures remain functional after bonding. Using this technique, microfluidic structures can easily be formed by direct bonding to the nitride passivation layer of CMOS devices without any additional processing.

KEYWORDS: microfluidic integration, parylene bonding, CMOS integration

INTRODUCTION

Attempts to realize CMOS-integrated microfluidic devices have been made aiming to reduce microfabrication and packaging costs. However, traditional footprints of microfluidic devices have been an order-of-magnitude larger than that of CMOS devices and integration of these two technologies generally is difficult [1-3], packaging and integration constituting major costs. Hybrid integration requires low-temperature bonding without any processing on the CMOS side, which is not achievable for anodic, eutectic or fusion bonding. Moreover, microfluidic footprints should be reduced to that of CMOS chips to economize on CMOS costs, which can be done by high pressure-resistant microfluidics, implying shorter and narrower channels for a given fluidic throughput. Consequently, a post-CMOS bonding technique 1) that is high-strength and enables high pressure-resistant devices, 2) that can be performed at a sufficiently low temperature for keeping metal integrity, and 3) that can use directly the passivation layer with minimal post-processing, can be an important enabling technology for CMOS-microfluidics integration.

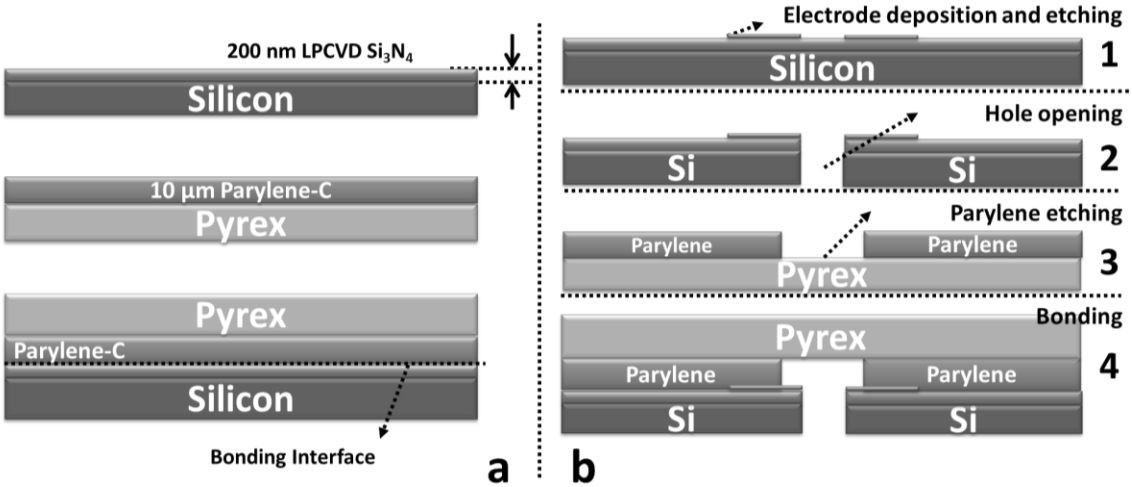

Figure 1 - Illustration of the bonding process. (a) The bonding process uses a Pyrex wafer covered with a 10 µm thick parylene-C layer and a silicon substrate with a 200 nm LPCVD Si_3N_4 layer. Bonding with parylene-C was performed at 280 °C under vacuum during 40 minutes while applying 1000 mbar tool pressure. Prior to bonding, Pyrex wafers were plasma treated during 15 s at 200 W under 400 sccm O_2 flow for surface activation of the parylene-C layer. (b) Fabrication of microfluidic devices with electrodes for burst pressure and metal integrity tests. 1) 100 nm Pt electrodes are evaporated and etched with reactive ion etching (RIE). 2) The fluidic inlet holes are opened in the silicon wafer by deep RIE. 3) Channels are etched in parylene-C using RIE via an a-Si mask and 4) wafers are bonded.

EXPERIMENTS AND RESULTS

Figure 1 illustrates direct bonding of silicon wafers covered by a 200 nm thick LPCVD Si_3N_4 layer and Pyrex wafers with 10 µm parylene-C. Prior to parylene-C coating, the Pyrex wafers are piranha-cleaned. Bonding with parylene-C is performed at 280 °C under vacuum during 40 minutes while applying 1000 mbar tool pressure. Prior to bonding, Pyrex wafers were plasma treated during 15 s at 200 W under 400 sccm O_2 flow for surface activation of the parylene-C layer.

In order to realize microfluidic devices that include electrodes for burst pressure and metal integrity tests, 100 nm Pt electrodes are evaporated and etched with reactive ion etching (RIE). Following this, the fluidic inlet holes are opened in the silicon wafer by deep RIE using a 10 µm thick AZ 9260 photoresist. Later, parylene-C is deposited on a Pyrex wafer after si-

lanization of the Pyrex surface using A-174 silane. The channels are etched in parylene-C using O_2 gas in an inductively coupled plasma (ICP) RIE via a 200 nm a-Si mask. After the removal of the a-Si hard-mask from the parylene-C surface, wafers are bonded with the recipe given above.

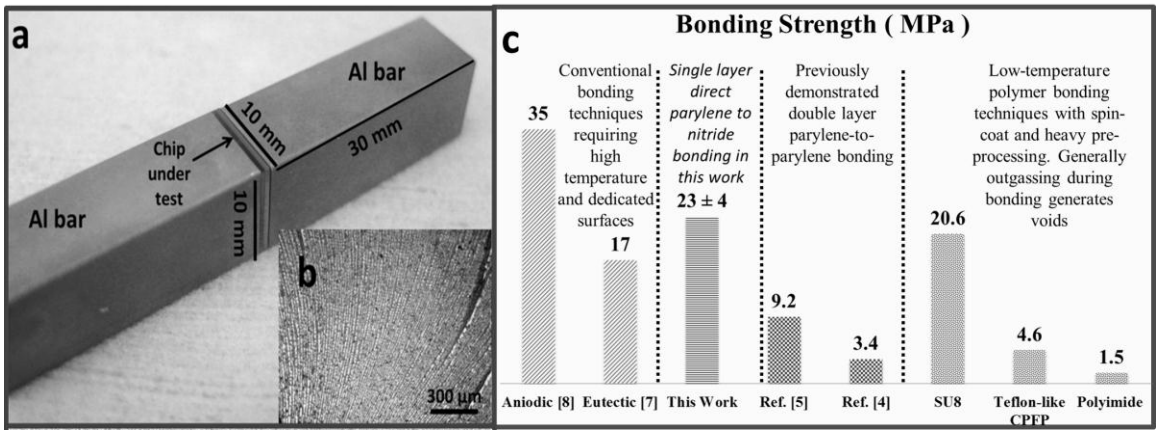

Figure 2 - Pull-testing and results. (a) Assembly of the chip sample with aluminum pulling bars. (b) Optical microscope image of fractured interface after pull-testing. In general, fracture occurs in the form of cracks in the parylene-C. (c) Results of the pull-test measurements and comparison with existing bonding techniques. For our study, the value of 23 ± 4 MPa is obtained from the results of 7 pull-tests. Rest of the data taken from [9].

To perform the pull tests, bonded wafers are diced in square dies. Then, aluminum pulling bars are used to fix the dies to the pull-test equipment, as shown in Figure 2.a. The tests are performed with 0.1 mm/min pull rate until the fracture point. Figure 2.c shows the results of pull test measurements demonstrating a 23 MPa average bonding strength, in comparison to existing techniques. The novelty of our process is that bonding directly occurs between a parylene-C and a silicon-nitride layer, avoiding a polymeric bonding interface in the bonding stack. In contrast, previous parylene bonding literature [4-5] suggests that both of the substrate surfaces should be coated with parylene-C and bonding is realized physically at a parylene/parylene interface, where fracture occurs at this interface during pull-tests. Such interface is avoided in our process, and hence, an average bonding strength of 23 MPa is achievable. Figure 2.b shows an image of a fractured interface, where the fracture patterns are observed typically in the parylene-C layer, but rarely at the bonding interface.

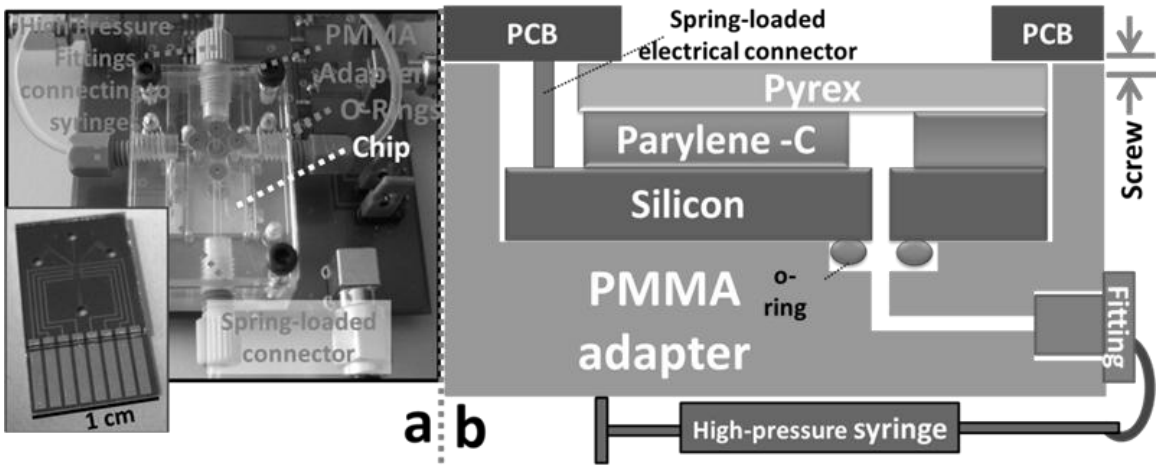

Figure 3 - Burst pressure experiments. a) Photograph of the integrated experiment setup, where a PMMA holder is used to establish a HPLC fitting to the chip. The inset shows a fabricated chip with electrodes. b) Cross-section illustration of the experimental setup.

For burst-pressure experiments, a PMMA holder, allowing application of commercial high-pressure resistant High Performance Liquid Chromatography (HPLC) connectors to the microchip, has been used. The chip is connected to this holder via o-rings, as shown in Figure 3. Flow is applied to microfluidic channels using a stainless steel syringe and pressure at the inlet is increased by 0.1 bar/s, as monitored by a sensor. The pressure value at which an abrupt decrease is observed is taken as the burst-pressure. For our study, burst-pressure is as high as 16 MPa, pressure at which a silicon or Pyrex failure is observed**.** Figure 4.a shows the results of burst-pressure measurements in comparison to existing techniques.

The histogram of measured resistance for pad-to-pad metal structures designed in our devices shows that the electrodes are functional and show a coefficient of variation (CV) of 1.5% of for 30 devices throughout the wafer, indicating that metals remain functional after bonding (Figure 4.b). This proves that electrodes remain intact after the bonding process.

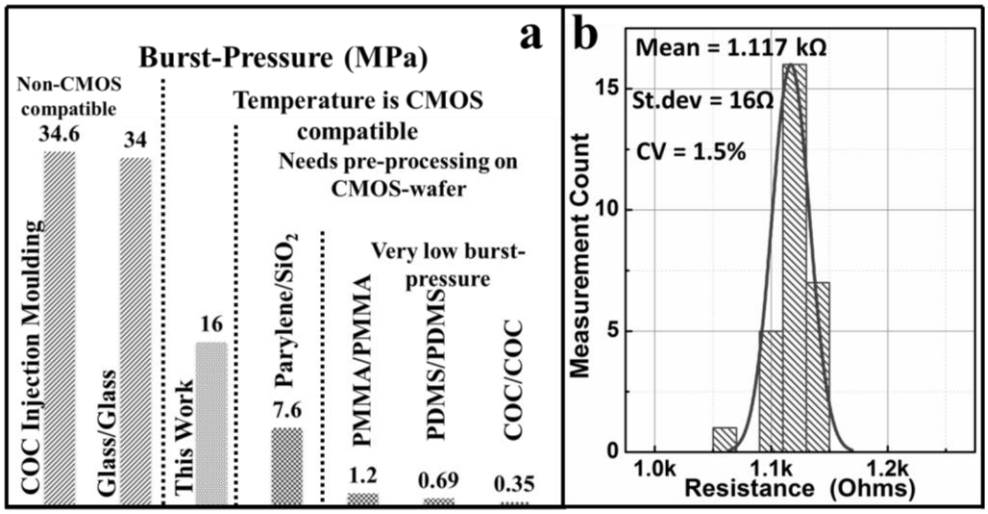

Figure 4 – Burst pressure and metal integrity tests. (a) Results of the burst pressure measurements and comparison with existing devices reported in the literature. Rest of the data was taken from [9]. (b) Results of metal integrity tests showing a low coefficient of variation in measured resistances for pad-to-pad metal structures designed in our devices.

CONCLUSIONS

We believe that our low-temperature and high-strength bonding technique with no pre-processing on the CMOS side will open perspectives in easy post-CMOS integration of microfluidic systems, which helps decreasing the gap between the traditional footprints of these two technologies and will open perspectives for three-dimensional integration and micro-chip cooling.

REFERENCES

[1] H. Lee, Y. Liu, D. Ham and R. M. Westervelt, Lab Chip, 2007, 7, 331-337

[2] H. Lee, Y. Liu, R.M. Westervelt, and D. Ham, IEEE Journal of Solid State Circuits, 2006, vol. 41, no. 6

[3] U. Lehmann et.al, Sensors and Actuators B, 132 (2008), pp. 411-417.

[4] H. Kim, and K. Najafi, Microelectromechanical Systems, vol. 14, no. 6, pp. 1347-1355, 2005.

[5] N. Hong-seok, M. Kyoung-sik, C. Andrew et al., Micromechanics and Microengineering., vol. 14, no. 4, pp. 625, 2004

[6] N. Hong-seok, P. J. Hesketh, and G. C. Frye-Mason, Microelectromechanical Systems, vol. 11, no. 6, pp. 718-725, 2002

[7] Y. Mei, G. Roientan, and K. Najafi, Solid-State Sensor, Actuator and Microsystems Workshop, Hilton Head Island, 2002, pp. 86–89

[8] J. Wei, H. Xie, M.L. Nai, C.K. Wong and L.C. Lee, Micromechanics and Microengineering, vol 13, no. 2, pp. 217-222, 2003.

[9] A.T. Ciftlik and M.A.M. Gijs, Micromechanics and Microengineering, vol 21, pp. 035011, 2011..

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