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Entitled

PASSIVE THERMAL MANAGEMENT USING PHASE CHANGE MATERIALS

For the degree of Master of Science in Mechanical Engineering

Is approved by the final examining committee:

Dr. Amy Marconnet
Chair

Dr. John Howarter

Dr. Xianfan Xu

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Approved by Major Professor(s): Dr. Amy Marconnet

Approved by: Dr. Jay Gore 10/4/2016

Head of the Departmental Graduate Program Date

PASSIVE THERMAL MANAGEMENT USING PHASE CHANGE MATERIALS

A Thesis

Submitted to the Faculty

of

Purdue University

by

Yash Yogesh Ganatra

In Partial Fulfillment of the

Requirements for the Degree

of

Master of Science in Mechanical Engineering

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West Lafayette, Indiana

This thesis is dedicated to my parents and family.

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I would like to express my gratitude to my advisor, Dr. Amy Marconnet. A hopeful email (addressed to an incorrect lab!) for an independent study project led to a collaboration which culminated in a Masters dissertation. This collaboration has been an enjoyable and an invaluable learning experience, where I have been inspired by her unique approach to research, standards for excellence, humility , and personal integrity. I appreciate her honest advice for helping me navigate through graduate school, from course selection to professional development activities. I thank her for the guidance and unreserved help for the last 2 years. This thesis would not be completed if not for her patience during the editorial process. I would also like to thank Dr. John Howarter and Dr. Xianfan Xu for serving on my defense committee.

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I consider myself fortunate to have strong pillars of support in the form of my parents, Yogesh and Nita, whose countless sacrifices enabled me to pursue a graduate degree. I strive to meet their exemplary dedication towards work and follow the path of continual self-improvement. I cannot thank my extended family enough especially, my aunts (Kalpana and Namrata) and my uncles (Tushar and Chetan), who are my parents away from home.

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ABSTRACT

Ganatra,Yash Yogesh M.S.M.E, Purdue University, December 2016. Passive Thermal Management using Phase Change Materials. Major Professor: Amy Marconnet, School of Mechanical Engineering.

The trend of enhanced functionality and reducing thickness of mobile devices has led to a rapid increase in power density and a potential thermal bottleneck since thermal limits of components remain unchanged. Active cooling mechanisms are not feasible due to size, weight and cost constraints. This work explores the feasibility of a passive cooling system based on Phase Change Materials (PCMs) for thermal management of mobile devices. PCMs stabilize temperatures due to the latent heat of phase change thus increasing the operating time of the device before threshold temperatures are exceeded. The primary contribution of this work is the identification of key parameters which influence the design of a PCM based thermal management system from both the experiments and the numerical models.

This work first identifies strategies for integrating PCMs in an electronic device. A detailed review of past research, including experimental techniques and computational models, yields key material properties and metrics to evaluate the performance of PCMs. Subsequently, a miniaturized version of a conventional thermal conductivity measurement technique is developed to characterize thermal resistance of PCMs. Further, latent heat and transition temperatures are also characterized for a wide range of PCMs.

In-situ measurements with PCMs placed on the processor indicate that some PCMs can extend the operating time of the device by as much as a factor of 2.48 relative to baseline tests (with no PCMs). This increase in operating time is investigated by computational thermal models that explore various integration locations, both at the package and device level.

CHAPTER 1. INTRODUCTION

Electronic devices are commonplace today. From large scale mainframes and servers to smartphones and wearable devices to devices embedded in home appliances, automobiles, and robots, the electronic computer is ubiquitous and nearly unrecognizable in some applications. The invention of the transistor led to the miniaturization of components, which in turn increased the package density (number of components per chip) and computational capabilities. The invention of the integrated circuit gave further impetus to this trend enabling thousands of devices per chip (Very Large Scale Integration). Higher packing density led to higher power dissipation. The power density of a Pentium 4 processor in 2004 was comparable to that of a nuclear power plant, as shown in Figure 1.1. Thermal management, therefore, became a bottleneck to processor system design. At that point, to halt the increasing power dissipation density, chip manufacturers limited the clock frequency and introduced multi-core processors. Even with this strategy, thermal management was critical to the reliability of electronic devices: 55 % of all failures in electronic devices in 1989 were related to thermal effects [2] and that trend has continued into the 21^{st} century.

The System on Chip (SoC) power dissipation for mobile devices has increased continually since 2009 as shown in Figure 1.2 [3]. Traditional cooling mechanisms [forced convection cooling using air or cooling fluids, extended surface heat transfer (fins)], which are used for large form factor devices like computers and mainframes, are not feasible for mobile devices due to size and weight constraints. Currently, a network of integrated heat spreaders transports heat away from the processors. Although this dissipates the heat from the hot spot, overall heat dissipation from mobile devices is still limited by natural convection from the case. Furthermore, mobile devices often operate with cyclic bursts of intense computation (power generation) followed by a rest period (background power dissipation level) to improve responsiveness.

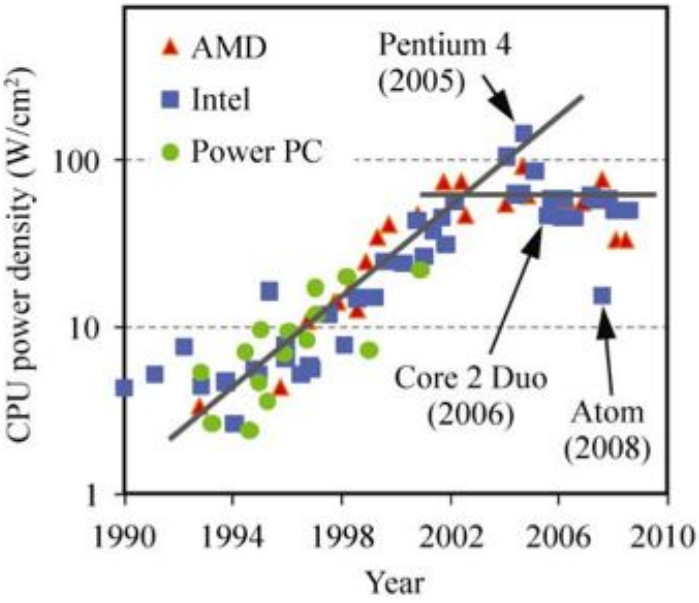


Figure 1.1. CPU Power density increased rapidly from the 1990's through early 2000's as the density of transistors on the chip increased. With the advent of multicore processors, the power density plateaued, but still leads to thermal management challenges (Figure reproduced with permission from [1]).

Thermal cycling induced by these cyclic loads exacerbates the probability of failure. Active cooling mechanisms tend to enhance the thermal cycling effect. Passive cooling mechanisms, which absorb the excessive heat generated during power bursts and dissipate it during the off-peak period, stabilize the average temperature inside the device making it less susceptible to failure due to thermal cycling. Phase change materials (PCMs) absorb heat during phase change (by virtue of their latent heat of melting) essentially pinning the temperature near the transition temperature (*i.e.* the melting point for isothermal phase change).

PCMs have been extensively used for latent thermal energy storage with an emphasis on applications like solar water-heating systems [4–6] and building heating and cooling [7–9]. Also, they have been used in spacecraft thermal management for rejecting heat to space at relatively low temperatures and for waste heat storage to maintain

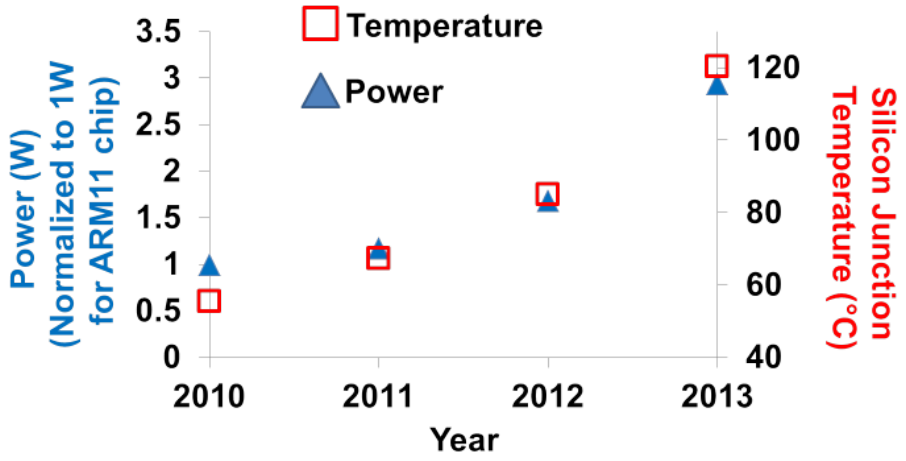


Figure 1.2. System on chip (SoC) power dissipation normalized with respect to ARM11 processor used in 2010 (blue filled triangles) and Silicon die temperature (rectangles with red outline) for Broadband mobile processors. The power dissipation has increased by about a factor of 3 from 2010 to 2013. The silicon temperatures also follow a similar trend and have reached their threshold temperature of about 125 °C (Adapted from [3]).

the temperatures of the electronic package within its operating limits [10–13]. These characteristics render them useful for limiting package and surface temperatures in electronic devices. Several approaches have been developed to quantify the effectiveness of integrating PCMs in electronics cooling [14–16].

This thesis comprehensively investigates PCMs for electronic thermal management. Beyond thermal storage properties, the thermal conductivity of the PCM impacts the effectiveness of integrating the PCM into the cooling scheme. The thesis is organized as follows

- In Chapter 2 existing experimental and numerical studies focused on use of PCMs in electronics thermal management are reviewed including different schemes for integrating the PCMs into electronic devices.

- Chapter 3, adapted from the author's InterPACK 2015 paper [17], describes an measurement technique to evaluate the thermal resistance of phase change materials.

- Chapter 4 discusses characterization of select thermophysical phase change properties including latent heat and the transition temperature using Differential Scanning Calorimetry (DSC).

- Chapter 5 focuses on the design of an *in situ* thermal cycling rig for interrogating geometry and material properties.

- Chapter 6 reviews analytical and numerical techniques to model phase change heat transfer.

- In Chapter 7, numerical techniques are implemented in COMSOL and validated against analytical solutions. Subsequently, device and package level computational models are developed to study temperature distributions.

- Chapter 8 summarizes key contributions of this work and proposes potential future directions.

CHAPTER 2. STRATEGIES FOR INTEGRATING PHASE CHANGE MATERIALS IN ELECTRONIC DEVICES

2.1 Overview

The primary objective of using PCMs in electronics thermal management is to limit temperature spikes (both at system and device level) through nearly isothermal absorption of energy during phase change. However, conventional PCMs like paraffins have low thermal conductivity, which can create localized high temperature regions (*hotspots*) that adversely affects device performance. Hence, the integration location and material properties need to be optimized under various thermal constraints. The following section, Section 2.2, discuses the use of PCMs as Thermal Interface Materials (TIMs) and the improvement to contact during phase change. Other integration locations that require high latent heat, such as in the heat exchanger and directly on the chip, are discussed in Sections 2.3. Section 2.4 discusses techniques to improve the thermal conductivity and latent heat of the PCM, in order to improve heat transfer and improve thermal performance.

2.2 PCMs as Thermal Interface Materials for Improved Thermal Contact

TIMs improve contact between adjoining parts by facilitating heat transfer by conduction across interfaces. TIMs can be applied in solid, liquid (molten solder), or semi-liquid form (thermal grease) states. Liquid TIMs provide a better contact at the interface than other TIMs due to their flow characteristics. However, they tend to pump out over time , regardless of whether they are in operation or not [18]. A TIM that changes from solid to liquid or semi-liquid state around the operating temperature is desirable. For PCM based TIMs, the material fills in the microscopic crevices between the materials improving contact and thermal transport. Upon heating, the

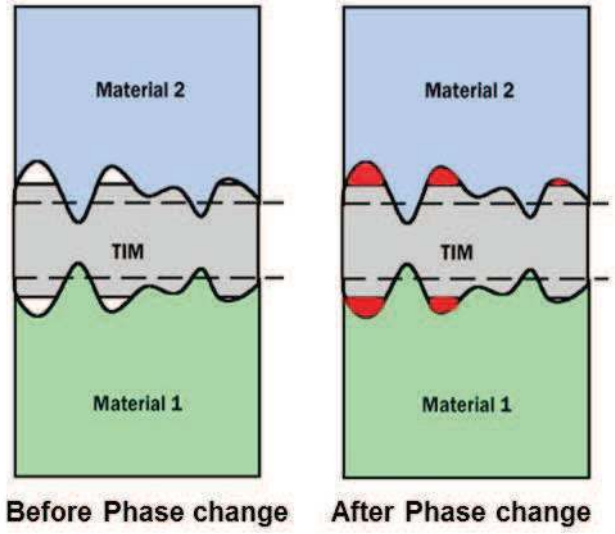


Figure 2.1. Improved contact due to increased flow of phase change TIM. Initially the PCM based TIM is applied as a thin solid sheet. Upon heating the TIM melts, and with compression of the system, the molten TIM fills in the gap (Figure reproduced with permission from [19]).

material melts to fill in gaps (see Figure 2.1) and the improved contact remains after cooling. TIMs are generally applied between chip and heat spreader (*TIM1*) and between heat spreader and heat sink (*TIM2*). To enhance power dissipation and reduce the interfacial thermal resistance, high thermal conductivity and low bondline thickness are desired. In addition to thermal properties, numerous mechanical and reliability challenges exist including induced thermal stresses and fatigue from the mismatch in coefficient of thermal expansion (CTE) [20]. Furthermore, it is advantageous if the TIM can be reworked after assembly to disassemble and reassemble the bond.

Phase change thermal interface materials are generally comprised of suspended particles of high thermal conductivity in a base material such as paraffin, polymer, or co-polymer [21; 22] As described by Ollila [23], these TIMs do not necessarily complete a phase change from solid to liquid, but rather there is a steep reduction in

viscosity resulting in improved contact between mating surfaces near the operating temperature. Several researchers [19;24–27] have reviewed and compared conventional and state-of-the-art TIMs in detail. To summarize, the advantages of using PCM based TIMs include better contact compared to thermal greases (see Figure 2.2) and no pumpout. These advantages are offset by the high pressure required to improve the performance of PCM over thermal greases, lower thermal conductivity, and difficulty in reproducing thermal performance data across different test facilities [27–30]. For more detailed reviews of thermal measurement techniques for TIMs, see Lassance [31], Bosch [32], and Rosten [33].

2.3 PCMs for Enhanced Latent Heat Storage

A unique advantage of PCMs is their ability to mitigate temperature spikes through melting or state-change. For mobile applications, achieving high latent heat per unit volume is crucial due to the limited package size. Here, strategies for integrating the PCM in the heat exchanger and on chip / inside the package are evaluated.

2.3.1 Integration with the Heat Exchanger

Due to the heat storage capabilities of PCMs, the processor can operate at full power for longer without overheating. In other words, the duration of sustained system performance is increased within given thermal constraints (e.g.near the die, the temperature can not exceed 80 °C or 110 °C and the case / surface temperature can not exceed 40 °C [34]). The low thermal conductivity (or thermal diffusivity in a transient context) of PCMs impedes heat transfer from the package leading to overheating. Hence, thermal conductivity enhancers are used to enhance the heat dissipation capability of the PCM (see also Section 2.4). Also, volume change during melting and void formation during solidification can lead to challenges in the packaging and integration of PCMs.

TIM	Advantages	Disadvantages
Thermal Grease	• High thermal conductivity • Low cost • Low thermal resistance due to relatively less interface thickness • No delamination	• Pumpout caused by thermal cycling • Dry out over times reducing reliability • Thickness control is difficult
Polymeric phase change TIM	• Less susceptible to pumpout • Easy to apply • Lower thermal resistance than thermal greases	• Lower thermal conductivity than thermal grease • Constant pressure required to hold the TIM which increases mechanical stress • Void formation due to thermal cycling
Low Melting Point alloy phase change TIM	• Easy to apply • High thermal conductivity since it is a metallic solder • No cure required	• Void formation due to dry out • Oxidation / Corrosion at high temperatures
Filled polymers	• No pumpout • Easy to apply since it can be cut to match the size of mounting surfaces	• Needs curing • Higher cost than thermal grease • Delamination can be an issue • Poor thermal contact than thermal grease since it does not flow freely • Lower thermal conductivity than thermal grease

Figure 2.2. Comparison of different types of TIM. A combination of a polymer base and ceramic (e.g.alumina and aluminum nitride) or metallic fillers (e.g.silver and aluminum) are the main constituents of thermal grease. These components are usually mixed together and applied as a paste. PCM based TIM's are generally low temperature thermoplastics enhanced with high conductivity fillers. They improve contact because of a decrease in viscosity rather than a change of phase in conventional PCMs (e.g.paraffin wax), from solid to liquid. These are usually available commercially as thermal pads. Low melting point alloys are metallic solders comprising of Bi , In, Sb, and Ga. Filled polymers are made of silicone and fusible fillers, sometimes mixed with non-fusible fillers (e.g.graphite flakes, carbon fiber) to enhance the overall thermal conductivity. (Adapted from [25]).

Phase change materials are useful in conditions where there is a need to maintain a nearly isothermal environment under vastly different thermal conditions - for example, satellites experience thermal gradients as they pass in and out of Earth's shadow and it is crucial to maintain a stable thermal environment inside a spacecraft on planets that do not have an atmosphere. Thus, early work on use of phase change materials focused on spacecraft thermal management [12; 35]. Bentilla et al [35] broadly categorized the integration of PCM in a heat exchanger into three systems: (1) the PCM on top of the heat dissipating component with all the heat absorbed by the PCM due to a combination of latent and sensible heat (2) the PCM integrated in the radiator to compliment heat transfer (e.g.in a fin) and (3) the PCM placed between the heat source and the radiator such that all heat went through the PCM before being dissipated via the radiator. These designs are shown in Figure 2.3. Thermal storage systems are often used as an enhancement to the existing heat rejection systems. Including PCMs results in weight savings since the latent heat of phase change enables the engineer to design for average heating loads rather than the peak loads (which represented the worst case scenario). Busby *et al.* [11] analyzed the feasibility of such a system used in radiators of spacecraft. They assumed heat transfer by conduction only without any temperature gradient in the liquid (melt) region for a pulsed power profile to compute the weight benefit of a thermal energy storage system. From this analysis, they recommended the use of PCMs for systems where a significant mass reduction is achieved, like short duty cycle power profiles. Furthermore, PCMs stabilize the temperature of electronic components operating for multiple duty cycles [13], as shown in Figure 2.4. PCMs can be used as a buffer to store waste heat from electronic components coupled with a thermoelectric device to generate electricity [36; 37]. PCMs are also applied in radiators (see Figure 2.4) due to potential weight reduction since the temperature stabilization due to the latent heat of phase change implied that the system could be designed for the mean heat removal rather than peak heat load [13]. Further, Hale *et al.* [13] suggested the use of PCMs to minimize temperature variations in the coolant fluid which circulates in the radiators.

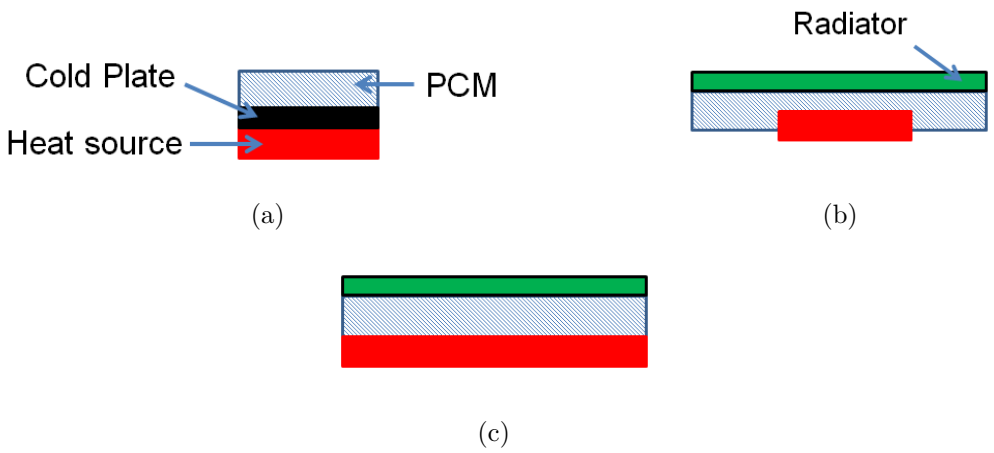
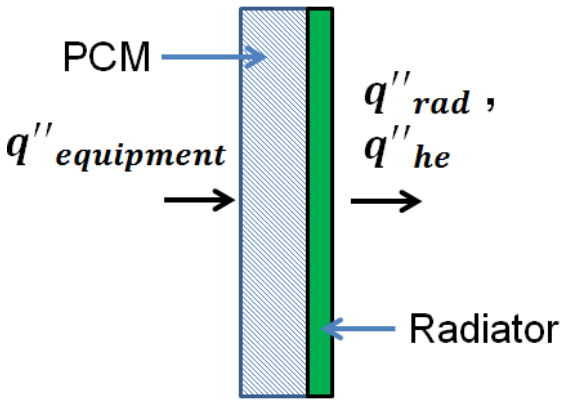


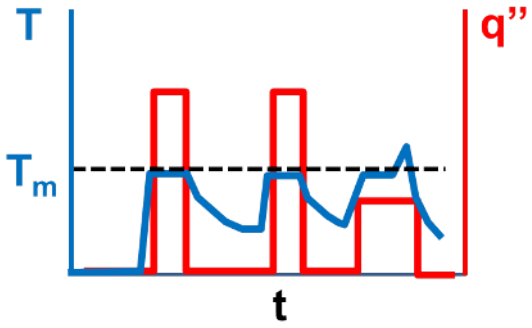
Figure 2.3. Integration of PCM in a heat exchanger. (a) PCM placed on top of the heat dissipating component in the absence of a radiator. Waste heat is completely absorbed by the PCM. No heat exchange with environment due to absence of radiator. (b) PCM placed between the radiator to stabilize temperatures. For example, the radiator can be a fin and the PCM placed between the fins. The surface area of radiator is greater than than that of the heat dissipating component. (c) Similar configuration to (b) except that the radiator surface area equals the surface area of the equipment. Extended surfaces (e.g.fins) are used as radiators and PCM is increased between these surfaces to enhance the overall thermal conductivity. The mass of PCM is determined from the heat absorbed by the PCM and the heat dissipated by the radiator to the ambient.(Adapted from Bentilla [35]).

Also, Humphries *et al.* [12] used PCM in heat exchangers with a flowing fluid as shown in Figure 2.5. The PCM, placed between the fins, was separated by a baseplate. An overall heat transfer coefficient was used to account for 2D behavior due to the fin. The axial heat conduction in fluid and effects of baseplate (which acts as separator) was neglected to simplify the energy equation for internal forced convection. As the PCM melts, the temperature drop of the fluid at the outlet decreased due to a decrease in the overall heat transfer coefficient, as expected.

To mimic a heat source in an Integrated Circuit (IC) package, Chebi *et al.* [38] heated a copper cylinder filled with PCM and a cartridge heater, as shown in



(a)



(b)

Figure 2.4. (a) PCM used in spacecraft thermal management for temperature stabilization. PCM absorbs the heat during peak power dissipation and stabilizes the temperatures. During “off” times, the radiator or a heat exchanger is used (heat fluxes denoted by q''_{rad}, q''_{he} respectively) to dissipate heat to ambient and aid in re-solidification of the melted PCM (Figure reproduced with permission from [13]). (b) Transient thermal response (shown in blue) of a PCM based thermal energy storage system in response to cyclic loads (shown in red). The PCM stabilizes the temperatures to within the allowable temperature limits. The duty cycle is tuned to ensure that PCM re-solidifies before the next power spike to ensure optimal utilization of latent heat of the PCM.

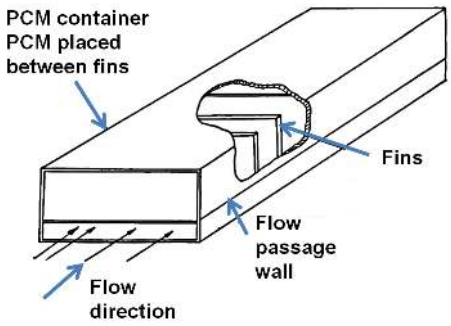


Figure 2.5. schematic of a testbed for measuring the heat transfer between a flowing fluid and PCM. PCM is placed between the fins which are used to improve the thermal contact between PCM and the heat transfer fluid. To simplify the model, 1D heat transfer is fluid considered by lumping multi-dimensional effects into a overall heat transfer coefficient (Figure reproduced with permission from [12]).

Figure 2.6. The cylinder was placed in different orientations with respect to the heater - heater at bottom, inverted, and sideways - to study the effect of natural convection. The effect of phase change and natural convection is lumped into an effective thermal conductivity. They modeled the system using a one-dimensional steady state analytical model, which neglected the radial temperature gradients, with top and bottom surfaces of cylinder modeled as heat flux and insulated boundaries, respectively. The heat flux was estimated from the the known voltage and resistances applied to the heater. The reported effective thermal conductivities were an order of magnitude higher than only the copper tube, which indicated the potential benefits of phase change and natural convection in liquid (melt) region.

2.3.2 Integration on Chip and Inside the Package

PCMs can also be integrated much closer to the heat source: directly "on-chip" or inside the package. This configuration finds application in mobile devices due to thickness limitations. The PCM can be placed in the microprocessor socket or in

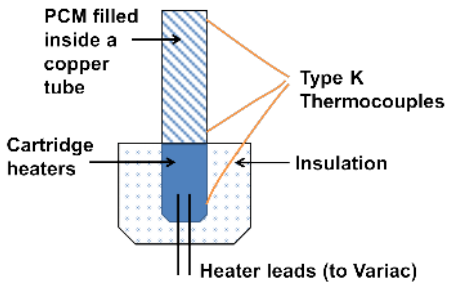


Figure 2.6. Schematic of experimental setup to study effectiveness of PCM (P-116 Sunoco Wax) placed on top of Integrated Circuit (IC) package, which is represented by the cartridge heaters. The copper cylinder containing the PCM is exposed to ambient and the cartridge heaters are insulated on all but the top surface. This configuration was analytically treated as 1D axisymmetric geometry. (Adapted from [38]).

a custom-built enclosure [39]. Gurrum *et al.* [40] studied the feasibility of using a metallic PCM (60 µm thick) on microwave power transistors of thickness 100 µm with peak heat flux of 6000 W cm^{-2} to 24 000 W cm^{-2} applied in a square wave pattern with *on-time* of 0.2 ms and *off-time* of 3 ms. The safe operating temperature of the device was 250 °C . Their results for the baseline configuration (see Figure 2.7)show that the effective thermal conductivity of the PCM significantly impacts the surface temperature - maximum surface temperature for effective thermal conductivity $k = 50\,\mathrm{W\,m^{-1}\,K}$ is higher than without PCM, but for $k = 400\,\mathrm{W\,m^{-1}\,K}$ it is lower. Essentially, the PCM acts as a thermal insulator due to the relatively low thermal conductivity. These results were validated using two experimental structures - PCMs filled in micro-channels and a diamond heat spreader. A 25 °C drop in peak temperature was obtained in test structure with PCM. Furthermore, PCMs can be used at chip level to sustain system performance under intense computational loads. Microprocessors with multiple cores (found in mobile devices) use dynamic core mitigation (DCM) which throttles the core frequency to limit temperatures [41]. Throttling events increase the computational load and power consumption if the cycling is rapid and present reliability issues [42]. Federov *et al.* [43] showed that increasing the ther-

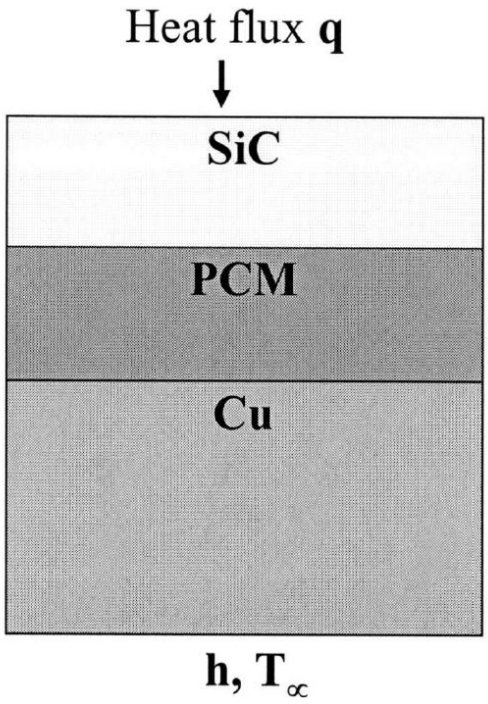


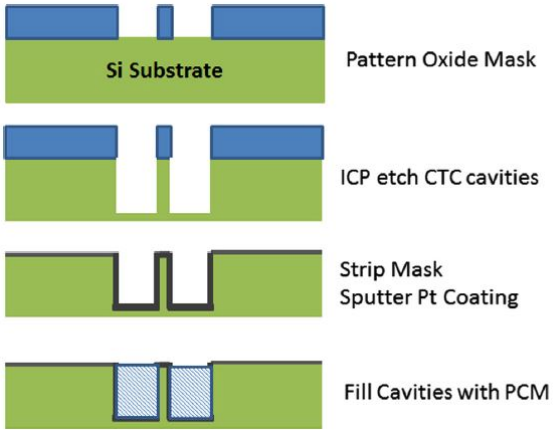
Figure 2.7. 1D stack of the computational model. Metallic PCM (60 µm) is placed between the SiC die (100 µm) and Copper baseplate (2500 µm). To simulate the effect of a steady state heat sink, convection coefficient ($h = 25\,000\,\mathrm{W/(m^2\,K)}$ is applied with ambient temperature ($T_\infty = 50\,^\circ\mathrm{C}$) (Figure reproduced with permission from [40]).

mal capacitance by adding PCM reduced the variations in the temperature, both in time and in space. In their device, the inactive back portion of the chip was etched to remove the substrate and create a cavity to fill PCM as shown in Figure 2.8(a). Following the recommendations of Rocha *et al.* [44], Green *et al.* [43] used a branching structure consisting of eight diamond shaped loops with metallic PCM filled in the void (see Figure 2.8(b)). The time taken to reach the cutoff temperature or the operating time (85 °C) was improved by a factor of 3.5 to 7.5 for heat flux of about $400\,\mathrm{W\,cm^{-2}}$ depending on the PCM volume and proximity to the hot spot. Apart from the heat fluxes, they identified the volume of PCM and the cavity depth as parameters that influence that influence the time taken to reach cutoff temperature.

The PCM with lesser volume but deeper cavity walls increased the operating time more significantly than the PCMs with more volume but less depth. When the melt front traversed the entire thickness of the composite device before throttling temperatures were exceeded , cutoff times increased significantly since the available latent heat was completely utilized.

Computational sprinting is an alternative to throttling down the core frequencies to stabilize temperatures. This is also known as the "dark silicon phenomenon" since not all the cores are active simultaneously - for the 22 nm node, dark silicon is estimated to be 21 % and for the 8 nm node at 50 % [45;46]. This technique improves responsiveness of the processor by boosting the core frequency exceeding the thermal design power (TDP) of the system by a factor of as much as 10 for a very short duration. Shao *et al.* [47] investigated the effect of increased thermal capacitance due to the addition of PCM for computational sprinting. The latent heat of the PCM (49 % Bi, 21 % In, 18 % Pb, and 12 % Sn) acted as a *buffer* - storing energy during peak loads and dissipating it during off-peak times. The performance of PCM was studied for two cases - the composite structure - which comprised of the PCM filled in the etched wells of the die freely suspended in air and *in-situ* - in a smartphone as shown in Figure 2.9. A heater was attached to the back of the CPU to control heat generation (see Figure 2.10). Sprinting state power of 11 W was applied for 0.6 s followed by idling at 10 mW to 20 mW. A temperature drop of 14 °C was observed when compared to a chip without PCM. However, due to additional solidification time of PCM, the temperatures were similar after 60 s which represented a limitation since the next power cycle could only start after complete solidification. However, when the TTC was integrated *in-situ*, due to the existing network of heat spreaders in a mobile device, namely EMI shield and filler material, the solidification time was $\approx$ 15 s. Also, a 55 % extension in sprint duration was observed for a single sprint cycle.

Kaplan *et al.* [48] studied the PCM performance placed on a chip package under standard Android benchmarks. A single board computer (SBC) - a development



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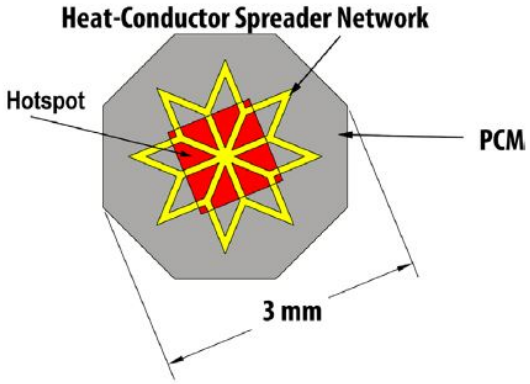


(b)

Figure 2.8. (a) Process steps for filling PCM in Si substrate for fabricating the CTC. The Composite Thermal Capacitor (CTC) is etched to a depth of 190 µm into a 300 µm thick Si wafer from the bottom. A Pt heater (1 mm × 1 mm) is integrated on the top side of the same wafer [43]. (b) Schematic of computational model for performance analysis of CTC. Diamond shaped loops (shown by yellow lines) made of Cu or diamond are used as heat spreaders. The PCM (metallic solder) was filled between the voids of the loops. The design is biologically inspired from the venation patterns of leaves (Figure reproduced with permission from [43]).

board consisting of essential components in a smartphone with a pre-loaded Android operating system. It can be interfaced with a computer and a display. The setup is

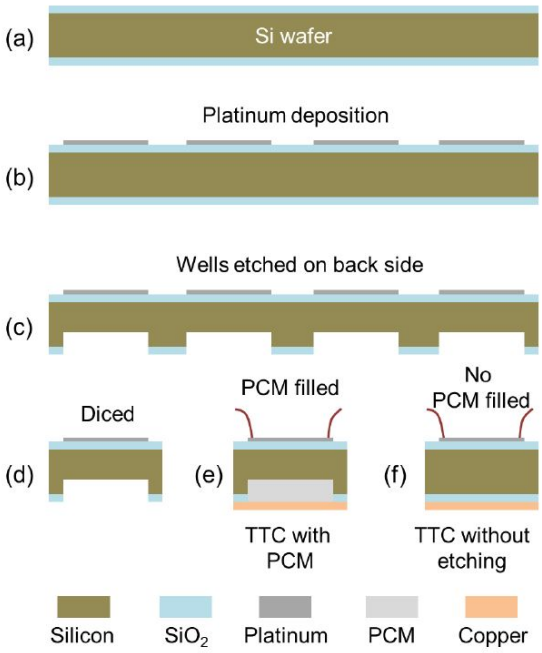


Figure 2.9. (a) - (e) Fabrication process of TTCs with integrated on-chip phase change heat sinks [47]. (a) 2 µm thick layer of SiO_2 is deposited on 101.6 mm thick Si wafer. (b) Ti/Pt thin film heaters and resistance thermometers are patterned using photolithography, e-beam evaporation, and lift-off. (c) - (e) Silicon wafers 0.525 mm thick and 10 mm × 10mm in the cross section are etched on the back side using with cavity depth of 0.2 mm and 8 mm × 8mm cross section by deep reactive ion etching to fill metallic PCM with a transition temperature of 58 °C. (f) TTCs without etched wells and not filled with PCM is used for comparison (Figure reproduced with permission from [47]).

shown in Figure 2.11. The core temperatures were monitored to validate the compact thermal model (based on R-C network). Different strategies of throttling core clock frequencies according to the chip temperatures were compared against a *PCM aware* strategy which estimated the remaining latent heat capacity (solid PCM) from the computational model. The impact of application duration and the threshold set for idling based on latent heat remaining was shown to have significant influence. They found that the PCM-aware strategy outperformed other strategies for relatively long application runtimes by 4.5 %. Also, for *PCM aware strategy*, cores were below the

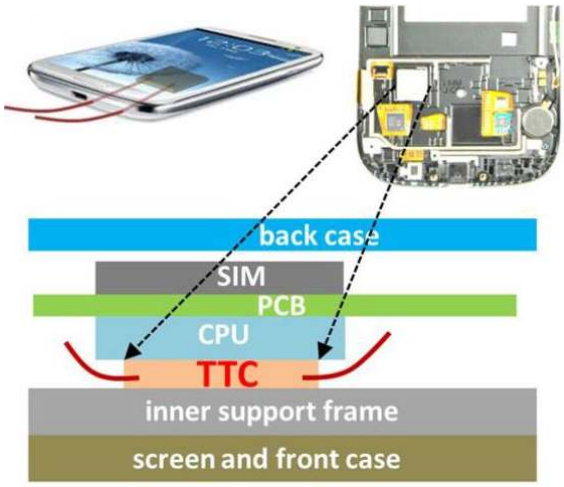


Figure 2.10. Integration of the TTC in a smartphone along with a cross section highlighting the position of the TTC in the thickness direction (Figure reproduced with permission from [47]).

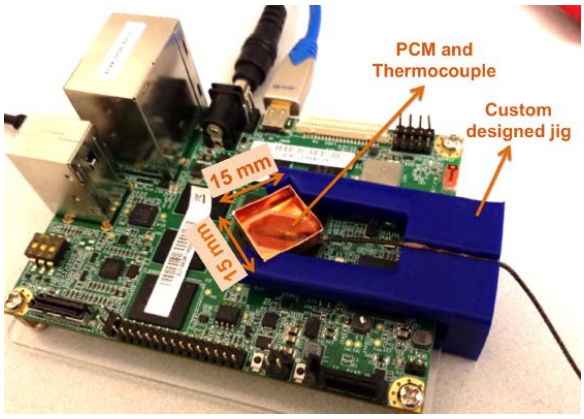


Figure 2.11. Experimental setup for testing impact of PCM on thermal performance of a PCM placed on the chip. Copper box holding Hexacosane PCM, placed on top of the Qualcomm Snapdragon (APQ 8064) die. Arctic Silver 5 TIM is applied between enclosure and die (Figure reproduced with permission from [48]).

cutoff temperature (75 °C) 80 % of the running time and for the frequency based strategy they were below only 36 % of the running time. For shorter benchmarks, the PCM aware strategy reduced the core frequencies even though the core temperatures

did not exceed the cutoff temperatures, hence they performed poorly compared to frequency based strategies.

2.4 Improving PCM Properties

2.4.1 Strategies for Improving Thermal Conductivity of PCMs

PCMs require high thermal conductivity whether used as a TIM, within the heat exchanger, on chip, or inside the package to minimize hotspots (especially if the PCM is placed near the package). Several strategies for improving the thermal conductivity of PCM based TIMs (discussed in Section 2.2), This section gives on overview of thermal conductivity enhancement techniques found in literature. Several strategies have been investigated including integrating high thermal conductivity fillers([49;50]) or foams [51–53].

The low thermal conductivity of most PCMs can prevent full utilization of the included material as heat does not spread effectively from the hot spot to the unmelted portion of the PCM. Bentilla *et al.* [35] compared the performance of metallic fillers - foams, wool, and honeycomb structures - for thermal conductivity enhancement. Honeycomb structures were most effective because of the larger surface area is in contact with PCM, compared to wool and foams. Chintakrinda *et al.* [54] compared the effectiveness of different thermal conductivity enhancers (aluminum foam, graphite foam and graphite nanofibers infiltrated with paraffin wax) with applied heat fluxes varied from $1.93\,\mathrm{W\,cm^{-2}}$ to $19.3\,\mathrm{W\,cm^{-2}}$ at the base. The foams were bonded to an aluminum baseplate and enclosed in a cubical container as shown in Figure 2.12. Natural convection effects (in the form of Rayleigh-Bernard currents) were observed for pure paraffins which caused a more uniform temperature distribution along the thickness. Conduction dominated heat transfer for infiltrated PCMs since clear temperature gradients were observed in the temperatures measured at the top and bottom of PCM. The baseplate (between the heater and the PCM housing) temperatures at different times, the temperature difference between the top and

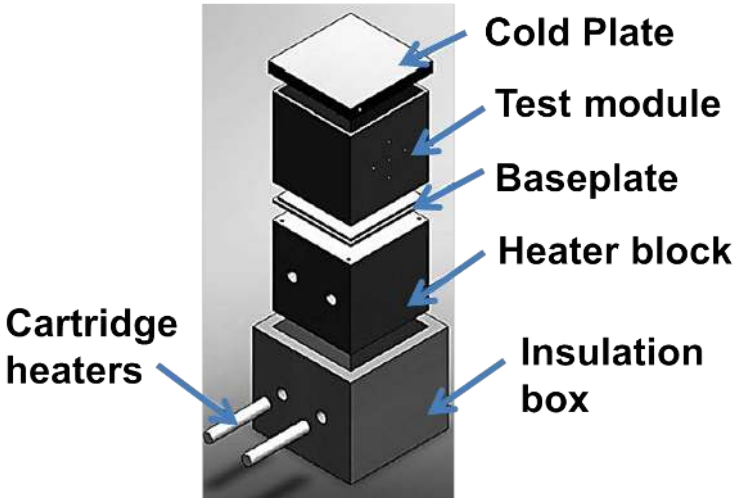


Figure 2.12. Experiment setup to compare performance of pure paraffin wax with paraffin enhanced with graphite nanofibers. The PCM is placed in a leak proof test module and has a volume of about 131 cm^3. The cold plate is kept below the phase change temperature at all times. The primary heat flow direction is from the bottom to the top. However, fin effects are observed due to high conductivity of Al sidewalls (Figure reproduced with permission from [54]. Copyright ©2016 Elsevier Masson SAS. All rights reserved).

bottom of PCM, and the time taken to melt were used as metrics for comparison. The graphite nanofiber - PCM composite showed the greatest delay in time taken to melt. However, the temperatures at the base were as high as pure paraffins for high heat flux. The graphite foam PCM composite (with higher thermal conductivity) had the lowest baseplate temperatures at these heat fluxes. These results highlighted the importance of thermal conductivity in design of PCM infiltrated heat sinks. Several researchers [55; 56] have reviewed thermal conductivity enhancement techniques for PCMs in detail.

2.4.2 Strategies for Improving Latent Heat Storage of the PCM

To minimize the volume required for PCMs, high latent heat per unit volume is desirable. Further, materials throughout the heat spreading network could be leveraged as heat storage locations if their latent heat is increased. One method for increasing the latent heat of a material is to embed encapsulated particles of PCM. Encapsulation is a process which involves surrounding the central core which comprises of the PCM with a shell (metallic or polymer). Conventionally, encapsulated PCMs in a carrier fluid were used as a two-component heat transfer fluid in a closed circulating loop for machining applications [57]. As an example, studies by Fossett *et al.* [58] used micro-encapsulated PCM of 30 µm to 50 µm diameter for avionics cooling. The design criteria for cooling system was environmental temperature of 71 °C and operating temperature of 95 °C. The performance of these micro-encapsulated PCMs was compared against PCM infiltrated with aluminum foam and a solid aluminum baseplate as shown in Figure 2.13. The transient temperature curves of micro-encapsulated PCM and aluminum foam infiltrated PCM agreed well. An added advantage of micro-encapsulation was a 9:1 weight reduction when compared with an aluminum heatsink. Jackson *et al.* [59] characterized and investigated the performance of micro-encapsulated PCM (Octacosane) of 10 µm to 30 µm diameter and observed a 16 % drop in surface temperature as compared to a sensible (no phase change) fluid. A review of synthesis and flow characteristics of micro-encapsulated phase change material is given by Zhang *et al.* [60].

2.5 Conclusions

Significant research efforts are focused on application of PCMs in electronic devices in the last 30 years due to their ability to dampen temperature spikes. Several integration strategies have been developed depending on the geometry, power profiles and mode of heat transfer from the source. Understanding these strategies help

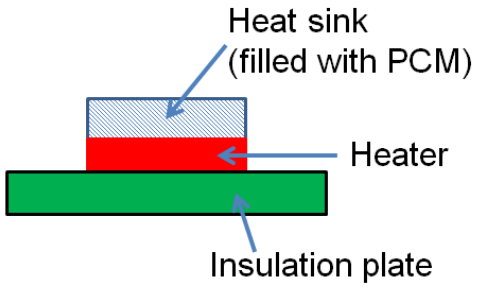


Figure 2.13. Experiment setup to investigate the effectiveness of a micro-encapsulated PCM (Micro-PCM 143) placed between Al fin and infiltrated in a sintered Al foam. A constant power of 90 W is applied for a maximum of 10 min. The base area of the heat sink and the heater is 12.7 cm × 22.9 cm. The mass of both, the unfilled fins and unfilled foam is equal (500 g) and 250 g of PCM is added. (Adapted from [58]).

in identifying key metrics to establish design guidelines for PCM passive thermal management system.

PCM based TIMs have the benefit of no pumpout and improved contact over conventional TIMs since their viscosity decreases when transition temperature is exceeded. However, the low thermal conductivity which results in localization of heat and high pressure requirement over thermal grease to keep them in place offsets the advantages mentioned above to some extent. Another strategy involves using PCM in conjunction with a heat exchanger setup (e.g.radiators in a spacecraft). The PCM can either be placed on top of the heat dissipating component to absorb all the heat or placed between fins to aid in the heat transfer process. Adding a PCM enables the design for average heat loads rather than peak loads which results in overall weight reduction of the system. PCMs can be used for short duty cycle power profiles since maximum weight savings are obtained based on conduction only phase change analysis. Natural convection effects in the melt region which enhance heat dissipation should be maximized during the design of a PCM based system. The significance of natural convection effects is indicated by the Raleigh number which is strongly influ-

enced (proportional to the third power) by the characteristic length of the system. PCMs can also be integrated on the chip package, which is closer to the primary heat source. This finds application in devices with thickness constraints. They are used in short duty cycle (on time of 2×10^{-4} s to 0.6 s) high peak loads ($6 \times 10^{3}\,\mathrm{W\,m^{-2}}$ to $24 \times 10^{3}\,\mathrm{W\,m^{-2}}$). These loads, which are usually 10 times the allowable thermal design power of the system are applied in bursts to improve the responsiveness of the device. PCMs are also compatible with "soft" thermal management strategies used in consumer electronics which limit the clock frequencies if a temperature threshold is reached. PCM are more suited to longer benchmark runtimes if a strategy that estimates the unmelted PCM mass is used. This creates a conservative scheme since clock frequencies are reduced even if the core temperatures are not exceeded. Actual integration in a mobile device involves optimizing the thermal management strategy to ensure that the PCM remains unmelted for a longer duration and considering the influence of structural components on the temperatures of the PCM and the die.

Thermal conductivity of PCMs can be enhanced through adding metallic fillers or encasing PCMs in fins and honeycomb structures to name a few. Honeycomb structures had the highest surface area in contact with the PCM and hence are better than impregnating the PCMs with metallic fillers. However, often the limited form factor of devices precludes the use of honeycomb structures or fins. Graphite nanofibers outperformed metallic fillers and are a promising alternative for honeycomb structures. Micro-encapsulated PCMs used in a heat transfer fluid (which acts as the carrier) or embedded in foams led to a drop in temperature and weight savings.

2.5.1 Key Challenges for PCMs

Based on the literature review, key challenges are identified and motivate the thermal analysis in this thesis.

- Enhancing thermal properties of PCMs also requires high-fidelity measurements of their performance.

- Typically, enhancing the thermal conductivity decreases the heat storage capability of a thermal energy storage system. Hence these properties need to be tuned according to the design constraints.
- The thickness of the PCM plays a crucial role since a PCM with greater thickness can act as an insulator leading to formation of temperature hotspots which adversely affect the device performance and eventually reduce the reliability.
- Mobile devices have complex networks for heat spreaders and minimal volume for integrating PCM. Models and measurements are required to understand the best strategies and locations for integrating the PCMs in the system.

CHAPTER 3. THERMAL RESISTANCE OF PCMS

Chapter 3 derives predominantly from the following published manuscript: Ganatra and Marconnet [17]

Y. Ganatra and A. Marconnet. Passive Thermal Management Using Phase Change Materials: Experimental Evaluation of Thermal Resistances. In *ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems collocated with the ASME 2015 13th International Conference on Nanochannels, Microchannels, and Minichannels*. American Society of Mechanical Engineers, 2015

3.1 Background

Passive cooling techniques use a combination of heat spreaders, thermal interface materials and thermal vias to move and store the heat within the device. Size and weight constraints in embedded or mobile systems can preclude the use of active cooling techniques, ensuring that all generated power must be dissipated by natural convection and radiation from the case. This limitation imposes restrictions on device performance often meaning that only a fraction of transistors are active at a given time. Runtime thermal management techniques, which monitor thermal behavior, optimize operating parameters of processor, and predict temperatures, have emerged as a consequence of this thermal bottleneck [61].

Thermal interface materials (TIMs) are often fabricated from low thermal conductivity polymers infiltrated with high thermal conductivity fillers. Low manufacturing costs and increased robustness of semiconducting polymers has made them a promising technology [62] and inorganic polycrystalline polymers have received much emphasis, especially semiconducting polymers which have improved charge transport

characteristics compared to most polymers. Additionally, recent work has shown that highly disordered or amorphous polymers perform as well as semicrystalline materials for photovoltaic applications [63]. The increased electrical performance of all of these materials compared to conventional polymers could also yield improved thermal properties making them intriguing for thermal applications. Noriega *et al.* [64] developed a unifying framework for charge transport which can also influence thermal transport. Bulk polymers generally have low thermal conductivity on the order of $0.1\,\mathrm{W\,m^{-1}\,K}$ [65] . But recent work has reported high thermal conductivity in individual nanofiber of polyethylene of order of $100\,\mathrm{W\,m^{-1}\,K}$, which is higher than many metals [66]. If the high thermal conductivity of the individual molecular chains that form the backbone of many polymers could be exploited in a more bulk format, polymers could prove useful as thermal interface materials.

Traditional TIMs are designed to fill the gaps between heat sink and chip thus reducing contact resistance. For passive thermal management applications, we consider polymers which undergo a gel-to-solid or amorphous-to-crystalline molecular state transition upon heating and cooling allowing energy to be absorbed through the latent heat of phase change, without pumpout and other issues associated with PCMs that melt. Furthermore, these materials are particularly interesting for passive thermal management because the high temperature state may have higher thermal conductivity. Thus, heat could be removed effectively during the state transition due to the enthalpy of phase change and continue to be transported effectively at the higher temperature state.

In short, simulations and experiments have demonstrated that integrating PCMs into electronics cooling systems can allow increased computational performance while stabilizing temperature in the system. However, materials properties including thermal conductivity in the low and high temperature state, the latent heat of phase change, and heat capacity contribute to performance. Furthermore, different integration schemes for including PCMs may require different materials. This chapter focuses on a developing a new strategy for measuring the thermal resistance of PCMs.

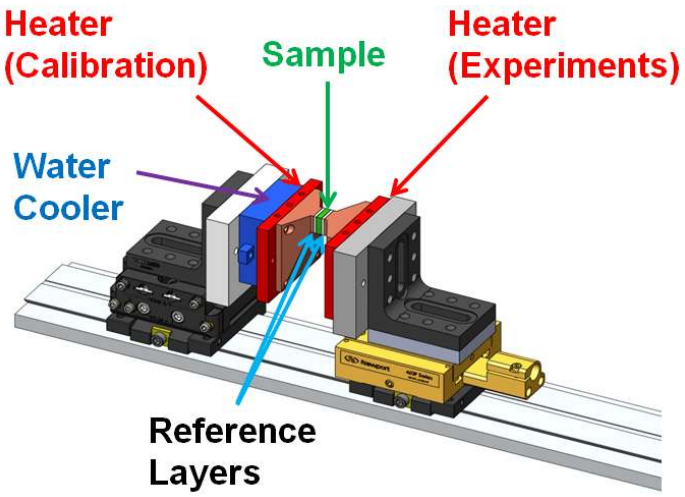


Figure 3.1. Schematic of the miniature IR thermal conductivity measurement rig. The sample is sandwiched between two reference layers of known thermal conductivity. Copper adapter plates, which are in contact with the cartridge heaters, are located adjacent to the reference layers. A water cooling system is attached to one side. Initially, the entire setup is heated to a constant reference temperature for emissivity calibration after which, a temperature gradient is created using the water cooler.

3.2 Experimental Procedures

In the conventional reference bar method [67], an unknown sample is sandwiched between long bars of a known reference material. Several thermocouples are placed along the length of the reference material to measure the heat flux through the sample and the measured temperature gradient is extrapolated to the sample location to estimate the thermal conductivity or total thermal resistance of the sample. For a single sample, it is impossible to separate the contact resistance from the intrinsic sample thermal conductivity and often several thicknesses of "identical" samples are measured to separate out these two effects.

In contrast, the miniature infrared (IR) reference bar method (see Figure 3.1, and Figure 3.2, Table 3.1) used in this work non-invasively measures two-dimensional temperature maps across the entire reference-sample reference stack. Compared

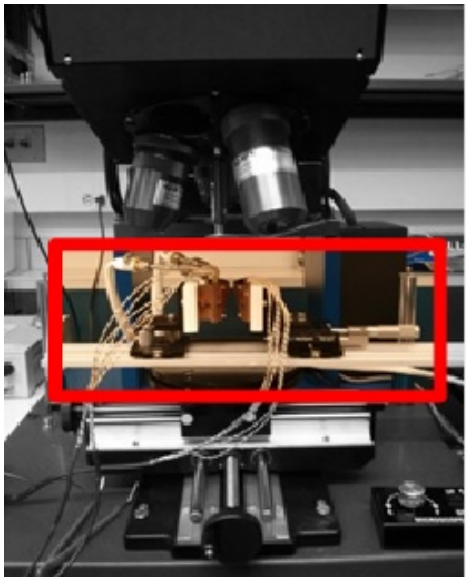


Figure 3.2. Miniature IR thermal conductivity measurement rig mounted on IR microscope stage. The components of thermal conductivity rig (in color and enclosed by red outline) are shown in Figure 3.1.

Table 3.1.
Dimensions and material properties of thermal conductivity rig components.

Component	Material	Dimensions (L x B x H) (mm)	Thermal Conductivity (W/(m K))	Density (kg/m^3)
Adapter plate	Copper	$40 \times 40 \times 3$	390	8900
Cooling system plate	Copper	$40 \times 40 \times 10$	390	8900
Heater plate	Copper	$60 \times 40 \times 6$	390	8900
Insulation Plate	MACOR®	$80 \times 45 \times 14$	1.46	2520
Reference	Fused Silica	$10 \times 10 \times 1.5$	1.4	2201

to the conventional method, the reference layers are much thinner ($\approx 1\,\mathrm{mm}$) and the material for the reference layer is chosen to have a thermal resistance ($R'' = L/k$ in $\mathrm{cm^2\,K\,W^{-1}}$) on the same order of the sample. A high spatial $1.7\,\mu\mathrm{m}$/pixel to $11.7\,\mu\mathrm{m}$/pixel and temperature ($\approx 0.1\,\mathrm{K}$) resolution IR microscope (Quantum Focus Instruments,Vista,CA) records the two-dimensional temperature map when a heat flux is passing through the sample and the thermal conductivity of the sample (reflected in the temperature gradient within the sample) can be spatially separated from interface effects (which appear as jumps at boundaries between materials) [68; 69]

In this method, the sample is sandwiched between fused silica reference layers forming the Reference-Sample-Reference. Two reference layers are required to quantify the heat flux and accurately account for heat losses to the surroundings. To prevent sample contamination, no coating is applied on the surfaces. Cartridge heaters (Watlow® Firerod C1J5) embedded in copper heater plates on either side of the Reference-Sample-Reference stack heat the sample stack to a uniform temperature during emissivity calibration. For calibration, the Reference-Sample-Reference stack is heated from both sides to $40\,^{\circ}\mathrm{C}$, which is less than the melting point of the samples. A reference radiance image is taken which compares the radiance at each pixel with a blackbody at the same temperature. This corrects for non-ideal emissive properties of the surface, accounts for variations in the surfaces of the sample, and allows measurement of multiple materials with different emissivities in one image. High thermal conductivity copper adapter plates taper from the large cross section heater plate to the smaller cross-section of the sample to ensure one-dimensional heat transfer through the sample stack (see Figures 3.1, 3.3(b)). Future work will include geometry optimization of the adapter plates to minimize cross plane temperature variation. After calibration, the cooling system is switched on and maintains the cold side temperature at $\approx 24\,^{\circ}\mathrm{C}$, while the heater power to the other side is adjusted to establish the desired temperature differential. The measurement is repeated at several different applied powers, and the thermal conductivity and interface resistances are extracted from the power-dependent results. Phase change is also recorded by movies of the

temperature and radiance maps. This entire measurement rig is supported by two linear stages to accommodate samples of different sizes and allow variations in the pressure applied across the sample. The stages are isolated from the heated and cooled regions using Macor ® insulation. Since heat flow is one-dimensional across the Reference-Sample-Reference stack, the thermal conductivity of the sample is determined by computing the heat flow across the three layer stack [70]. For uniform cross-sectional areas, the relationship between the temperature gradient in each layer i and temperature jumps at an interface are given by Equation (3.1)

$$q_i'' = -k_i \frac{dT_i}{dx_i} = \frac{\Delta T_{int}}{R_{int}}. \tag{3.1}$$

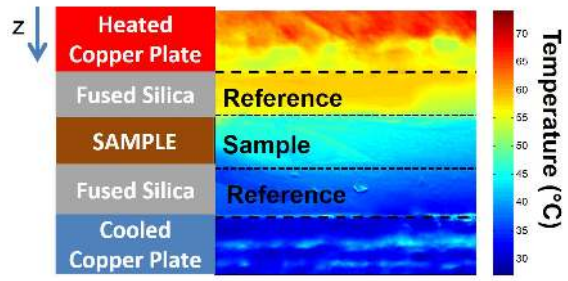
where q'' is heat flux in x-direction k_i is thermal conductivity $\frac{\mathrm{d}T_i}{\mathrm{d}x}$ is temperature gradient in i^{th} layer, ΔT_{int} is the temperature jump at an interface and R_{int} is the thermal resistance of the interface $\mathrm{m^2\,K\,W^{-1}}$. Thus, the ratio of the thermal conductivities of the sample and reference regions related to the temperature gradients in each region as shown by Equation (3.2)

$$\frac{k_{sample}}{k_{ref}} = \frac{(\frac{\mathrm{d}T}{\mathrm{d}x})_{ref}}{(\frac{\mathrm{d}T}{\mathrm{d}x})_{sample}}. \tag{3.2}$$

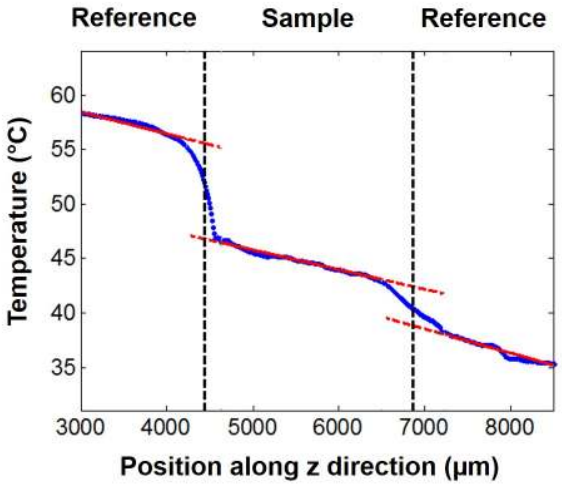
and the interface resistances can be calculated from Equation (3.3)

$$R_{int}'' = \frac{\Delta T_{int}}{-k_{ref}\,(\frac{\mathrm{d}T}{\mathrm{d}x})_{sample}}. \tag{3.3}$$

Figure 3.3 shows an example temperature map and 1-D averaged temperature profile for an average sample temperature near 45 °C for a commercial phase change thermal interface material (Chromerics Thermflow ™T766-06) [71] which has phase change temperature range from 51 °C to 58 °C. The sample contains a non-adhesive metal foil carrier on one face which faces the heater and the adhesive PCM faces the water cooling system. In Figure 3.3, the sample is still completely solid and has not experienced phase change. From these temperature maps, a total thermal resistance of the TIM ($R_{tot}'' = R_{int,hot}'' + \frac{L}{k} + R_{int,cold}''$) of $13\,\mathrm{cm^2\,K\,W^{-1}}$ (in the solid state) can be extracted and separated into three components: the PCM material with



(a)



(b)

Figure 3.3. (a) Two dimensional surface temperature map with Chromeric T766 TIM as the sample. The corresponding regions of the cross plane model are shown on the left. Spatial surface temperature maps obtained from IR thermal imaging. The emissivity calibration for the setup is done at 40 °C. (b) Averaged one-dimensional temperature profile of a cross section of TIM sample near the vertical centerline between two reference layers. The red dashed lines linearly fit the temperatures in the reference and sample layers. Temperature jumps at interfaces are clearly visible in the averaged temperature profile in addition to the linear region in the sample region. Thus, the interface resistances can be spatially separated from the thermal conductivity of the sample.

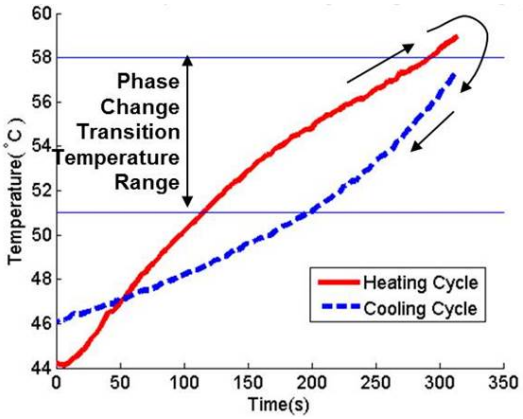


Figure 3.4. Temperature history of T766-06 TIM during thermal cycling. The mean temperature of a small region of interest around the center of the sample is plotted with time. During heating, phase change occurs over a range of temperatures (51 °C to 58 °C) as indicated by blue reference lines, but during cooling the impact of phase change is not as obvious indicating the freezing temperature depressed. Arrows indicate that after the sample was fully heated the material was subsequently cooled.

an intrinsic thermal conductivity of $0.3\,\mathrm{W\,m^{-1}\,K}$ and interface resistances of $R''_{int,hot} = 0.30\,\mathrm{cm^2\,K\,W^{-1}}$ and $R''_{int,cold} = 6.19\,\mathrm{cm^2\,K\,W^{-1}}$. Additionally, two-dimensional effects can be observed through the variations in temperature along each vertical column of pixels due to non-uniformities in the sample and contact conditions.

Upon further heating of the hot side, melting occurs in a localized manner around "hot spots" with temperatures greater than melting temperature along the sample-reference interface on the hot side. Figure 3.4 shows the evolution of the temperature profile using two different cycles which is tracked by recording using the movie mode in IR-Microscope. For the heating cycle, initially, the heater power is raised such that temperature exceeds the phase change temperature range, after which the heater is switched off (cooling cycle). The variation of thermal resistance during these cycles is summarized in Table 3.2. The effective thermal resistance is reduced during phase change (compared to when the sample is fully solid). Also, after fully melting the thermal resistance is reduced by $\approx 50\,\%$ and remains at this reduced value throughout

Table 3.2.
Thermal Resistance (cm^2 K/W) for heating and cooling cycles for temperatures between and below (solid state) phase change temperature range.

Cycle	During phase change	Solid
Heating	11.0	13.1
Cooling	6.7	6.6

cooling. This is due to improved contact at the interfaces of the TIM after melting that persists even during resolidification, as well as a reduced bond line thickness. Spatially varying temperature gradients in the sample induce stresses which often lead to pump out of the thermal interface material after melting. After resolidification, the thickness of the TIM remaining in between the two reference layers has reduced such that the film remaining is semi-transparent (as compared to a fully opaque layer before testing). This result highlights the need to control and confine the sample during the melting and re-solidification process, as well as a potential advantage of the dry PCMs which never fully liquefy.

3.3 Transient Analysis

The above analysis of thermal resistance is valid under the assumption of steady state conditions. Phase change is a transient process and involves absorption (during melting) or release (during solidification) of heat during phase change. Hence, the heat flux on either side of the melt (or solidification) front are unequal. A 2D COMSOL simulation is done to study the validity of this method for a transient process like phase change. The reference layers (each 1 mm thick) are acrylic plastic and the sample (2 mm thick) is paraffin wax with a thermal conductivity of $0.2\,\mathrm{W\,m^{-1}\,K^{-1}}$ and $0.21\,\mathrm{W\,m^{-1}\,K^{-1}}$, respectively. For acrylic, built-in thermophysical properties (see Table 3.3) are used. A heat flux of $4.8 \times 10^3\,\mathrm{W\,m^{-2}}$ is applied on the left edge of the sample and the right edge is held at a constant temperature of 20 °C since it is

Table 3.3.
Material properties for reference (acrylic plastic) and sample layers. Paraffin wax PCM is used as the sample with a latent heat of $2.092 \times 10^5\,\mathrm{J\,kg^{-1}}$, transition (melting) temperature of 324.5 K, and a transition temperature range of 10 K (See Section 6.5.2 for details about modeling phase change in Comsol).

Component	Thickness (mm)	Thermal conductivity (W/(m K))	Specific Heat (J/(kg K))	Density ($\mathrm{kg/m^3}$)
Acrylic Plastic	1	0.18	1470	1190
Paraffin Wax	2	0.21	800	3046

directly connected to a cooling loop. The top and bottom edges are assumed to be insulated since convection effects are neglected. A transition (or melting) temperature of 324.5 K and transition temperature range of 10 K was used for the PCM. The simulation duration is sufficiently long that steady state is achieved by the end of the simulation. Specifically, the temperature remains unchanged after about 426 s (see Figure 3.5).

Initially, due to sensible heating and finite speed of heat transfer through the reference layer, the hot side temperature gradient is larger than the cold side gradient (see Figure 3.5). As phase change begins to occur, the difference in the flux on either side of the sample is due to a combination of the sensible heating effect and the absorption of energy to move the phase change front. Eventually, a steady-state is reached as seen by the reduced spacing between the temperature profiles at different times. To probe the accuracy of the quasi-steady state analysis conducted in the previous section, the transient variation of thermal resistance computed using (1) average heat flux, (2) hot side heat flux, (3) cold side heat flux, and (4) thermal conductivity of sample, as shown in Figure 3.6. The average heat flux is computed by taking the average of the hot and cold side temperature gradients. The hot side

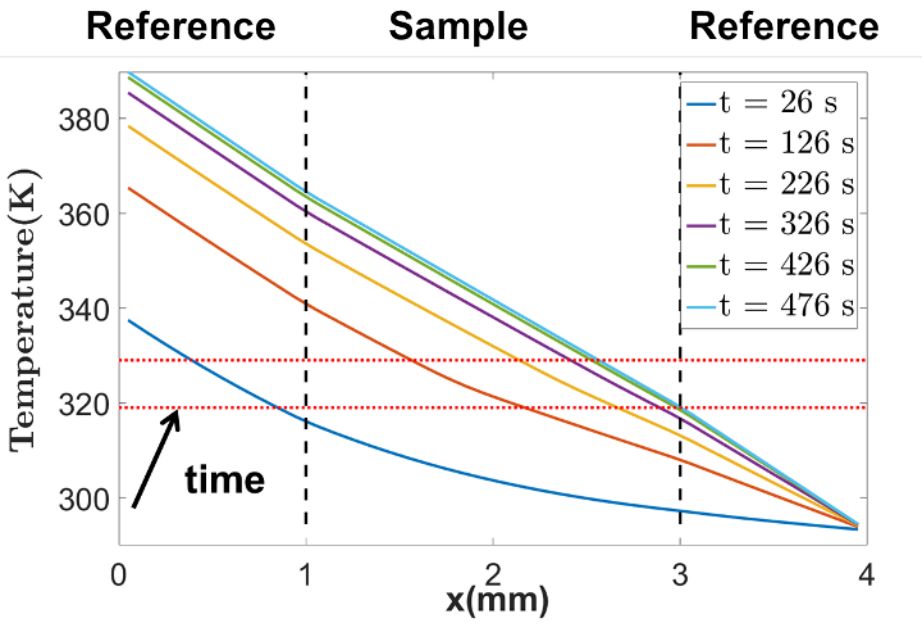


Figure 3.5. Temperature profile from a 2D COMSOL simulation along horizontal centerline of reference - sample - reference stack (see Section 3.2) for different times. The red horizontal dotted lines represent the transition temperature range. A heat flux of $4.8 \times 10^3\,\mathrm{W\,m^{-2}}$ is applied on the left edge and the right edge is held at a constant temperature of 20 °C. As time increases the temperatures tend to a steady state as the spacing between successive lines reduces. Initially, the hot side temperature gradient is greater than the cold side due to sensible heating and phase change. With time, the cold side temperature gradient increases ultimately reaching steady state conditions after about 426 s seconds. Note that even in the absence of phase change, it takes some time for heat to propagate through the sample stack. The temperature gradients are used to calculate the heat flux and subsequently thermal resistance as shown in Figure 3.6.

and cold side heat fluxes are determined by considering either hot and cold side temperature gradients. For each approach, the thermal resistance is calculated by

$$R_{th} = \frac{\Delta T}{q''}. \tag{3.4}$$

For comparison, the thermal resistance is also calculated from approximately linear temperature gradient in sample and average heat flux in both the reference layers

(see "calculated" line in Figure 3.6). The heat flux flowing across both hot and cold side reference layers are unequal, as expected. Since heat is absorbed during melting, heat flux through the cold side reference layer is lower than the hot side reference layer. Thus, the thermal resistance is apparently as much as 6 times larger than the cold side layer during the heating process. The difference in heat flux between the reference layers decreases as the temperatures tend to a quasi steady state, which indicates that the steady state measurements discussed in the preceding sections are valid once a quasi steady state is established.

3.4 Conclusions

This chapter focused on a testing method developed to characterize performance of dry PCMs for thermal management applications. Namely a miniaturized infrared microscopy version of the standard reference bar method was presented as a compact system for evaluating thermal resistance and phase change behavior of these complex systems. Preliminary results for a commercially available phase-change thermal interface material demonstrated the efficacy of the technique and illustrated that pump out of conventional PCMs which melt was a major issue.

The last section explored the viability of this technique for PCMs due to the transient nature and energy absorption or release during phase change process through COMSOL simulations. Thermal resistances were computed by taking the average of hot and cold side temperature gradients, considering only the hot and cold side temperature gradients in both the reference layers separately. The temperature along the horizontal centerline cutting along reference - sample - reference stack reached a quasi steady state after an initial variation due to sensible heating effects. The apparent thermal resistance as viewed from the cold side reference layer was greater than the hot side since the heat flux flowing across the hot side was higher than the cold side. The difference between the hot and cold side temperature gradients re-

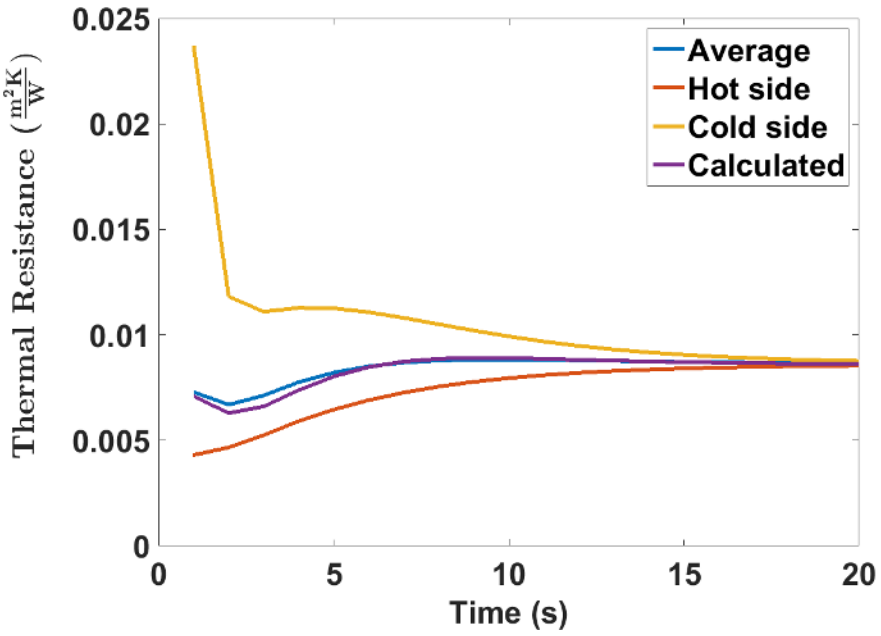


Figure 3.6. Transient variation of thermal resistance calculated from temperature gradient. The gradient is computed as follows (1) Average - average of hot and cold side temperature gradients from known temperature drop and thickness of sample , (2) Cold - only cold side temperature gradient used, (3) Hot - only hot side temperature gradient used, and (4) Calculated - thermal resistance is computed from approximately linear temperature gradient in sample and average heat flux in both the reference layers. The apparent hot side thermal resistance is initially lower than that calculated from the cold side as some heat that flows into the PCM is absorbed in the phase change process and the finite propagation speed of heat through the sample stack. Thus, the heat flow out the cold side is always smaller than the heat flow in from the hot side. Both the hot and cold side thermal resistance tend to the average thermal resistance as steady state is approached.

duced with time and they matched the thermal resistance obtained by taking average temperature gradients of both the reference layers.

CHAPTER 4. PHASE CHANGE PROPERTIES OF PCMS

This chapter discusses the characterization of select thermophysical properties like latent heat and transition temperature of PCMs used in the computational models (discussed in Chapter 7) and *in situ* tests. The PCMs used for *in situ* tests were obtained from Entropy Solutions LLC, Plymouth, MN (brand PureTemp) and Sigma-Aldrich, St.Louis, MO. The PureTemp-42 PCM (transition temperature 42 °C) was wax-based since it had similar properties to wax but enhanced with fillers to increase the thermal conductivity [72]. The other PCM was unenhanced paraffin with a transition temperature of 62 °C. The datasheet from the manufacturer was unavailable and we assumed that it had properties identical to the paraffin used by Kandasamy *et al.* [73]. To identify key parameters, wide range of commercial PCMs such as metallic solder based, wax based and enhanced with metallic and graphitic fillers and unenhanced paraffin (obtained from Frank Ross Company) were used in the computational models (properties listed in Table 7.3). The properties of metallic solder were used from the datasheet [74] and not characterized. Phase change was modeled using the Apparent heat capacity method (discussed in Section 6.5.2) where the effect of phase change was modeled as a sharp spike in specific heat over a finite range of temperature known as the transition temperature range. This range and the latent heats of PCMs were determined from Differential Scanning Calorimetry (DSC) tests [1]. A heating rate of 1 °C min^{-1} was used for all samples. The samples were cycled from 20 °C to 100 °C. The results from the first cycle were discarded since it was used to erase the (unknown) thermal history of the sample. The measurement error is estimated to be 10 %.

[1]DSC curves were obtained with the assistance of Alex Bruce, PhD candidate in Materials Engineering, Purdue University working with Dr. John Howarter.

A typical DSC curve plots the heat flow (in $\mathrm{mW\,g^{-1}}$) on the y-axis with the temperature or heating rate. For endothermic transitions like melting, the heat rate is negative since energy is consumed by the sample to change phase. At the molecular level, this inflow of energy causes the bonds to break which enables phase change. For solidification, the transition is exothermic and the heat flow is positive since energy is liberated since the inter-molecular distance is reduced. The DSC curve for PureTemp PCM [75] with a reported transition temperature of 68 °C is shown in Figure 4.1. The red line represents the heating curve where the sample is heated till 100 °C and then cooled down (shown by the blue line). The two peaks represent transition temperatures during melting and solidification. The difference between the transition temperatures during heating and cooling cycles is because of undercooling. Solidification is initiated from nucleation sites which include container walls,impurities or voids in the sample. In the absence of these nucleii, the liquid phase can be maintained throughout. Since the PCMs are comprised of multiple constituents (base material + fillers) which serve as nucleation sites, they solidify with a relatively low degree of undercooling. All the PCMs tested had a degree of undercooling of less than 5 °C. Multiple transitions can be represented by multiple peaks on the heating and cooling curves. PCMs infiltrated with graphitic materials (from All-Cell technologies [76]) exhibit multiple transitions. Multiple transitions imply that a mixture of PCMs are present. For example, for paraffins, the melting point is directly proportional to the chain length of the hydrocarbon. A mixture of waxes would exhibit multiple peaks because of different transition temperatures of individual components. Also, mixtures are usually represented by broad asymmetric peaks. A sharp change in slope of the constant heat flow lines signal the start and end of phase change. The transition temperature range is determined from the from the length of the extrapolated constant heat flow line at the base of the peak. The latent heat is determined from the area under the peak as shown in Figure 4.2.

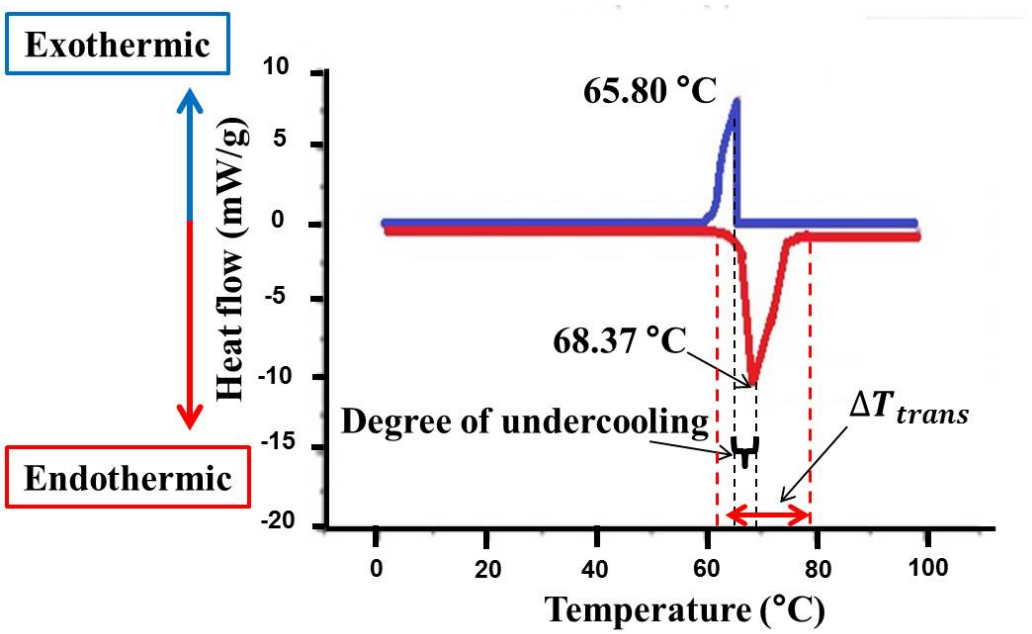
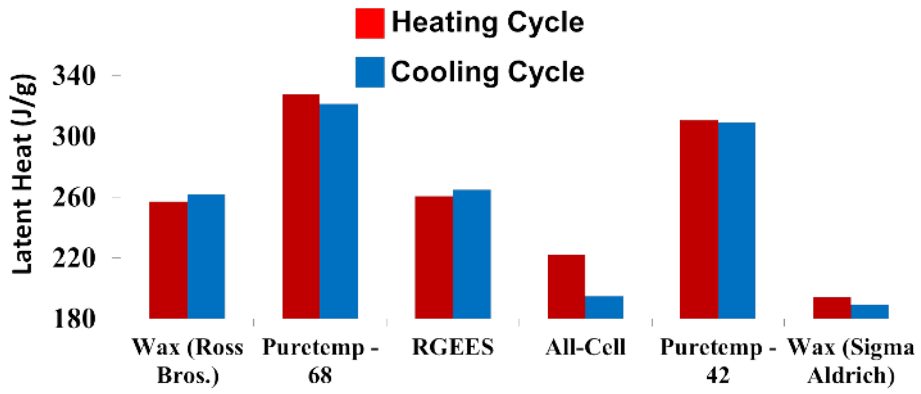
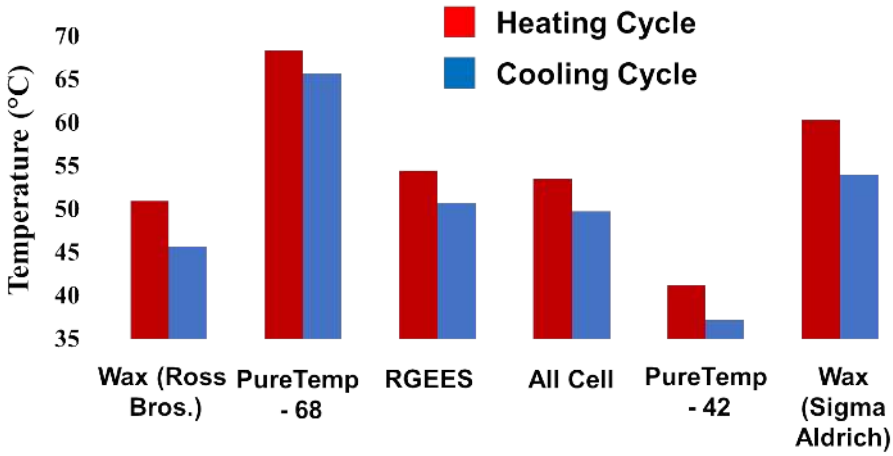


Figure 4.1. DSC Curve for PureTemp PCM with a reported transition temperature of 68 °C. The red line represents the heating curve and the blue line represents the cooling curve. A heating rate of 1 °C min^{-1} is used and the PCM is cycled to 100 °C. Melting is an endothermic process and the transition temperature (during heating) is the peak of the heating curve. The transition temperature during cooling can be determined in a similar way. The difference in transition temperatures between heating and cooling cycle is because of undercooling. The asymmetric peaks indicate that the PCM is a mixture. The transition temperature is determined from the width of the base of the heating curve. The area under the peak gives the latent heat.



(a)



(b)

Figure 4.2. Characterization of select thermophysical properties of PCMs. The first four PCMs are used in the simulations in Chapter 7 to identify key parameters involved in design of PCM based system for temperature stabilization. The last two PCMs (Purtemp - 42 and Wax from Sigma Aldrich) are used in experiments in Chapter 5. (a) Latent Heat during heating and cooling cycle. The PureTemp PCM has the highest latent heat, while the All-Cell PCM has the lowest due to presence of high conductivity fillers.(b) Transition temperatures of PCMs during heating and cooling cycle. The transition temperatures of wax (Ross Bros), used in simulations and wax (Sigma Aldrich), used for *in situ* tests are 51 °C and 58 °C respectively. The difference in the transition temperatures between the two cycles is within 5 °C which, indicates that undercooling effects maybe insignificant.

CHAPTER 5. EXPERIMENTAL THERMAL DEVICE CHARACTERIZATION

5.1 Introduction

This chapter discusses *in situ* testing of PCM to study their feasibility in mobile devices. A Single Board Computer (SBC) - an Android based development board, which contains essential components found in a typical smartphone is used. Core temperature profiles are extracted while running Android benchmarks. The PCM is placed in an enclosure which is attached to the die. The impact of enclosure size and material are studied for two PCMs and two benchmarks. Section 5.2 and Section 5.3 discuss the experimental setup and results respectively. The goals of these *in situ* tests are to

- study the feasibility of integrating the PCM on the primary heat source - the die.
- validate the computational model (described in Chapter 7) with a relatively simple experimental setup.

Different enclosure sizes, materials, and PCMs are used to identify key parameters that influence the integration of the PCM. These combinations were evaluated against the time taken to reach cutoff temperature, the maximum temperature, and the weight of the PCM.

5.2 Experimental Setup

The setup consisted of an enclosure filled with PCM placed directly on the die. The enclosure is filled with the PCM by crushing the solid blocks of PCM to a fine powder to ensure maximum fill of the enclosure. The powdered PCM is heated on a hotplate at 90 °C until it is fully melted. Then, it is cooled down under natural

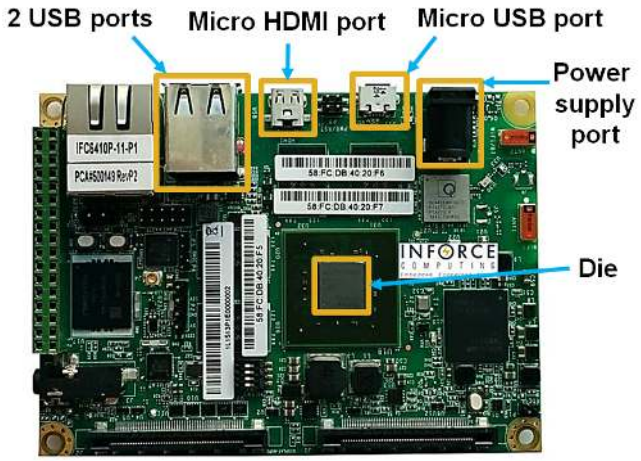


Figure 5.1. Experimental setup and connections of SBC. Key components include the die, which is the primary focus in this work and the GPU. Core temperatures of the die are recorded using a custom script. The SBC is connected to a display via micro HDMI port , and Input/Output via USB ports.

convection while the hotplate remains at a constant temperature of 30 °C. If the PCM overflows, the volume of the PCM is reduced and the process repeated till no PCM leaks out of the container. The containers are made of copper or steel sheets (McMaster Carr, Elmhurst,IL) with a wall thickness of 0.3 mm.

A Single Board Computer (SBC), (see Figure 5.1) is a development board, which contains the essential components in a smartphone - the processor, GPU, memory and, input/output (I/O) laid out on a single Printed Circuit Board (PCB). A SBC is used because it runs Android based benchmarking applications which are configured to stress the processor thus representing worst case realtime usage scenario for a mobile device. Also, since the components are laid out laterally rather than stacked up vertically (a common arrangement in mobile devices), it enables non-contact thermal measurements using infrared (IR) imaging. The SBC (model IFC 6410, Inforce Computing Inc., Fremont, CA) runs an Android 4.0 (“Ice Cream Sandwich”) operating system. It has a Qualcomm Snapdragon APQ 8064 processor, which is modeled in

Section 7.4 of this thesis. The SBC was connected to I/O using USB ports, to a display via micro-HDMI port and to a computer for data acquisition via micro-USB port. A custom script is used to extract core temperatures from eight temperature sensors located on the die and clock frequencies sampled at 60 Hz. The cutoff temperature is chosen as 70 °C because the temperature of the sensor between the GPU and the cores only increases before this limit is reached. Note that the temperatures of other sensors are not logged until the cutoff temperature is reached. The clock frequencies exhibit a similar trend - before the cutoff temperature, the frequency of only the CPU core 0 is greater than the baseline frequency of 384 Hz, while other clock frequencies are less than or equal to the baseline frequency. The maximum clock frequency of all cores is 1728 Hz. Figure 5.2 plots the clock frequencies of all cores filtered using moving average of 2 data points. Until ≈ 20 s , CPU core 0 is dominant. Cores 2 and 3 are mostly inactive (at 0 Hz until the benchmark was started). The start of benchmark test is indicated by a sharp increase in clock frequencies of all cores (at ≈ 20 s). The end time of the benchmark test is also indicated by a sharp decline in clock frequencies of all cores, specially cores 1 to 3 .

The resolution of the temperature sensors is 1 °C. Hence discrete steps due to rounding error are observed towards the end (≈ 850 s) of the benchmark as shown in the region circled in red in Figure 5.3. IR thermal imaging, which is a non-contact technique, is used to measure surface temperatures (as two-dimensional temperature maps) instead of thermocouples. The IR microscope (Quantum Focus Instruments Corporation, Vista, CA) detects wavelengths in mid range of IR spectrum, from 3 µm to 5 µm, using a 1024×1024 InSb focal plane array. The imaging is done at 75 Hz. The temperature and spatial resolutions are 0.1 K and 1.7 µm (at 20x optical zoom). This work used 1x optical zoom, which images an area of about 121 mm^2 with with 11 µm resolution.

To evaluate the impact of the PCM, first two baseline experiments without PCM are conducted: (1) the bare die with no added thermal solutions and (2) the bare die with each empty enclosure. Note that the enclosure itself adds significant thermal

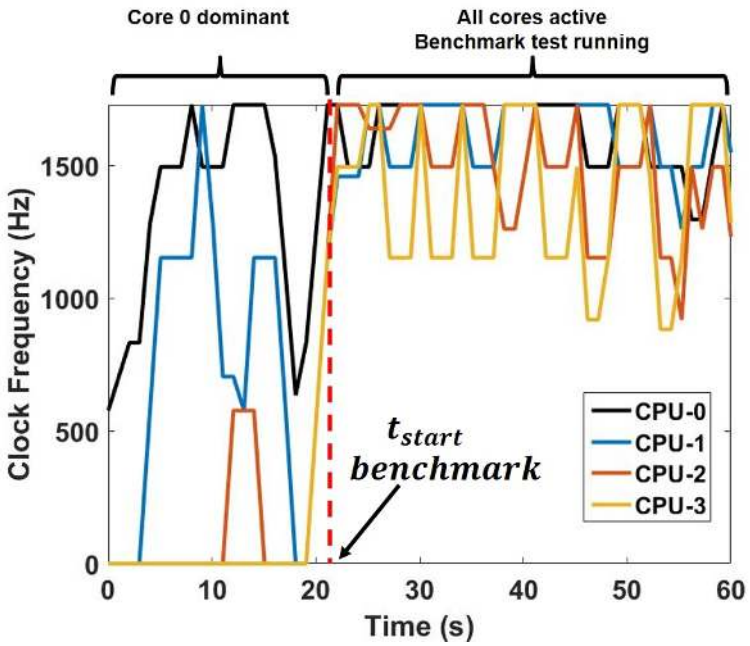


Figure 5.2. Clock frequencies of all cores. Until about 20 s, Core 0 is dominant after which clock frequencies increase rapidly. Cores 2,3 become active after the start of the benchmark.

mass to the system impacting the thermal performance. The enclosure to the die is attached with Omegatherm 201TIM [77].

For the die only experiment, the top surface of the die which is thermally imaged, is coated with graphite spray (The B'Laster Corporation,Cleveland, Ohio) to ensure uniform emissivity. After measuring the baseline cases, the enclosures are filled with PCM. The masses of the two PCMs (PureTemp-42 and paraffin from Sigma Aldrich) for each copper enclosure are listed in Table 5.1. The setups for all three experiments were calibrated in the unpowered state - i.e.without any connections to power supply, display and computer with a constant emissivity of 0.9. The emissivity of the coating is determined by comparing against materials with known emissivity (e.g.electrical tape) coated on the same surface and the emissivity values are scaled to match surface temperatures from known and unknown emissivity coatings.

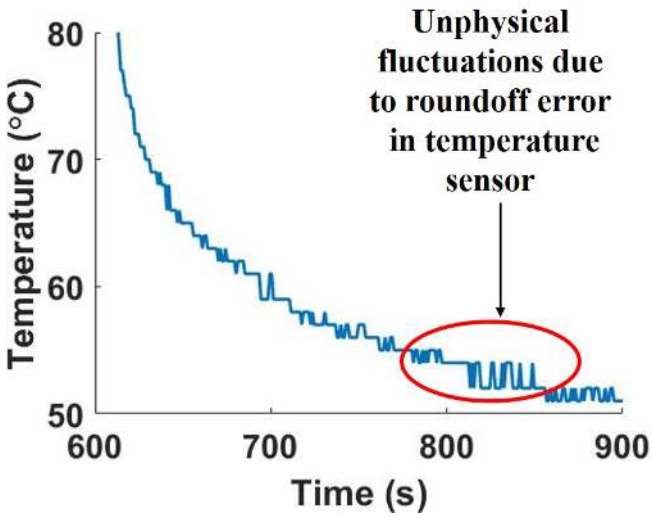


Figure 5.3. Core temperatures after benchmark is completed for copper enclosure of size 10 mm × 10 mm × 5 mm filled with PureTemp - 42 PCM. After 800 s, discrete temperature steps are observed. This unphysical behavior is due to rounding error since the resolution of the core temperature sensor is 1 °C.

Thermal movies are recorded at 200 to 900 frames depending on the duration of the benchmark with a frame delay of 1 s for approximately twice as long as the benchmark to capture the entire heating and cooldown process. The movies are long enough so that the temperature at the end is almost equal to the initial temperature ($\approx 30\,^{\circ}\mathrm{C}$). The temperature logging script starts at about the same time as the movie. There is an approximately 10 s delay in starting the benchmark test. Note that, auxiliary functions (location and internet) are turned off and the display brightness is set to Auto, but there is no display on the SBC itself.

5.2.1 Benchmark

In this work, the LINPACK Benchmark [78] is used to evaluate the performance of the die, each unfilled enclosure attached to die, and each enclosure filled with PCM attached to die. The LINPACK Benchmark was first introduced by Jack Dongarra

Table 5.1.
Mass of PCMs used for *in situ* tests in (g) for three copper enclosures of size 10 mm × 10 mm × 3 mm, 10 mm × 10 mm × 5 mm, 15 mm × 15 mm × 5 mm. The mass is measured using a weighing balance (model Entris, Sartorius Corporation, Bohemia,NY) with a resolution of 0.001 g. Copper enclosures have a wall thickness of 0.3 mm.

Enclosure Dimensions (mm)	10 × 10 × 3	10 × 10 × 5	15 × 15 × 5
PureTemp - 42	0.27	0.3	0.72
Paraffin - Sigma Aldrich	0.274	0.447	0.963
Enclosure only	1.136	1.7111	2.878

in 1978 to estimate the time required by systems to solve a dense system of linear equations of the form $Ax = b$. It uses the LINPACK library which is based on Basic Linear Algebra Subprograms (BLAS) in Fortran to solve a dense system of linear equations. The results of the benchmark represent the systems performance for floating point operations only and not the overall performance. Additionally, the theoretical peak performance (in Mflops/s) is computed by counting the number of full precision floating point addition and subtraction operations completed during the cycle time of the machine. The parallel implementation of this benchmark is used to rank supercomputers in the Top500 list. The runtime of the benchmark is determined from the clock frequencies of the cores as follows

- The start time is the time at which there was transition from a single active core (CPU 0) to multiple cores (not necessarily all four) and this transition sustains for more than 11 s.

- The end time is the time at which there was a transition to only an active core (CPU 0) from multiple cores. Usually,this was characterized by a sharp reduction in frequencies with only CPU core 0 active after this transition.

Square matrices from size 250 to 1000 are solved for three different step sizes - 50, 25 and 15 using the LINPACK benchmark. All 4 cores are used during the tests. However, the core temperatures are below the cutoff temperature(70 °C) for the LINPACK benchmark with a step size of 50. The LINPACK benchmark with step sizes of 25 and 15 are referred as LINPACK 1 and 2 respectively. During a test, the matrix sizes are picked randomly from the set of chosen steps and vary on repetition.

In addition to the LINPACK benchmark, the AnTuTu benchmark was considered. It measures user experience, speed of reading from and writing to Random Access Memory (RAM), and CPU and GPU performance. For AnTuTu benchmark, except for two temperature spikes which coincide with peak CPU core 0 clock frequency, the temperatures are also below the cutoff temperature. Hence, these results are not used for comparison.

5.3 Results

Here, the enclosure size and the choice of PCM are varied to interrogate optimum performance configuration. For latent heat based energy storage systems, the time taken to reach a pre-determined cutoff temperature is used to compare the performance of PCMs (see Chapter 2). This time is referred as the "cutoff time". Figure 5.4 and Figure 5.5 compare the transient core temperature plots for the die, the unfilled enclosure, and the enclosure filled with PureTemp-42 PCM for LINPACK 1 and 2 benchmarks respectively. The temperature oscillations observed until the benchmark is complete are due to rapid variations in clock frequency. After the benchmark is complete, the plateaus in temperature plot are due to roundoff error as explained in the previous section (see Figure 5.3). Attaching an unfilled enclosure increases the cutoff time due to improved heat spreading, increased surface area available for convection , and the added thermal mass of the system with the enclosure. Additionally, filling the PCM delays this cutoff time by as much as 40 s for the LINPACK 1 and 33 s for the LINPACK 2 benchmarks, due to the latent heat of PCM, which absorbs

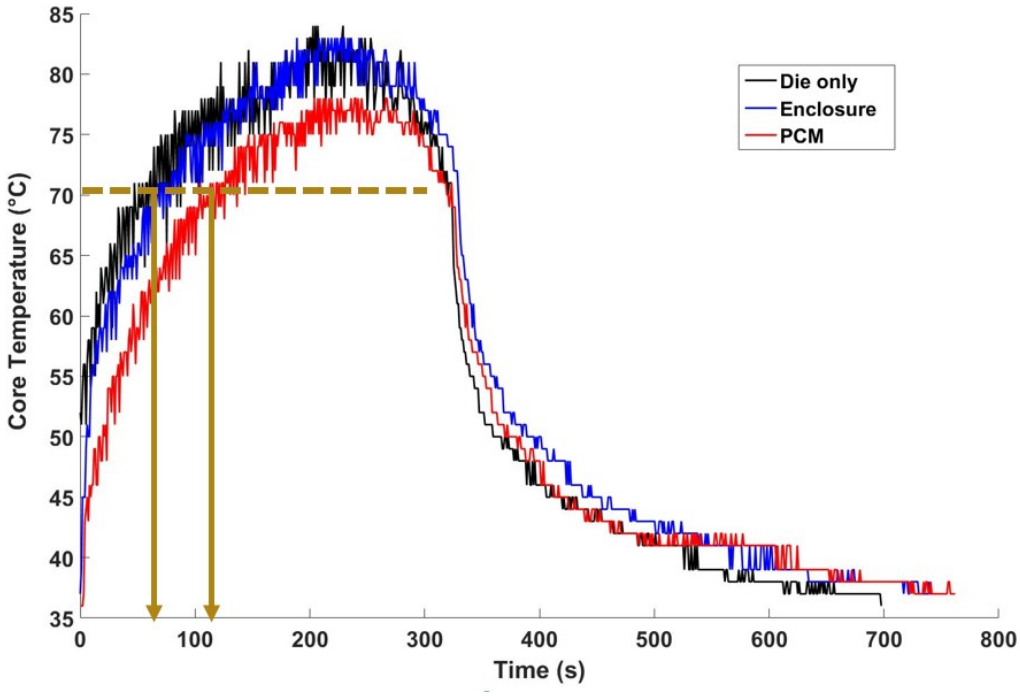


Figure 5.4. Transient temperature plot of the core temperatures from the LINPACK 1 benchmark for 10 mm × 10 mm × 3 mm size copper enclosure filled with PureTemp-42 PCM. The addition of the PCM delays the cutoff time by ≈ 40 s for the LINPACK 1 benchmark relative to the unfilled enclosure.

energy during the nearly phase change process while pinning the temperature to the transition temperature. Note that a plateau in the melting range is not obvious in the data in Figures 5.4 and 5.5 because temperatures presented are the core temperatures, physically separated from the PCM by many layers. However, the shift in the curves with the PCM indicates the effect of melting. Also, the cooling curves (after the benchmark is complete) are similar for all cases. At the end of the experiment, the PCM is fully solidified.

The effect of enclosure dimensions is studied by comparing enclosures of different dimensions. In addition to the 10 mm × 10 mm × 3 mm case shown above, enclosures with (1) an equal base area, but taller (10 mm × 10 mm × 5 mm), and (2) a larger base and height (15 mm × 15 mm × 5 mm) are evaluated. The cutoff times are shown

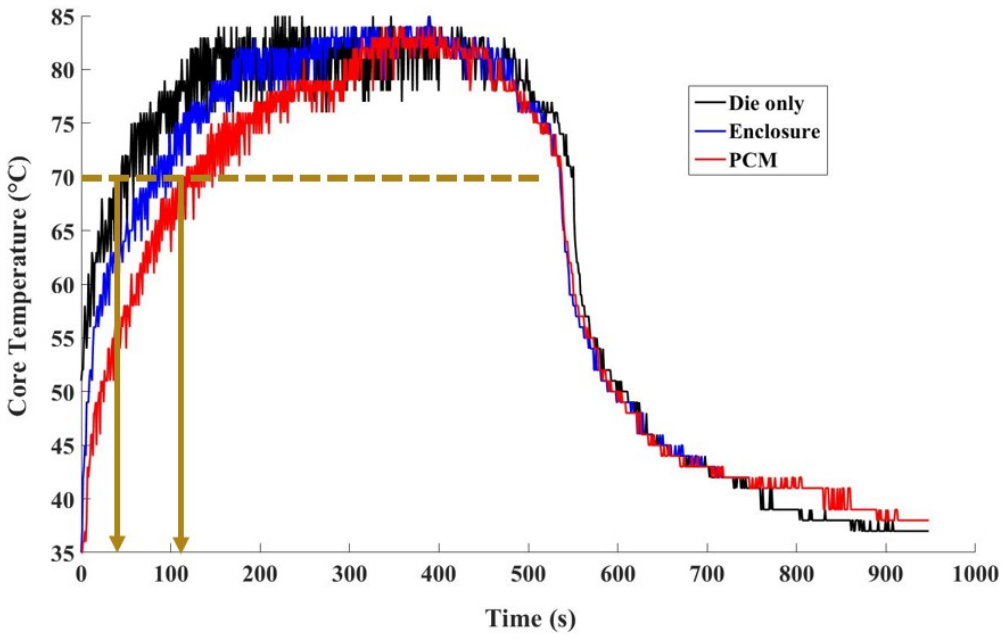


Figure 5.5. Transient temperature plot of the core temperatures from the LINPACK 1 benchmark for 10 mm × 10 mm × 3 mm size copper enclosure filled with PureTemp-42 PCM. The addition of the PCM delays the cutoff time by ≈ 33 s for the LINPACK 2 benchmark relative to the unfilled enclosure.

in Figure 5.6(a) and Figure 5.6(c) for baseline cases and for enclosures filled with PureTemp-42 PCM for both benchmarks. For unfilled enclosures, the time taken to reach the cutoff temperature increases with increased enclosure height (from 3 mm to 5 mm) because of the increased area for convection and the added thermal mass of the enclosure.

The cutoff time is increased for the enclosure filled with PCM compared to the unfilled enclosure for all benchmarks and enclosure sizes because of heat absorption in the transition temperature range due to latent heat of phase change. There is about 11 s decrease in the cutoff time between the enclosures of size 10 mm × 10 mm × 3 mm and 10 mm × 10 mm × 5 mm for the LINPACK 1 benchmark and approximately 28 s decrease for the LINPACK 2 benchmark. Table 5.2 shows the 2D tempera-

ture maps (obtained from IR imaging) of the baseline cases and the enclosure (10 mm × 10 mm × 3 mm) filled with a PCM (PureTemp-42) during the LINPACK 2 benchmark for three times. A maximum temperature difference of 0.5 °C and 8 °C along the horizontal and vertical centerlines respectively, is observed for the die. The spatial temperature gradients from the left bottom vertex for the die only case at $t = 273$ s are observed when the benchmark is running. This is due to the proximity of the heat generating components - CPU cores and GPU (see Figure 7.19). For other times, the temperature maps are uniform to a large extent for the baseline cases. The melt front propagates inward from the enclosure walls as shown by the red arrows and from the bottom to the top of the enclosure also as shown by the transient core temperature plot in Figure 5.5. The melt front propagation inward from the walls is due to high thermal conductivity of the enclosure walls.

Generally, the addition of PCM decreases the maximum temperature observed in the die. However, adding additional PCM (increasing thickness) does not improve this metric. Specifically, the maximum temperature for 10 mm × 10 mm × 5 mm PCM-filled enclosure is higher by 7 °C for the LINPACK 1 and 4 °C for the LINPACK 2 benchmarks relative to the PCM-filled enclosure of size 10 mm × 10 mm × 3 mm. Although the available surface area of the enclosure increases as the enclosure height increases, the increased thickness of the PCM, results in an increase in the thermal resistance between the die and ambient in the vertical direction, resulting in an inferior heat dissipation through the PCM. Hence, the maximum core temperatures are higher than the a shorter enclosure, which also shortens the cutoff time (see Figure 5.6(b) and Figure 5.6(d)).

For a larger base area (height unchanged), the cutoff time increases by as much as 2.6 times for the LINPACK 1 benchmark and 2.48 times for the LINPACK 2 benchmark due to improved heat spreading capabilities. The maximum core temperature (see Figure 5.6(b) and Figure 5.6(d)) for this enclosure filled with PCM is lower by 15 °C for the LINPACK 1 and 9 °C for the LINPACK 2 benchmarks relative to the 10 mm × 10 mm × 5 mm enclosure due to improved heat dissipation around the die.

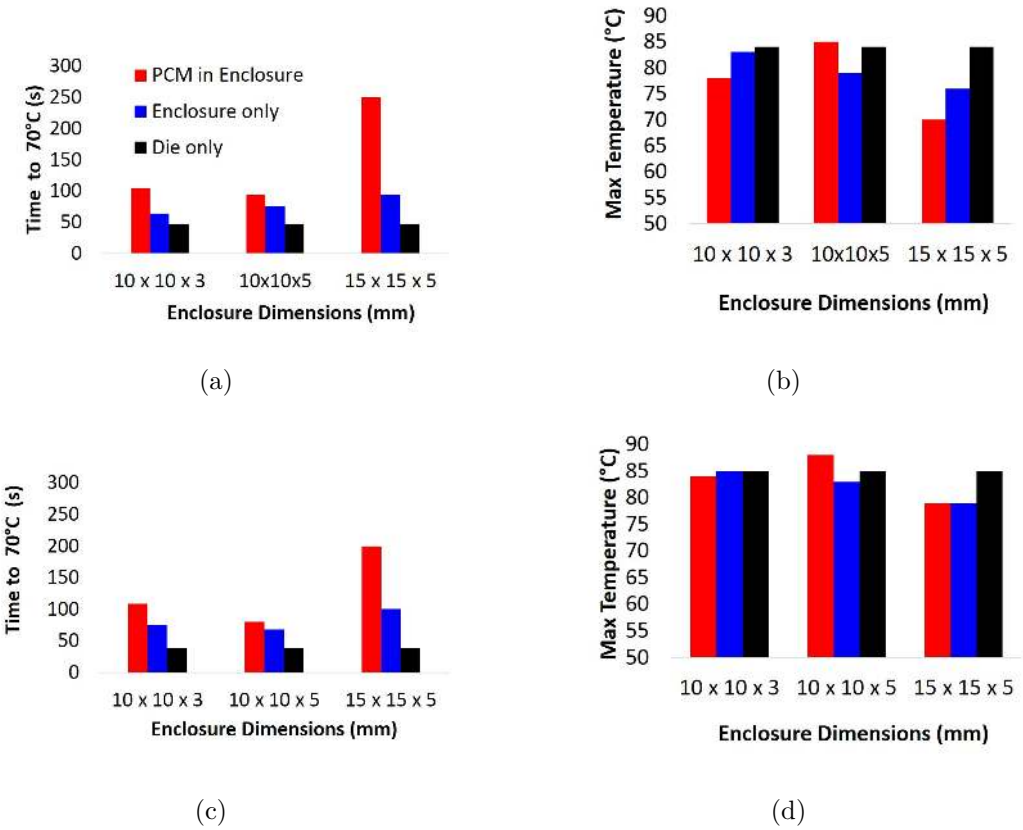


Figure 5.6. Effect of enclosure size on time taken to reach the cutoff temperature of 70 °C ((a) - (c)) and maximum core temperature ((b) - (d)) for the LINPACK benchmarks. (a) - (c) Cutoff times for the LINPACK benchmarks. The addition of PCM (PureTemp-42) increases the cutoff time when a larger base is used due to enhanced heat spreading capabilities. (b) - (d) Maximum core temperature for the LINPACK 1 benchmark. The addition of PCM (PureTemp-42) reduces the core temperatures when the base area is increased due to combined effects of latent heat and greater surface area for heat spreading and natural convection. The maximum core temperature is higher for the second enclosure relative to the first due to high thermal resistance of the PCM leading to heat concentration near the die.

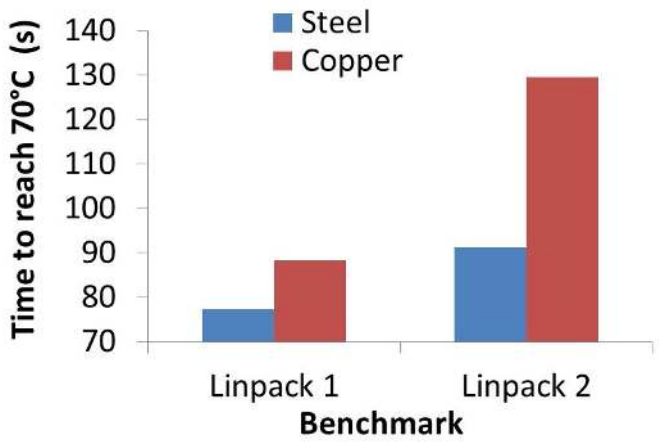
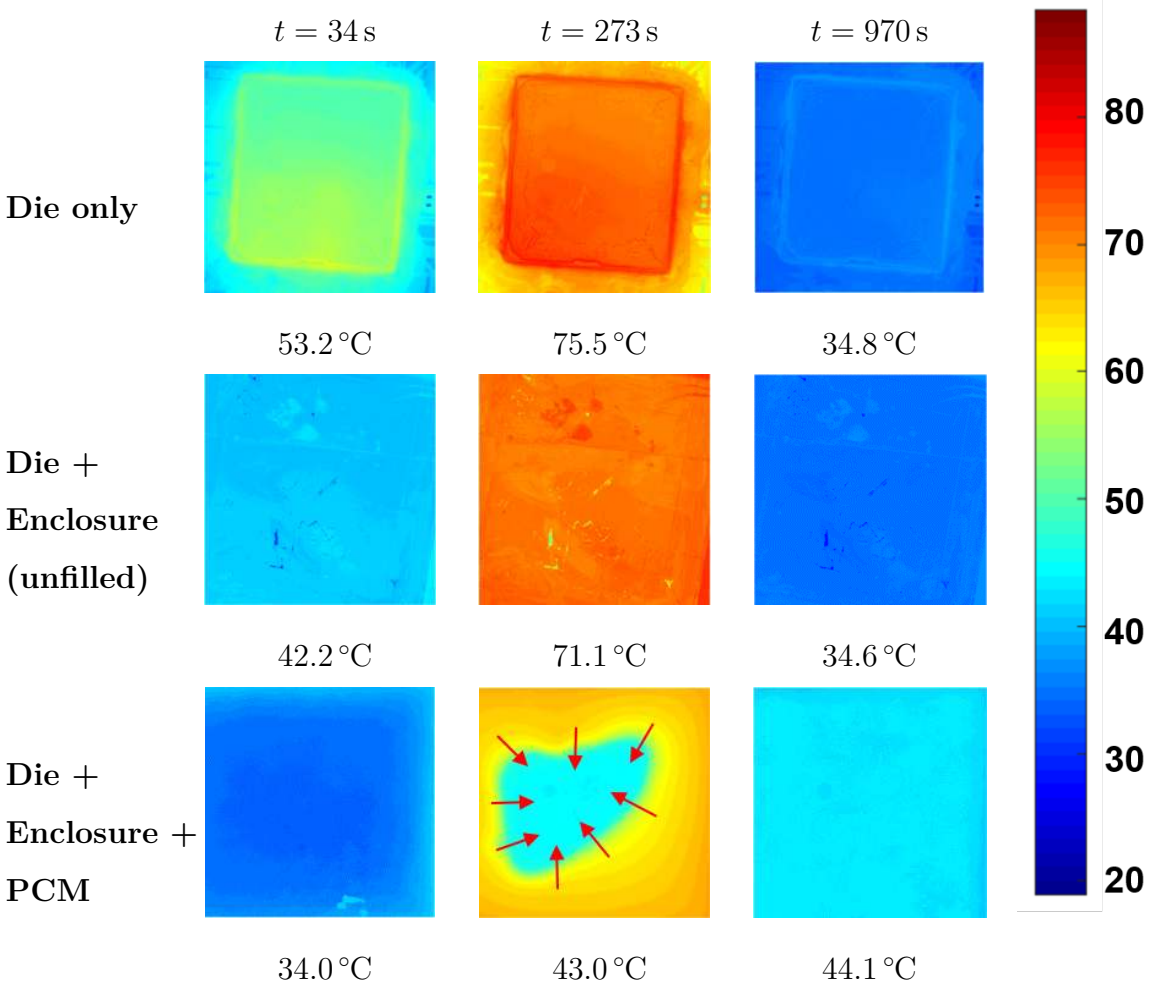


Figure 5.7. Effect of enclosure materials on cutoff time. A 10 mm × 10 mm × 5 mm enclosure filled with paraffin wax (Sigma-Aldrich) is made of copper and steel. Due to higher thermal conductivity of copper, a significant increase (11 s to 39 s) in cutoff time is reported for copper.

To study the effect of enclosure materials, 10 mm × 10 mm × 5 mm enclosures were made from copper or steel (McMaster Carr, Elmhurst, IL) using a paraffin wax PCM (Sigma-Aldrich) (transition temperature range of 58 °C to 62 °C) as the PCM. As expected, due to higher thermal conductivity of copper (8x), the cutoff time increased by about 11 s for the LINPACK 1 benchmark and 38 s for the LINPACK 2 benchmark (see Figure 5.7).

The performance of the PureTemp PCM, consists of paraffin wax like material enhanced with polymer or metallic fillers, is compared against (unenhanced) paraffin with a transition temperature range from 58 °C to 62 °C for the LINPACK 2 benchmark (see Figure 5.8). The cutoff time for paraffin is 2 s lower than the unfilled enclosure due to the higher thermal resistance of paraffin layer, which results in relatively high core temperatures. The paraffin increases the cutoff time by about 13 s for the LINPACK 1 and 32 s for the LINPACK 2 benchmark but the cutoff times are lower than PureTemp-42 PCM due to relatively low thermal conductivity (see Table 7.3) and latent heat of pure paraffin (see Figure 4.2). The difference between the maxi-

Table 5.2.
2D surface temperature maps (in °C) using IR microscope for the die, enclosure (unfilled) attached to die, and enclosure filled with PCM (PureTemp-42) for thee times - before phase change, during phase change and after complete solidification during the LINPACK 2 benchmark. The temperatures below each image represent the maximum surface temperature. The maximum temperature gradients for the die at 273 s, along the horizontal and vertical centerline is 0.5 °C and 8 °C respectively. Hotspots are observed in bottom left corner due to the proximity to the heat generating components (see Figure 7.19). For other times, the baseline cases exhibit spatial uniformity in the temperatures. The melt front propagates inwards from the enclosure walls (shown by red arrows) and from the bottom of the enclosure to the top (see Figure 5.5).



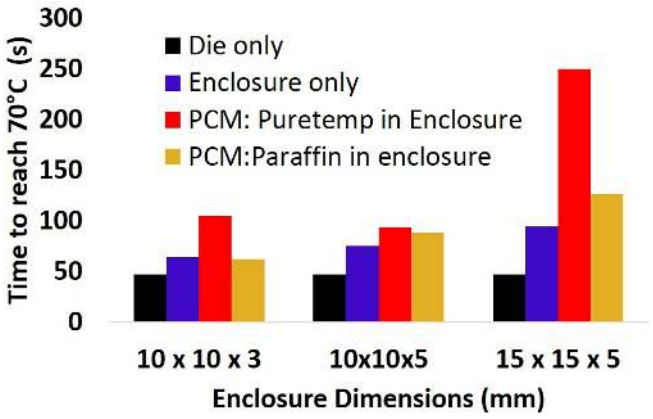
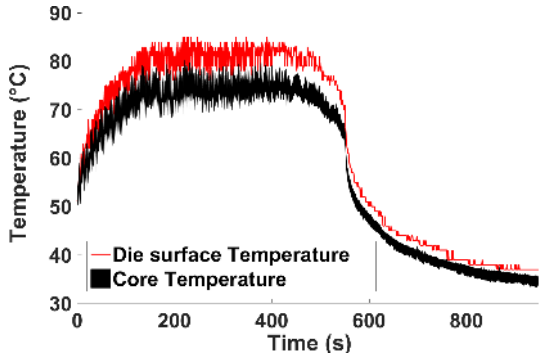


Figure 5.8. Effect of PCMs on cutoff time for three enclosure sizes for the LINPACK 2 benchmark. The copper enclosures have a significantly higher increase in cutoff time than steel enclosures because the thermal conductivity of copper is about 8 times that of steel.

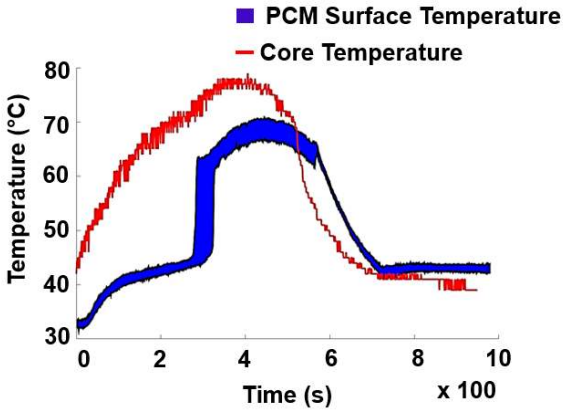
mum and minimum surface temperature of die and PCM from IR imaging is compared with the core temperatures recorded by the custom logging script in Figure 5.9. The upper and lower limits of the black (Figure 5.9(a)) and blue (Figure 5.9(b)) filled regions indicate the maximum and minimum surface temperatures of die and PCM respectively. The die is 0.68 mm thick, hence the surface temperatures are slightly lower but follow the core temperature trend well. The phase change occurs between approximately 150 s to 300 swhich is observed from the change in slope of PCM surface temperature in Figure 5.9(b). This also follows from a change in slope in core temperatures in this interval. The phase change occurs over a range of temperatures (12 °C). This sharp increase in temperature after phase change could be due to a change in emissivity and needs further investigation.

5.4 Conclusions

To summarize , due to the latent heat of phase change, the temperature spikes are stabilized which lead to an increase in the cutoff time. However, local hotspots



(a)



(b)

Figure 5.9. Comparison of surface temperatures of a small region of interest around the center obtained from IR imaging to core temperatures for copper enclosure of size 15 mm × 15 mm × 5 mm for the LINPACK 2 benchmark. The upper and lower limits of black and blue bands represent maximum and minimum surface temperatures of die and PCM respectively. (a) Comparison of the surface temperature of the die and the core temperature. The surface temperatures for the die follow the core temperature variation and are slightly lower due to relatively high thermal conductivity and less thickness of the die.(b) PCM surface temperatures plotted with corresponding core temperatures. The phase change process follows from a change in slope of surface and core temperatures between 150 s to 300 s.

are created because of low thermal conductivity of PCMs for certain enclosure sizes. Enclosures with larger base area increase the cutoff time by as much as 2.48 times for the LINPACK 2 benchmark relative to an enclosure with same height but smaller due to enhanced heat spreading of the enclosure. As a result of improved of heat spreading, the melt front propagates in two directions - from the enclosure walls inward and from bottom to the top of enclosure as shown by the surface temperatures of PCM obtained from IR imaging. The temperature drop during cooldown (time interval between the benchmark and movie end) for the core (see Figures 5.4 -5.5) is steep, which is also reflected in the surface temperatures (see Figure 5.9). The effect of emissivity change during phase change needs to be investigated to explain the rapid increase in surface temperature after phase change (see Figure 5.9(b)). By comparing results between different enclosure sizes, materials, and PCM, an interplay between the thermal conductivity (of the enclosure and PCM) and the latent heat of PCM is clearly evident. This is further explored in Chapter 7 through device and package level computational models.

CHAPTER 6. BRIEF OVERVIEW OF MATHEMATICAL AND NUMERICAL MODELING APPROACHES FOR PCMS

6.1 Introduction

This chapter discusses techniques used to model the temperature evolution during phase change. Early applications [11; 13] of phase change materials for spacecraft thermal management modeled phase change as a quasi-steady state process - assuming that the time required for interface movement is greater than the time taken for the heat to diffuse through the interface. This quasi-steady state thermal model is discussed in the first section (Section 6.2). The next section discusses transient modeling of phase change considering conduction only. These problems, first solved by Stefan [79], are known as *moving boundary problems* and are used to validate the computational models in this thesis (see Section 7.2). The last section of this chapter summarizes models that include convection effects in the liquid portion of the phase change material.

6.2 Quasi Steady State Models

Quasi steady state models enable rapid and approximate estimations of key design criteria such as the amount of phase change material required for a particular heating load and the time required for the phase change material to melt. Although these models do not capture the details of the phase change process, they are useful for initial system design. As an example, Hale *et al.* [13] focused on the use of PCM for spacecraft thermal management and laid out design guidelines based on heat transfer and thermodynamic constraints. Only heat generation and radiation to space were

considered as the energy transfer processes in order to calculate the required radiator area:

$$\epsilon\, A_{rad}\, \sigma\, T_{melt}^4 \Delta\, t_{cycle} = \dot{Q}_{pulse}\, t_{pulse}. \tag{6.1}$$

, where ϵ is the emissivity, A_{rad} is the radiator surface area,T_{melt} is the phase change temperature of the PCM, $\Delta\, t_{cycle}$ is the total cycle time (includes the time during which no power is applied), $\dot{Q}_{pulse}$ is the magnitude of periodic heat dissipation pulse which is applied for a duration of t_{pulse}. They assumed that the time to reach a quasi steady state temperature distribution is shorter than the time required for appreciable interface movement. Mathematically, this assumption translates to $\frac{C_p}{L} << 1$, where C_p and L denote the specific heat capacity and latent heat of the PCM. While the study presented useful design guidelines and considered the impact of different parameters (thermal conductivity, latent heat, and duration of heat pulse), phase change was essentially considered as a steady-state process. Inherently, phase change is a transient process with a moving phase change boundary and significant convection effects in the melt region [80; 81] and more detailed analyses are required for accurate thermal models.

6.3 Moving Boundary Problem

Beyond the quasi-steady state methods, the simplest approach to model phase change involves considering energy balance across the solid-liquid interface and considering conduction as the dominant heat transfer process. The effects of convection can be understood by an energy balance over a control volume taking into account fluid velocities (fluid-flow) which is described in this section. Analyses including the spatial-temporal variation in temperature and phase enable better representation of real systems than the quasi steady state models. These models allow determination of the rate of interface movement, inclusion of temperature-dependent thermal properties, interrogation of different boundary conditions (constant temperature, constant heat flux, etc.), and generally provide more accurate models of the phase change

process. While not representative of the complete device geometry, these 1D analytical solutions provide a method to validate numerical solutions to the phase change problem. Consider a 1-D semi-infinite media ($0 \leq x \leq \infty$) undergoing isothermal phase change with the left edge ($x = 0$) at the phase change temperature (T_m). Here, isothermal refers to melting or solidification occurring at a single phase change temperature, T_m, rather than over a finite temperature range as might be observed for alloys. The derivation of the equations is based on melting, however the same equations hold true for solidification. The application of temperature boundary condition at the left edge results in melt front propagating into the bar ($s(t)$ represents the interface location over time). The goal is to find the temperature spatial and temporal temperature distribution and track the melt front. In this analysis, the volume change due to phase change is neglected and the temperature in the solid phase is assumed to be constant. The domain is subdivided into liquid and solid regions separated by a moving boundary. In the liquid region, the 1D transient heat diffusion equation is given by

$$\rho\, C_p \frac{\partial\, T}{\partial\, t} = k_L \frac{\partial^2\, T}{\partial\, x^2}. \tag{6.2}$$

The boundary and the initial conditions for the different regions are described below.

Liquid region - $0 \leq x \leq s(t)$.

$T(x, 0) = T_m$.

Neumann boundary condition.

$T(0, t) = T_{wall}$.

Solid region - $s(t) \leq x \leq \infty$.

$T(x, t) = T_m$.

The problem is ill-posed since the interface location $s(t)$ is unknown. This is solved by applying an energy balance on a control volume around the interface. Only conduction and phase change is considered and it is assumed that the material properties remain

same after phase change. This interfacial energy balance, given by Equation (6.3) is known as the Stefan condition.

$$\begin{aligned} &\text{Stefan Condition} \\ &-k\frac{\partial T}{\partial x} = L\,\rho\frac{\partial s}{\partial t}. \\ &\text{Interface Temperature} \\ &T(s(t),t) = T_m. \end{aligned} \tag{6.3}$$

With this added constraint, this problem is now well-defined. However, closed form analytical solutions exist only for simple cases. For example, for a the 1D semi-infinite domain with a constant temperature boundary condition, the interface is given as

$$\begin{aligned} &s(t) = 2\,\lambda\sqrt{\alpha_l\,t}. \\ &\text{where,}\lambda\,e^{\lambda^2}\,\mathrm{erf}(\lambda) = \frac{\mathrm{St_l}}{\sqrt{\pi}}. \end{aligned} \tag{6.4}$$

,where $\mathrm{St_l}$ is the Stefan Number of the liquid phase ($\mathrm{St_l} = \frac{C_p\,(T_{wall}-T_m)}{L}$) , α_l is the liquid thermal diffusivity ($\frac{k}{\rho\,C_p}$) , $\lambda = \frac{s(t)}{2\sqrt{\alpha_l\,t}}$ is the similarity parameter introduced to analytically solve the equation set above and $\mathrm{erf}(\lambda) = \frac{2}{\sqrt{\pi}}\int_0^\lambda e^{-t^2}\mathrm{d}t$ denotes the error function. The unknown λ is determined iteratively by root finding algorithms, e.g.Newton-Raphson method. Beyond this solution, transient temperature boundary conditions of the form $f(t) = e^t - 1$ can be applied [82].

6.4 Modeling Convection Effects

After the solid melts, buoyancy effects in the liquid phase can lead to natural convection. These effects may be significant depending on the time and length scales in the system. Benard *et al.* [83] determined experimentally the transition time (t_0) for the boundary layer region to establish in the liquid region for the onset of convection as

$$t_0 = 4.59\left(\frac{\mathrm{Pr}}{\mathrm{St}}\,\frac{\rho_s}{\rho_l}\,Ra^{0.5}\right), \tag{6.5}$$

Table 6.1.
Momentum and Energy conservation equations for both, liquid and solid domains to model phase change.

For the liquid region, Continuity	$\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} = 0.$
x- momentum	$\frac{\partial u}{\partial t} + u\,\frac{\partial u}{\partial x} + v\,\frac{\partial u}{\partial y} = -\frac{1}{\rho}\frac{\partial P}{\partial x} + \mathcal{V}\,\nabla^2\,u.$
y- momentum	$\frac{\partial v}{\partial t} + u\,\frac{\partial v}{\partial x} + v\,\frac{\partial v}{\partial y} = -\frac{1}{\rho}\frac{\partial P}{\partial y} + \underbrace{g\,\beta(T - T_m)}_{\text{Buoyancy effects}} + \mathcal{V}\,\nabla^2\,v.$
For the liquid and solid regions, Energy	$\frac{\partial \rho \mathbf{H}}{\partial t} + \nabla \cdot (\rho\,\mathbf{u}\,H) = \nabla \cdot (k \nabla\,T).$

where Pr is the Prandtl number, St is the Stefan number,Ra is the Raleigh number and the subscripts s,l denoted the densities (ρ) of the solid and liquid phases respectively. The significance of convection can be determined from the geometry, comparing the time-scales of heating and cooling and the transition time (t_0). To model convection, apart from the heat transfer, fluid flow (Navier Stokes) and continuity equations, must also be solved, which increases the problem complexity. The influence of natural convection in the momentum equation is accounted for by considering buoyancy effects. These effects arise due to density differences caused due to temperature gradients. This effect is only considered in the body force ($F = \rho\,g$) term of the momentum equation. The 2D conservation equations for mass, momentum, and energy in Cartesian coordinate systems are given by the set of equations shown in Table 6.1. Here, u and v are the x and y components of the fluid velocity vector $\mathbf{u}$, P is the pressure gradient , ρ is the density, $\mathcal{V}$ is the kinematic viscosity, g is the local gravitational acceleration, β is the coefficient of thermal expansion, $\mathbf{H}$ is the total mixture enthalpy, k is the thermal conductivity and T is the temperature.

The mixture enthalpy, **H**, consists of sensible heating in the solid and liquid phase along with phase change, and is given by [84]:

$$\mathbf{H} = g_s \int_{T_{ref}}^{T} \rho_s \, C_{p,s} \, \mathrm{d}\theta + g_l \int_{T_{ref}}^{T} \rho_l \, C_{p,l} \, \mathrm{d}\theta + \rho_l \, g_l \, L. \tag{6.6}$$

, where C_p is the specific heat, L is the latent heat , g denotes the sold or liquid fraction, T_{ref} refers to the transition temperature and, the subscripts s and l refer to the solid and liquid phases, respectively.

6.5 Numerical Solution Methods

6.5.1 Overview

Two class of methods are widely used to solve the resulting system of equations - moving grid and fixed grid. (1) Fixed grid methods rely on characterizing phase change through melt fractions (*ie.* the fraction of the PCM melted). Since the effect of phase change is modeled using the source terms in the energy equation, the *Stefan Condition* (see Equation (6.3)) derived in the previous section, need not be satisfied explicitly. Since the interface effects are "smeared" over a mesh element, the need to know the location of the interface becomes redundant [84; 85]. (2) Moving grid or front tracking methods track the melt front to determine temperature profile. The solid-liquid interface is fixed in time and space by using a curvilinear coordinate transformation. The advantage of moving grid method is that there is no loss of accuracy due to discretization. However, the governing equations are more complex and hence this process is computationally expensive. Jaluria *et al.* [86] compared these methods over a wide variety of test cases. Apart from the computational time and memory requirements, rate of interface movements, heat transfer rates, and nature of convection were also compared. They found that the moving grid methods more accurately predicted fluid-flow patterns and interface location, but the fixed grid methods were twice as fast for all the test cases. They recommend moving grid methods for isothermal phase change problems and fixed grid methods for alloys or plastics where phase

change occurs over a range of temperatures (*transition temperature range*). For the computational model development in this thesis, fixed grid methods have been used since they are faster and the PCMs has a finite transition temperature range For conduction only phase change with constant thermophysical properties, the energy equation reduces to

$$\rho \frac{\partial \mathbf{H}}{\partial t} = \nabla \cdot (k \nabla T). \tag{6.7}$$

$$\mathbf{H} = C_p T + g_l L. \tag{6.8}$$

For simplicity, the subsequent derivations for fixed grid methods are done for conduction only phase change with constant thermophysical properties.

6.5.2 Apparent Heat Capacity Method

With the apparent heat capacity method, the effect of phase change via latent heat is modeled by artificially increasing the specific heat capacity C_{app} over a finite temperature range to reflect the energy required to change phase at the transition temperature. Numerically this is represented in the temperature-dependent heat capacity by a Dirac function, as shown in Figure 6.1. Thus, the apparent specific heat is defined as [88]

$$C_{app} = \frac{\partial \mathbf{H}}{\partial t} = C_p(T) + \rho L \, \delta(T - T_m). \tag{6.9}$$

where δ denotes the Dirac function $C_{app} = \begin{cases} \rho_s C_{p,s}, & \text{if } T \leq T_m. \\ \rho_l C_{p,l}, & T \geq T_m. \end{cases}$

Substituting C_{app} in Equation (6.7) to get

$$C_{app} \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T). \tag{6.10}$$

6.5.3 Source Term Based Methods

In the source term based methods, the effect of phase change is lumped into a "fictitious" heat source. Unlike apparent heat capacity methods, there is no need for

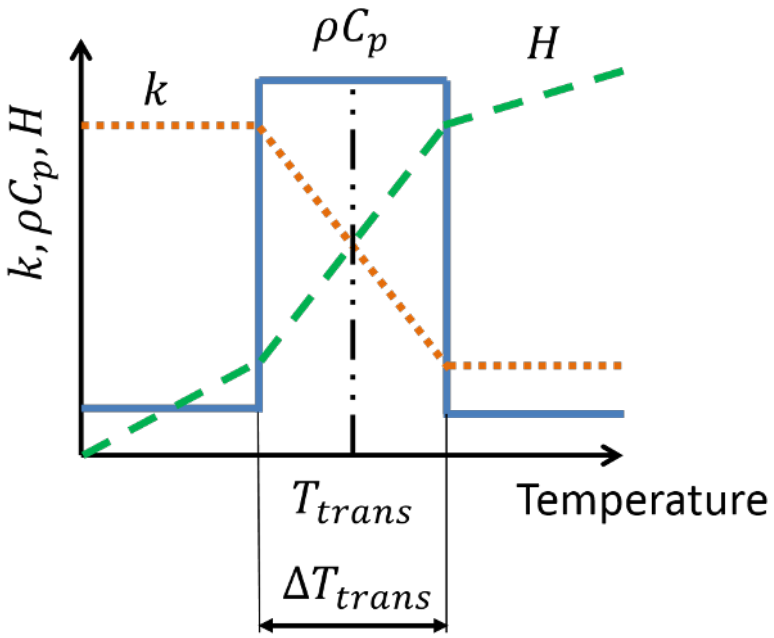


Figure 6.1. Apparent heat capacity method. The effect of phase change is modeled by artificially increasing the volumetric heat capacity ($\rho\, C_{\mathrm{p}}$, shown by solid line) over a temperature range known as the transition temperature range ($\Delta\, T_{\mathrm{trans}}$). For isothermal phase change also, a transition temperature range is required which introduces an error. The total enthalpy (H, shown by dashed green line), which comprises of sensible heat capacity and latent heat, increases with temperature. Typically, for conventional PCMs, the thermal conductivity (shown by dotted orange line) of the liquid phase is lesser than that of the solid phase (Adapted from [87]).

introducing artificial transition temperature ranges. Substituting Equation (6.8) into Equation (6.7) yields

$$\rho\, C\, \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla\, T) - \rho\, L\, \frac{\partial g_l}{\partial t} \tag{6.11}$$

, where g_l the liquid fraction and is an unknown. Several possible relations have been proposed for updating g_l. Generally, the updating scheme includes an overshoot / undershoot factor to ensure that liquid fraction is bounded between 0 and 1 [89–91].

6.6 Conclusions

We reviewed analytical and numerical approaches for modeling phase change. Early analytical models for the design of radiators considered phase change as a quasi steady state process and assumed that the time taken for interface movement was much longer than the time taken to reach a linear quasi steady-state. Another approach considered the transient nature of the phase change process and tracking the interface position and the temperature distribution. These set of problems are known as the moving boundary problems and under simplifying assumptions (e.g.constant thermophysical properties in solid and liquid phases , no density change) , can be solved analytically. Due to the complexity of the problem and the simplifying limitations of analytical methods, numerical methods were discussed which discretize the governing equations to a system of equations which are solved via matrix methods. In the apparent heat capacity method (used in this work), the effect of phase change was reflected in specific heat capacity by considering phase change as a sharp increase in specific heat over a finite range of temperature. Another approach involved considering energy absorption or release during phase change and modeling this as a source term in the governing differential equations. The apparent heat capacity method led to erroneous temperature spikes when modeling isothermal phase change and increasing the temperature range also modeled the physics inaccurately. Although these issues were offset by the source term method, under-relaxation parameters are needed to ensure convergence which typically rely on user's judgment [84]. However, both methods do not track the melt front explicitly. The melt front is calculated from the change in temperature which is used to determine if a cell or a control volume is undergoes phase change. Front tracking methods involve solve for phases separately and are matched along the phase change interface for consistency.

CHAPTER 7. THERMAL DEVICE SIMULATIONS

7.1 Introduction

This chapter describes the computational model used for the device and *in situ* level simulations. Comsol [92], a commercial FEA software, is used for modeling. The first section of this chapter validates the numerical model using the apparent heat capacity method (Section 6.5.2) against standard benchmark solutions. Then the model is extended to realistic mobile device geometries for evaluation of the PCM integration schemes (see Section 7.3.2). Package level models are presented in Section 7.4 to study the effect of PCM placed on the chip and to validate the results from *in situ* tests (Section 5.3).

7.2 Stefan Problem Validation

The theory, initial conditions, and boundary conditions for the Stefan problem are discussed in Section 6.3 of Chapter 6. A Dirichlet boundary condition, or constant temperature, boundary condition e is applied as $T(x = 0, t > 0) = T_w$. For the validation case, $T_w = 350\,\mathrm{K}$ and the initial temperature is $T_{\text{initial}} = T(x, t = 0) = 313\,\mathrm{K}$. The transition temperature of the test PCM (paraffin) is $314.5\,\mathrm{K}$ with an assumed transition temperature range of $3\,\mathrm{K}$ (hence, the transition temperature varies from $313\,\mathrm{K}$ to $316\,\mathrm{K}$). The thermophysical properties of the PCM are shown in Table 7.1 The analytical solution for this setup is given by Equation (6.4). A 2D rectangular domain with a length 4 times longer than the width is used to model the 1D semi-infinite geometry as shown in Figure 7.1. Adiabatic boundary conditions are applied to the top and bottom edges. A free time stepping scheme with an initial step size of $0.001\,\mathrm{s}$ and maximum step size of $0.5\,\mathrm{s}$ was used with 10×10 rectangular mesh elements. To evaluate the accuracy of the COMSOL model, temperature and interface

Table 7.1.
Thermophysical properties of Paraffin wax used for validation of the Comsol phase change module [93]. Phase change is modeled with the apparent heat capacity method.

Property	Value
Thermal conductivity, k	$0.2\,\mathrm{W/(m\,K)}$
Latent heat, L	$175 \times 10^3\,\mathrm{J/kg}$
Specific heat, C_p	$2400\,\mathrm{J/(kg\,K)}$
Density, ρ	$750\,\mathrm{kg/m^3}$
Transition temperature , T_m	$314.5\,\mathrm{K}$
Transition temperature range , ΔT	$3\,\mathrm{K}$

locations evaluated at several times (0.8 h, 3 h, 6 h, 10 h and 16 h) are compared to the analytical solution (see Figure 7.2). The numerical results under predict the interface location due to the presence of a mushy region to distinguish solid and liquid phases with a root mean square error of 2.77×10^{-3}. Note that the temperature in solid region (large x values) is nearly constant and equal to the initial temperature at all times. This confirms that the given 2D domain size is long enough to approximate the 1D semi-infinite domain in the Stefan Problem. Note that at short times, a slight unphyscial dip in the temperature, below the initial condition, is observed in the COMSOL results. This may be due to numerical error of the algorithm. At long times, the COMSOL simulation matches well with the Stefan solution. A grid independence study is carried out to study the effect of the numerical discretization (see Figure 7.3). For the initial increase in grid elements from 15×15 to 25×25, there is a noticeable improvement in the solution accuracy as the numerical result fits the analytical solution more closely. Further grid refinement does not lead to a significant improvement in the solution accuracy. All solutions match well with the analytical solutions except very close to the interface between the liquid and the

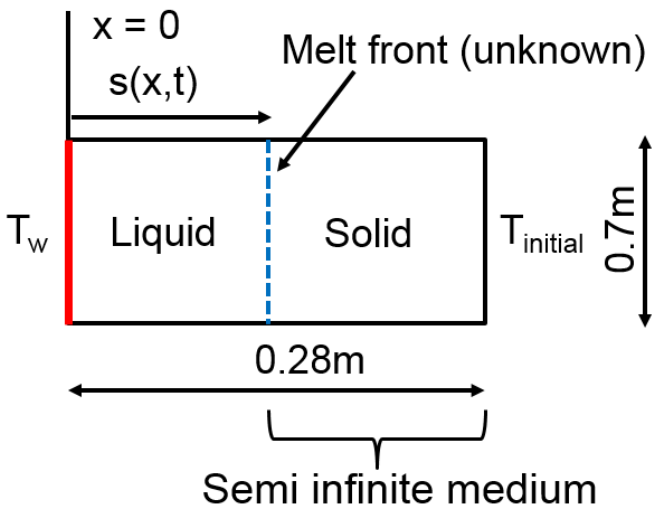


Figure 7.1. Setup of the Stefan problem. The system is modeled as a 2D rectangular domain with the length significantly larger than the width. Thus, the setup can be considered as a 1D semi-infinite geometry analytically since the temperatures in the solid region remain unchanged spatially for a given time. Constant temperature (Dirichlet) boundary conditions are applied on the left and right edges and the top and the bottom walls are insulated. The melt front and temperature distribution are unknown and solved using apparent heat capacity method in Comsol.

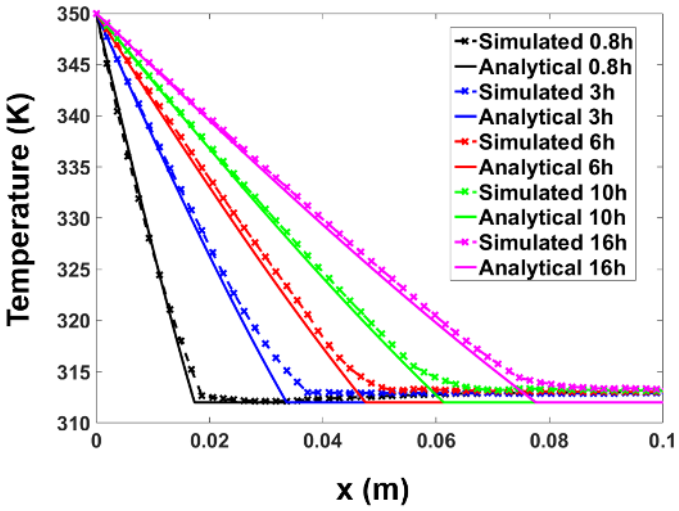
solid. Here, the approximation in the analytical solution is evident in the abruptly 0 temperature gradient in the solid portion of the domain.

7.3 Device Level Simulations

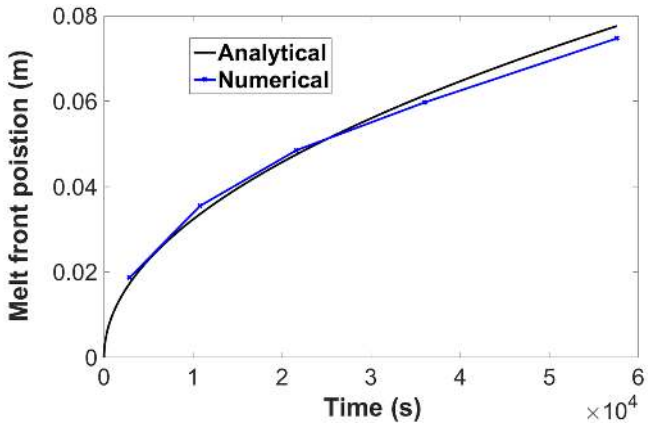
7.3.1 Overview of Mobile Package Model

After confirming the accuracy of the apparent heat capacity model in COMSOL, a numerical model is built to evaluate thermal performance of PCMs integrated into realistic mobile devices. The goals of the computational are to

1. Study heat dissipation paths in a smartphone with and without PCMs



(a)



(b)

Figure 7.2. Comparison of analytical and numeric solutions for 1D phase change problem modeled using a 2D rectangular domain in Comsol. The apparent heat capacity method is used to model phase change. (a) Temperature profile along the horizontal centerline for different times. The temperatures in the solid region are nearly constant for all times and equal to the initial temperature, which shows that the modeled geometry is large enough to be considered as semi-infinite body. (b) Interface location with time. Since phase change occurs over the transition temperature range, the melt front is computed by identifying the regions whose temperature is greater or lesser than the transition temperature (which is the mean of the maximum and minimum transition temperatures).

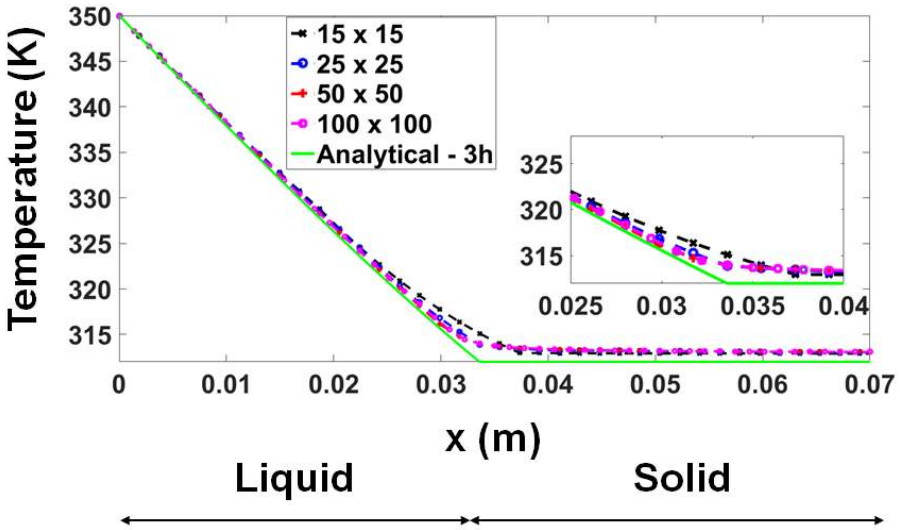


Figure 7.3. Impact of the grid refinement on the temperature profile in the liquid region of the phase change material at t = 3 hours. As grid size is increased from 50×50 to 100×100, no significant change is observed. The constant temperatures in the solid region implies that the geometry can be reduced to a 1D semi-infinite domain to obtain analytical solutions.

2. Compare effect of PCMs on time taken to reach allowable maximum temperatures

3. Determine key material properties and optimize the design

Typically, in a mobile device, convection and radiation from the outer case to the ambient are the primary modes of heat transfer. Thermal constraints include the safe operating temperature of the die (70 °C to 110 °C) [34] and the maximum safe-to-touch case or surface temperature (40 °C) [3]. A key challenge involves dissipating heat away from the heat source to the ambient without going beyond the permissible case temperature limits. Thus, in this work, processor and surface temperatures are chosen as metrics and the performance of alternative cooling solutions is evaluated by comparing the time taken to reach these temperatures. Inside a mobile device,

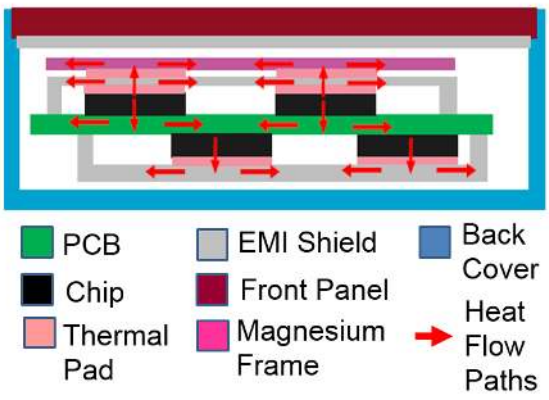


Figure 7.4. Approximate conduction heat flow paths in Samsung Galaxy S3 (adapted from [94]). Inside the mobile device, conduction is the dominant mode of heat transfer due to limited aspect ratio and gap thicknesses which limit the influence of natural convection and the relatively low temperatures minimize the impact of radiation.

conduction is the dominant mode of heat transfer. Approximate conduction heat flow paths are shown in Figure 7.4.

Although modern mobile phones vary widely in construction, there are some common structural elements that facilitate the development of a generic thermal model *et al.* [95] including the Printed Circuit Board (PCB) with components, middle plate, back plate, battery, and display, as shown in Figure 7.5. The processor is mounted on the PCB. The typical internal structure of the processor comprises of the silicon die mounted on a FR-4 substrate, interconnects and encapsulation. An Electro-Magnetic Interference EMI shield (usually, aluminum) surrounds the processor to prevent interference with electromagnetic waves. The middle plate (also known as the stiffener) provides structural integrity and has high heat spreading capabilities. Furthermore, there are thermal pads or TIMs at some interfaces and high conductivity sheets (made from graphite) around the battery in some devices. The geometrical complexity at the device and the package level (example, modeling interconnects) combined with unknown thermophysical properties of the constituent materials make it challenging

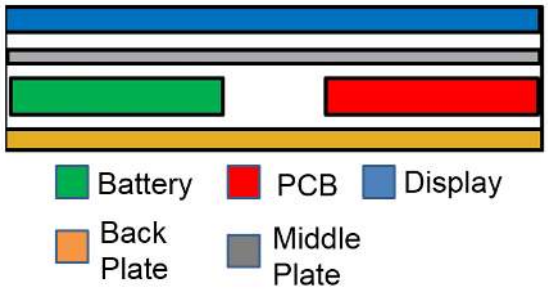
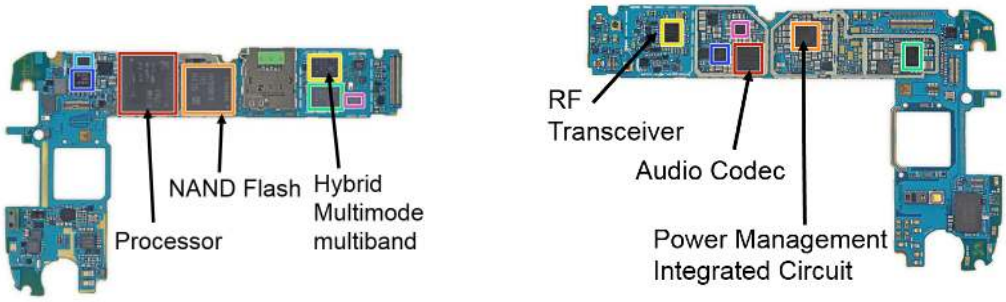


Figure 7.5. Cross sectional schematic of a representative mobile device package with a touch-screen. The chip or the package is the major heat source, along with battery and display. The middle plate serves the dual purpose of providing structural rigidity and spreading heat. For system level models, in this work, the processor is treated as the only heat source.

to create a complete model of the device. Thus, it is common to model the processor as a uniform heat source, rather than to include the details of the internal structure of the package. Hence, initially, the processor was modeled as a uniform *volumetric heat source*. Subsequent refinements modeled the processor in more detail - with the the underfill, epoxy, and interconnect structure. Results of the refined package level models are presented in the next section (Section 7.4).

Here, the model cell phone geometry is based off from publicly available tear-downs [96] and schematic of old models [94]. The *volumetric* heat sources are approximately identified according to their relative sizes and function from the layout of the components of the PCB as shown in Figure 7.6. In this work, perfect interfaces are assumed by neglecting thermal boundary resistances. Hence the model *under-predicts* the temperatures. Based on the available information [94; 96], the system is modeled with four volumetric heat sources on either side of the PCB. Three of the four heat sources on each side represent real components: the processor, NAND flash, and hybrid multimode multiband on the top side and RF transceiver, audio codec, and power management integrated circuit on the bottom side (see Figure 7.6). Heat generation from all other components on each side are lumped together into the

fourth heat source. Boundary conditions at all external surfaces are modeled as a combination of natural convection($h = 5\,\mathrm{W/(m^2\,K)}$) and radiation with $\epsilon = 0.9$ from both to ambient ($T_{amb} = T_{initial} = 20\,^{\circ}\mathrm{C}$). Internal radiation and convection were previously found to be insignificant and are neglected in the present work. In this model, the components on PCB are considered as the only heat sources. The cross



(a) Top PCB (b) Bottom PCB

Figure 7.6. Components at the top (a) and bottom (b) of PCB modeled as heat sources. Heat generation from all other components is lumped into a fourth heat source (Figure reproduced with permission from [96]).

section of the mobile device geometry is shown in Figure 7.7. Mobile phones are ultra compact and there are minimal locations for integrating the PCM without moving components or expanding the device size. In this work, we evaluate integrating PCMs into the existing air gaps near the die (enclosed by *red rectangles* in Figure 7.7). We expect this location to be ideal for improving thermal performance since the PCMs have a higher conductivity than air and no additional cavities or special arrangements need to be made thus keeping the thickness of the device unchanged.

7.3.2 Steady State Device Level Simulations

To validate the model, initially steady state performance is evaluated (without any PCM). A total power of 10 W is applied and distributed such that the heat

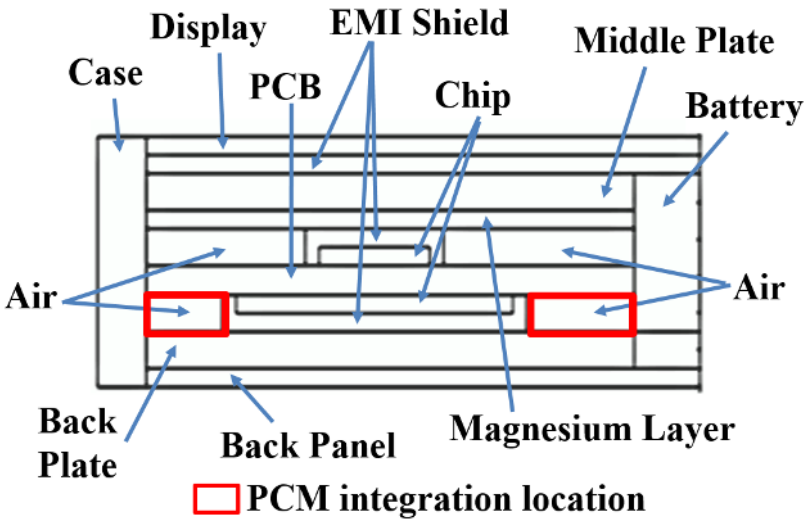


Figure 7.7. Mobile device cross section in X-Y plane at Z = 40 mm . Overall phone dimensions: 6.8 mm × 70.5 mm × 143.4 mm . The phone volume is $V_{phone} \approx 68.77\,\text{cm}^3$ and the combined volume of air pockets $V_{air} \approx 9\,\text{cm}^3$. However, the PCM is placed in the air pockets (enclosed by red rectangles) adjacent to the processor and $V_{pcm} \approx 4.1\,\text{cm}^3$.

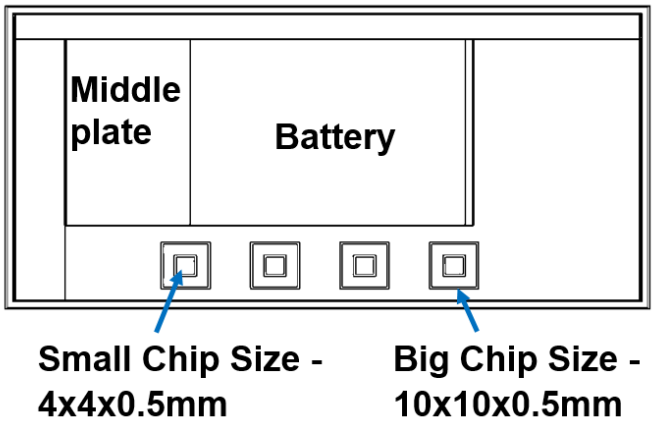


Figure 7.8. Top view (XY-plane) of the device level model with the display *hidden* to show the internal components. For steady state simulations, a constant total power of 10 W is applied. The chips are modeled as volumetric heat sources.

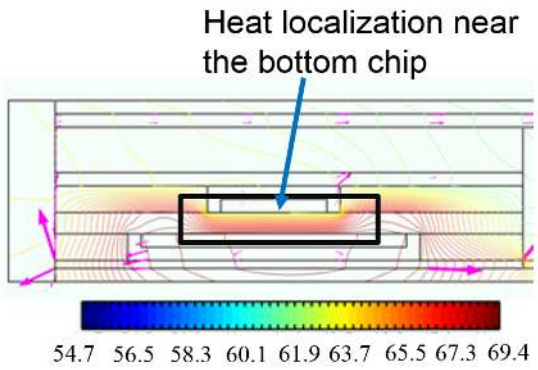


Figure 7.9. Isothermal contours for the steady state model for a cross-section in the X-Y plane at Z = 40 mm with a total power dissipation of 10 W. Heat localization near the bottom processor is due to poor thermal conductivity of surrounding components. The temperature gradients around top processor are less localized because of high heat spreading capabilities of magnesium plate which is in contact the top processor.

flux of all components are equal, which resulted in 2.2 W power applied to bottom heat sources and 0.34 W applied on the top. A Normal Physics-controlled mesh was generated in Comsol with 93 518 domain elements. Default solver - Iterative (Multigrid) with a relative tolerance of 1×10^{-3} and an absolute tolerance of 1×10^{-5} was used. Figure 7.7 and Figure 7.8 show the side (X-Y plane at Z = 40 mm from the bottom of the phone) and top (X-Z plane) views of the mobile phone, respectively. Some components (like the display) are hidden to view the internal components. For the steady state models, the area enclosed by the red rectangles in Figure 7.7 are air gaps, whereas for the transient models they are filled with PCM. The cross section of the side view (see Figure 7.7) is taken at Z = 40 mm from the bottom of the phone since it cut through most components. At a different positions along the height of the phone, the layout differed. Hence, the model cannot be considered as *extruded* from the side view cross section, but rather the geometry is truly three dimensional. The material properties for the steady state case are listed in Table 7.2.

Table 7.2.
Properties of components used for the steady state model. Maximum thickness values are shown in this table.

Domain	Material	Thermal conductivity (W/(m K))	Thickness(mm)
Display	Glass	1.4	0.5
EMI	Aluminum	238	0.5
Magnesium Layer	Magnesium	96	0.5
Processor	Silicon	130	0.5
Battery	Lithium-Ion	15	5
Middle Plate	Alumina	15	5
Case	Aluminum 6013	150	1.76
Back Plate	Aluminum 6013	150	0.3
Air	Air	0.024	1
PCB	FR4	0.3	0.8
Back Panel	Glass	1.4	0.5

Figure 7.9 shows the isothermal contours for a representative cross section (in XY plane at Z = 40 mm). The maximum temperature is $\approx 69.5\,^{\circ}\mathrm{C}$. The isotherms are closely spaced near the bottom processor since it dissipates a greater power relative to the top processor. This is in sharp contrast to relatively low temperatures around the top processor since its in thermal contact with high conductivity components like magnesium plate. Also, from the length of the heat flux vectors (superimposed as pink arrows on the isotherms), a significant fraction of heat is dissipated vertically, both up (from top processor →EMI shield →Magnesium plate→ambient) and down (from bottom processor →back plate →ambient). Furthermore, the heat flux vectors indicate the significant influence of lateral heat spreading, which is difficult to account

for using Resistor-Capacitor based thermal models [97–99]. Also, materials used in mobile devices often have anisotropic material properties (for example, a graphite sheet placed around the battery in Apple iPhone 5), which is challenging to account for using Resistor - Capacitor models.

7.3.3 Transient Device Level Simulations

The PCM is integrated in the air pockets (enclosed by red rectangles in Figure 7.7) with an approximate volume of 4.1 cm^3. The transient simulations are evaluated over 2000s with approximately 2 s time steps with the same geometry as in the steady state simulations. The free time-stepping (default) scheme adapts the time step size based on the error residuals (or convergence behavior) of the previous iteration and thus the time steps do not correspond to the initial user input time intervals. An absolute tolerance of 1×10^{-5} and relative tolerance of 1×10^{-3} are specified. The iterative, fully-coupled solvers are selected to evaluate the transient simulations. A total constant power of 10 W is applied to the 8 chips. The time taken for the processor to reach 80 °C and case to reach 40 °C are chosen as the key metrics to evaluate the impact of adding commercial PCMs (properties in Table 7.3). Placing a PCM improves the cutoff time for both, the processor and the surface when compared to the no PCM (only air) case. Metallic solder (Bi-In-Pb-Sn) and All Cell PCMs whose thermal conductivities are greater than wax based PCMs by as much as 40 exhibit the greatest increase in cutoff time compared to no PCM (only air) as shown in Figure 7.10. This indicates the importance of high thermal conductivity of PCMs.

Typical mobile devices are used intermittently: roughly 8 s of use, followed by 15 s period of inactivity. Furthermore, given the recent popularity of computational sprinting (discussed in Section 2.3.2) , we studied the temperature profiles for a pulsed power case with a peak power of 15 W. This pulse is applied to only 1 processor - the larger of the second chip from the left as indicated in Figure 7.8 starting at 60 s and applied for 1 s (see Figure 7.11). Similar to the transient constant power sim-

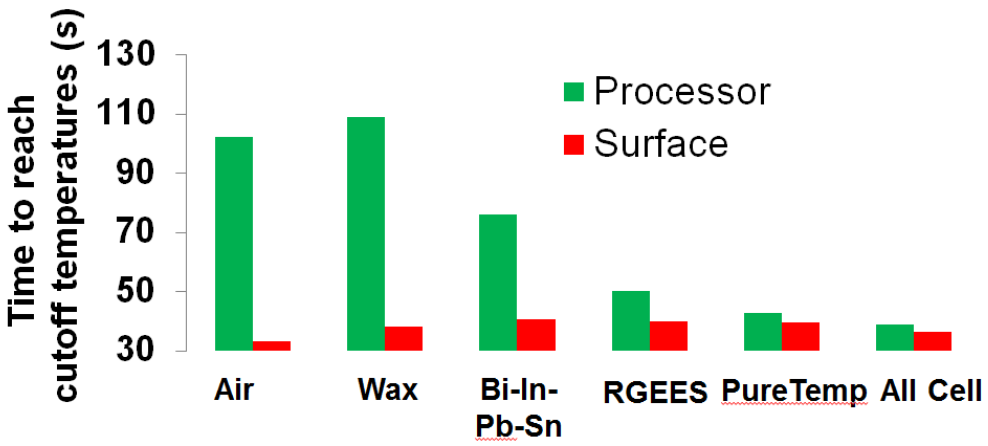


Figure 7.10. Time taken (shown in **boldface above bars**) for the processor to reach 80 °C (shown in green) and the case to reach 40 °C (shown in red) in s for no PCM (air pockets) and PCMs integrated in air gaps .

ulation, the time taken for the processor and the surface to reach their respective cutoff temperatures gave preliminary insights on the effect of the PCM. These cutoff temperatures were exceeded when wax is used. It was expected that improving the thermal conductivity of the PCM (e.g.wax integrated with a thermally conductive filler material) would improve the effectiveness of PCM over single and multiple power cycles. The maximum temperature of the chip and the surface are below the prescribed limits (80 °C for processor and 40 °C for surface) for $k_{wax} \geq 1\,\mathrm{W\,m^{-1}\,K^{-1}}$, as shown in Figure 7.12. Hence, $k_{wax} = 1\,\mathrm{W\,m^{-1}\,K^{-1}}$ was used for the subsequent set of simulations.

To isolate the impact of the latent heat of phase change, the effect of the PCM for one power cycle (see Figure 7.11) is compared against a material with identical properties but *without phase change*. The maximum surface temperature of the paraffin undergoing phase change is 5 °C lower than an identical material with no phase change (see Figure 7.13(a)). After about 60 sec after the end of power spike, the surface temperature stabilizes at about 32 °C. A successive power spike applied

Table 7.3.

Material properties of PCM's used in transient constant power transient simulation. Also, the mass of the PCM and the % of PCM relative to the device mass is tabulated. Subscripts s and l in parenthesis denote the solid and liquid state properties where available. All other properties, unless indicated are for solid phase. Properties of wax (obtained from Ross Brothers Inc) were taken from Kandasamy *et al.* [73] and other PCMs were taken from the respective manufacturer datasheets (Indium [74],RGEES [100],PureTemp [75] and AllCell [76]). As expected, metallic PCM has the highest conductivity but weighs $\approx$ 10 times more than organic PCMs. The transition temperature range of all PCMs except metallic solder is determined from Differential Scanning Calorimetry (DSC) (see Chapter 4).

Material	% of Current Phone Mass	Mass (g)	Transition Temperature (°C)	Transition Temperature Range (°C)	Thermal conductivity (W/(m K))	Latent Heat (J/kg)	Specific Heat (J/(kg K))	Density (kg/m^3)
Wax	1.19	3.28	51	20	0.21 (s) 0.12 (l)	173.4×10^3	2890	900(s) 750 (l)
Bi-In-Pb-Sn	11.9	36.98	58	5	10	28.9×10^3	167 (s) 201 (l)	9010
RGEES	1.24	3.45	55	12	0.25	210×10^3	730	840
PureTemp	1.42	3.94	68	10	0.25 (s) 0.15 (l)	213×10^3	1850 (s) 1910 (l)	960 (s) 870 (l)
Allcell	1.29	3.59	55	3.8 or 13	10 (in-plane) 6 (cross-plane)	165×10^3	1960 (s) 2200 (l)	875

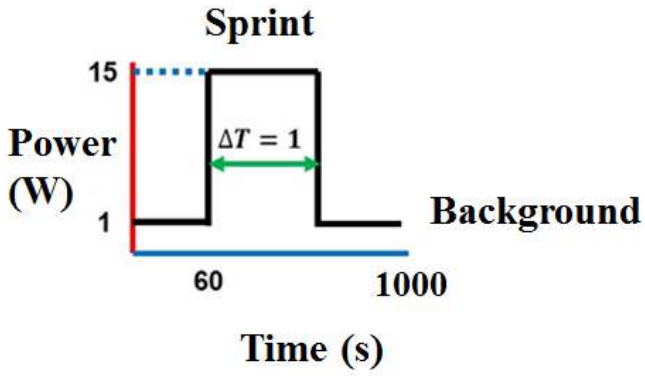


Figure 7.11. Sprinting power profile. 15 W is applied from 60 s to 61 s and a background power of 1 W is applied all other times .

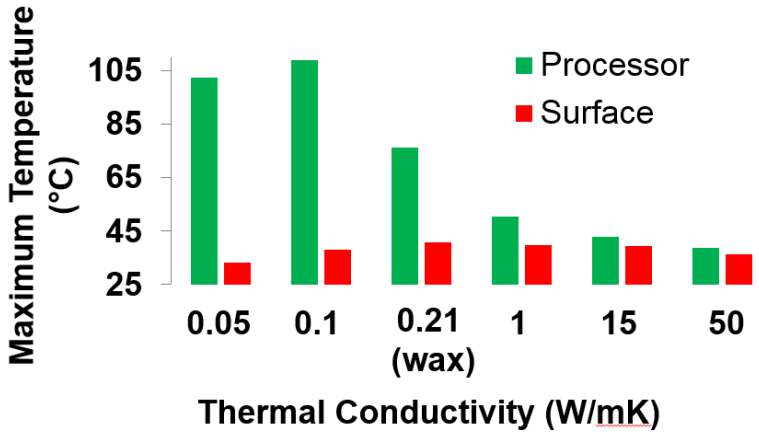
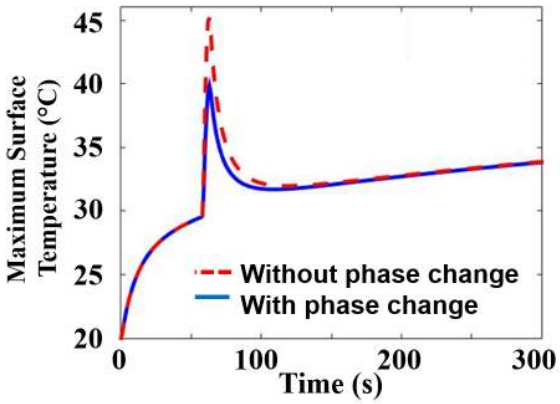
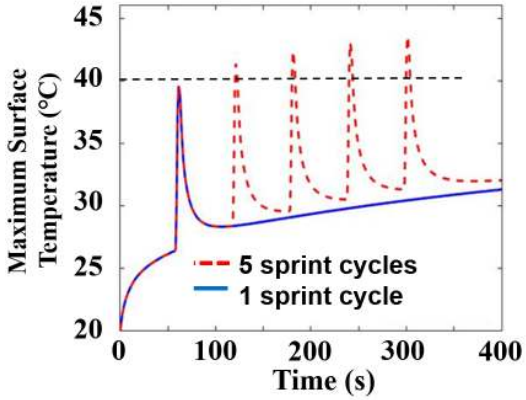


Figure 7.12. Maximum temperatures of processor (shown in green) and case (shown in red) for different conductivities of wax ($\mathrm{W\,m^{-1}\,K}$) . For $1\,\mathrm{W\,m^{-1}\,K}$ both the temperatures are below the cutoff temperature and hence, this is used for the subsequent set of simulations.

before the temperature drops below the transition temperature (and remains relatively constant) is not optimal because capacity will not be fully utilized, since the PCM has not completely re-solidified. Hence a time period of 60 s is chosen between multiple sprint cycles. The maximum surface temperature increases with each cycle as shown in Figure 7.13(b). The increase in temperature with every sprinting cycle



(a)



(b)

Figure 7.13. Maximum transient surface temperature for the sprinting power profile shown in Figure 7.11 for two scenarios - paraffin wax (which undergoes phase change) and a material with identical properties to paraffin but without phase change. These test cases highlight the effect of latent heat. Thermal conductivity of paraffin (enhanced) is $1\,\mathrm{W\,m^{-1}\,K}$ (see Figure 7.12) (a) Maximum transient surface temperature for 1 sprinting cycle. A $5\,^{\circ}\mathrm{C}$ drop in the maximum temperature is observed for the paraffin wax undergoing phase change. (b) Maximum transient surface temperature for 5 sprinting cycles. The cutoff temperature is $40\,^{\circ}\mathrm{C}$ as shown by the black dotted line. For 5 power cycles, the surface temperatures increase above $40\,^{\circ}\mathrm{C}$ after 2 sprint cycles. The end time for both cases is 1000 s but the results are shown until 300 s and 400 s only to clearly illustrate the effect of peak power.

is due to thermal mass (mC_P) of each component and the exhaustion of latent heat of PCM. The simulation endtime is 1000 s, however the results are shown until 300 s to 400 s.

7.4 Package Level Simulations

In the previous section, the processor was modeled as a uniform block of silicon. However, a typical processor package consists of multiple layers and has localized heat generating regions on the die (hotspots). For example, the silicon die is typically attached to the substrate by solder bumps and interconnects encapsulated in an epoxy. This section discusses model refinements at the processor level. Specifically, here the package is modeled as a flip-chip assembly since they are extensively used in microprocessors [101]. In a conventional flip chip assembly, the die is inverted and solder bumps, known as Controlled Collapse Chip Connections (C4), make electrical connections between the die and substrate. The short electrical connections enable high performance applications. Ball Grid Arrays (BGAs) connect the package to the board. Wide variations in materials and geometries exist - for example, the die can be located above or below the substrate and a plastic or ceramic casing can be used as the mold and each combination leads to a variation in the design.

Figure 7.14 shows the model geometry in Comsol. For ease of modeling, the die is located above the substrate. Underfill and mold caps are modeled as thin layers. Also, the thermal conductivity of underfill is enhanced (i.e.effective thermal conductivity approximation) to account for the solder bumps (C4 connections), which are not modeled as a separate layer. This simplification is done to preserve the generality of the model. The ball grid array is modeled based on the Exynos 7420 processor (used in the Samsung Galaxy S6) [102]. A grid independence confirms the mesh is appropriate before integrating the package level model with the experimental setup (device level). The Power Management Integrated Circuit (PMIC) and CPU are located on the diagonal of the die and modeled as boundary heat sources. The PMIC

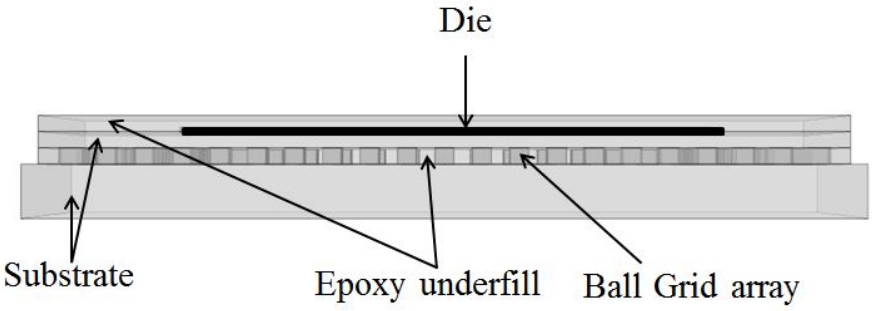


Figure 7.14. Side view (Y-Z plane) of flip chip package in Comsol. To account for the solder bumps (interconnects) between the die and the substrate, thermal conductivity of the underfill epoxy layer is enhanced.

Table 7.4.
Material properties for the die floorplan study shown in Figure 7.18. Thermophysical properties are used from the Comsol database [92].

Component	Material	Thermal conductivity (W/(m K))	Specific Heat (J/(kg K))	Density (kg/m^3)
Die	Silicon	130	700	2329
Underfill	Epoxy	0.35	1000	1600
Substrate	FR4	0.3	1369	1900
BGA	Solder	50	150	9000
	Epoxy	0.35	1000	1600

dissipates a constant 1 W of power and a linear ramp profile from 0 W to 10 W in 30 s is applied to the CPU (see Figure 7.15). Material properties are shown in Table 7.4.

The sides and the bottom surface of the substrate are treated as adiabatic walls. Similar to the device level models, natural convection and diffuse-surface ($\epsilon = 0.9$) radiation boundary conditions are applied to external surfaces. Figure 7.16 shows the variation of maximum die temperature with grid sizing and the associated compu-

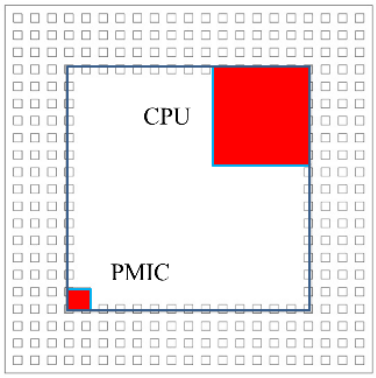


Figure 7.15. Top view (X-Y plane) of flip chip package in Comsol. Solder bumps are modeled as repeating arrays which were translated laterally. The heat sources on the processor - the PMIC and CPU are highlighted by red filled rectangles.

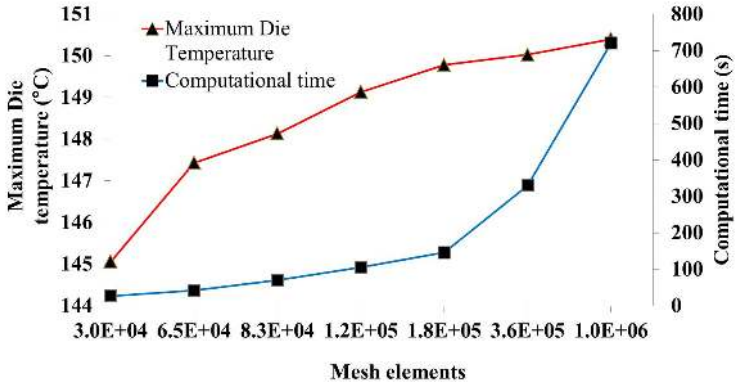


Figure 7.16. Grid independence test of maximum die temperature (in °C). Time taken for each trial is shown on the secondary vertical axis (in s). There is an $\approx 0.4\,°C$ difference between 3.6×10^5 and 1.0×10^6 mesh elements but the computational time is doubled. Hence, for subsequent simulations mesh size of 3.6×10^5 is chosen.

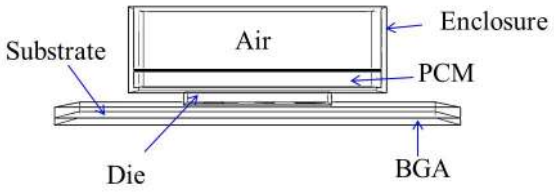


Figure 7.17. Schematic of the model geometry in Comsol for studying the feasibility of PCMs "on-chip". PCM (thickness 2 mm is contained in a copper enclosure 10 mm × 10 mm × 5 mm which is attached to the package. The package comprises of a die which is attached to the substrate via underfill (not labeled in Figure). The package is attached to the device using BGA. Effective material properties to ensure the generality of the model. Different floorplans of heat sources on the die found in literature are used to study the temperature distribution.

tational time. The mesh with 1.04×10^6 cells had 2.8 times more elements than the previous mesh and took almost twice as long to compute. However, the difference in maximum die temperature was $\approx 0.4\,^{\circ}\mathrm{C}$. Based on the added computational expense and the relative change in temperatures, we chose 3.60×10^5 elements are used for subsequent simulations.

7.4.1 Study of Various Die Floorplans

In experiments (see Chapter 5), an enclosure containing PCM is attached to the package to evaluate the performance of the PCM. This setup is an example of placing the PCM "on-chip". (see Section 2.3.2). Here, this experimental setup is modeled in COMSOL (see Figure 7.17) in order to interrogate and validate the experimental results. The Single Board Computer (SBC) has a Qualcomm Snapdragon APQ 8064 processor. *Due to limited public information on connection of package to the device, the BGA is modeled based on the Samsung Exynos 7420 processor.* The location and magnitude of heat sources in APQ 8064 processor,are based on the work of De Vivero

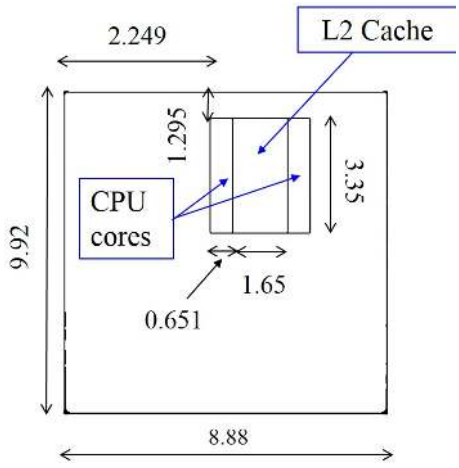


Figure 7.18. Heat source locations in Qualcomm Snapdragon APQ 8064 processor. 3 W are applied to each CPU core from 10 s to 30 s and 1 W is applied at other times. A constant power of 0.847 W is applied to L2 Cache. All dimensions are in mm(Figure reproduced with permission from [48].

et al. [48], who used McPat [103], integrated power, area, and timing modeling tool, to estimate the power consumption of various components (CPU,on-chip L2 cache and board level components) on the APQ 8064 processor. Similar to device level models, these components are modeled as boundary heat sources (see Figure 7.18). Other board components are not modeled as heat sources since their total power consumption is three orders of magnitude lower (i.e.in mW) than other components. Since the processor temperatures exceeded the maximum operating temperatures of the die by $\approx$ 30 °C (considering maximum allowable temperature of 110 °C) as shown in Figure 7.16, the die floorplan was refined further based on inputs from our project sponsors as shown in Figure 7.19 (See Table 7.5 for material properties). A copper enclosure of 10 mm $\times$ 10 mm $\times$ 5 mm is attached to the die and paraffin wax is completely filled in the enclosure. Perfect interfacial contact is assumed. Natural convection ($h = 5\,\mathrm{W\,m^{-2}\,K^{-1}}$) and diffuse radiation boundary conditions ($\epsilon = 0.9$) are applied to all surfaces exposed to ambient. The effect of adding PCM is compared with two baseline cases - no PCM (enclosure has an air pocket) and filled with a "wax-like"

material which has identical properties but does not change phase (see Figure 7.20). The PCM increased the time taken to reach 90 °C by 70 s when compared to just the enclosure on top of the die and 27.5 s relative to the "wax-like" material (no phase change) case.

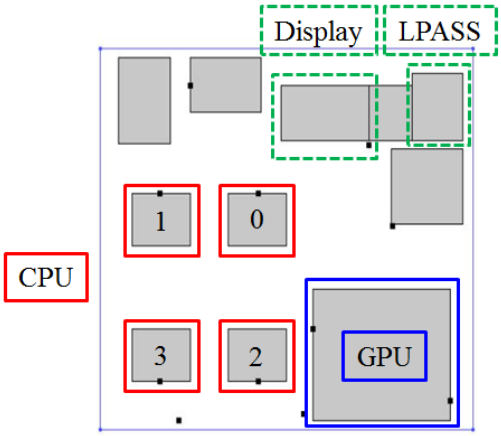


Figure 7.19. Heat source locations in Qualcomm Snapdragon APQ 8064 processor. The CPU and the GPU are the primary heat sources and are enclosed within red and blue boxes (solid outline), respectively. The CPU cores numbered 0.3 dissipate 0.193 W and 1 and 2 dissipate 0.119 W. The GPU dissipated 0.8 W power. The LPASS and Display, enclosed in green boxes (dashed outline) dissipate 0.04 W and 0.035 W, respectively.

The processor temperatures increases rapidly and reaches 120 °C in 10 s. The models described above over-predict the operating temperatures (85 °C to 110 °C), potentially due to the assumption of isotropic material properties or incorrect magnitudes or duration of power spikes. Package level models are complex since a package contains many components and wide variations exist in the overall layout [104–106]. Further, material properties of most components are not publicly available. Also, typically, layers like underfill have anisotropic material properties and modeling them as a single layer with effective material properties is suitable only as a first level approximation. More importantly, most mobile devices use "soft thermal management

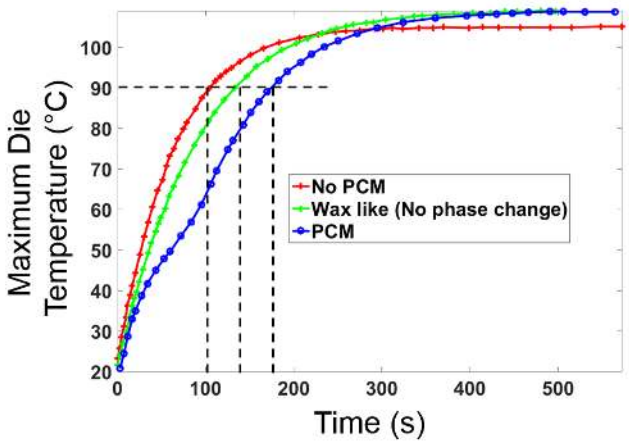


Figure 7.20. Transient variation of maximum die temperature (floorplan shown in Figure 7.19) for three cases - no PCM in enclosure , "wax-like" material without phase change and paraffin wax PCM. To highlight the influence of latent heat, the time to reach cutoff temperature (90 °C were evaluated (shown by black dotted lines). The latent heat of phase change increases the time taken to reach the cutoff temperature relative to the two baseline cases.

strategies", where clock frequencies (of CPU cores) are throttled down (to the lowest level depending on the case) if the temperature of a sensor exceeds the cutoff temperature, to protect the processor from overheating. To develop a thermal model that takes into account frequency throttling of cores, either the transient variation of core power consumption must be measured or the power consumption must be correlated to the readily available transient core frequency data. Initial attempts to experimentally extract transient power variation focused on using Android based applications ("apps"). Two apps - Powertutor [107] and App tuneup kit [108] were used. These apps only compute the average power consumption during the operations. The results varied by an order of magnitude between the two apps. Thus, a custom script is used to extract the core temperatures and clock frequencies of cores of the SBC

Table 7.5.
Material properties for Qualcomm APQ 8064 shown in Figure 7.19. Anisotropic material properties are given as a set of triplets as, $(\gamma_{xx}, \gamma_{yy}, \gamma_{zz})$, for a property γ and *xx,yy,zz* denote the directions of axes in Cartesian coordinate system.

Component	Thermal conductivity (W/(m K))	Specific Heat (J/(kg K))	Density (kg/m^3)
Die	Temperature dependent At 26.85 °C, $k = 148$ shown in Appendix A.	Temperature dependent At 25 °C, $C_p = 705$ shown in Appendix A.	2329
Underfill	[0.8,0.8,8.23]	544	3046
Substrate	[71.3,71.3,4.25]	948	2033
BGA	[0.045,0.045,16.9]	240	2151

with APQ 8064 processor. Dynamic (capacitive) power consumption in a processor and frequency are related as [109]

$$P = \frac{1}{2} C V^2 A f, \tag{7.1}$$

where P is the dynamic power consumption due to switching transitions, C is the capacitance which depends on transistor size, V the supply voltage (which is decreasing with successive fabrication generation), A is the activity factor which estimates the frequency of switching, and f denotes the clock frequency (which is increasing with time). Hence, neglecting parasitic effects due to leakage current , and assuming that all parameters listed above (in Equation (7.1)) are independent would predict that power is linearly proportional to frequency. Assuming this linear relationship, the instantaneous clock frequencies were normalized with respect to maximum clock frequency of a core to determine the power consumption as

$$P(t) = P_{max} \frac{f(t)}{f_{max}} c, \tag{7.2}$$

where c is the fitting parameter determined by comparison to data from experiments. However, this approach is not recommended and does not provide accurate power levels. Additional information from manufacturers is needed to better model the power dissipation. It was observed that the maximum core temperatures from experiments and simulations were comparable. For the case with no PCM (only the enclosure attached to the die), the maximum core temperature from the experiment was 82 °C and from the simulation was 78 °C when the GPU power was neglected and $c = 1.1$. Also, for both cases, the fitted temperatures peak early by around 100 s. Although the temperature curves match qualitatively, a more quantitative analysis requires finding the relationship between power and clock frequency of a core which is non-linear.

7.5 Conclusions

In summary, we developed device and package level computational models for various power profiles and evaluated them (1) on time taken to reach cutoff temperatures at the processor and the surface (2) maximum temperature and spatial temperature distribution in the package. The device level models estimate the heat flow through various components, for example, the back plate, middle plate, and case. Also transient device level simulations showed that the addition of PCM (near the processor) increased the time taken to reach cutoff temperature by a minimum of 16 s and a maximum of 1000 s depending on the properties of the PCM. Also, feasibility of using PCMs for computational sprinting was explored and found that PCMs when enhanced with metallic fillers (thermal conductivity of $1\,\mathrm{W\,m^{-1}\,K}$ reduced the surface temperature by 5 °C. The key challenge was the low thermal conductivity of the PCM after melting which was partially offset by the presence of high thermal conductivity components like EMI shield. The package level models initially focused on internal details of chip package - substrate, BGA , interconnects, and die. The interconnects were modeled as a pattern of legs. The floorplans and the package details were modified (for example, interconnects were modeled as an array of legs

and separately as a single layer with effective material properties) to ensure that the maximum die temperature was below the operating temperature. Finally, to validate the experimental results the clock frequencies of the cores were used assuming a linear relationship between core power consumption and clock frequency. A qualitative fit was obtained and this relationship needs to be further explored since it is non-linear.

CHAPTER 8. CONCLUSIONS

8.1 Summary

The trend of enhanced or added functionality for consumer electronic devices coupled with a reduction in form factor (specifically thickness) continues. This results in a manifold increase in power density from the package and other components for example, battery, and display. However, thermal limits for different components (CPU, device surface, *etc.*) remain unchanged unchanged. Active cooling mechanisms, for example, circulating a coolant or using a fan, are challenging to implement due to thickness and weight. Passive cooling strategies are a promising alternative due to absence of moving parts and relative packaging ease. PCM based thermal management is one such strategy that exploits the latent heat of phase change to dampen the temperature spikes thus increasing the operating time of the device before cutoff temperatures are reached. This dissertation focuses on identifying and understanding key metrics involved in design for using PCM for electronics thermal management. Successful implementation of a PCM-based passive thermal management system is a multi-step process which begins by identifying suitable integration locations of the PCM in the device and strategies for adding the PCM at the desired location. For example, the PCM can be impregnated in a metallic filler (e.g.foams), encapsulated, embedded with graphite nanofibers, and\or placed between or in fins or honeycomb structures (see Chapter 2).

Both the location and the method for implementation depend on the thermophysical properties of the PCM, particularly thermal conductivity and latent heat. Cross plane intrinsic thermal conductivity and interface thermal resistances of PCM-based TIMs are measured using miniaturized reference bar method. IR imaging is used for non-contact temperature measurements (Chapter 3). The key challenge in these

measurements is the pumpout and the transient nature of phase change process. The latter is investigated further via Comsol models and that the temperatures along the horizontal centerline of the reference - sample - reference stack tend to a quasi steady state after initial transient effects due to sensible heat capacity subside (Section 3.3), which indicates that this measurement can be extended to PCMs once a quasi steady state is reached. Latent heat and transition temperatures are characterized using DSC for a range of PCMs: unenhanced paraffin wax as well as well as wax based PCMs enhanced with polymers and graphite. The graphite based PCM with a relatively high thermal conductivity had the lowest latent heat since addition of high thermal conductivity fillers simultaneously reduces the overall heat storage capability.

In-situ characterization of these PCMs is done using an Android based development board (Chapter 5). The PCM is housed in an enclosure and attached to the die (Figures 5.1,7.17). The effect of enclosure size, enclosure materials, and PCMs is studied by measuring surface and core temperatures. Enclosures with larger base area increases the cutoff time by 2.48 times relative to an enclosure with same height but smaller due to enhanced heat spreading of the enclosure. However, local hotspots are created due to low thermal conductivity of PCMs for certain enclosure sizes. The results indicate that thermal conductivity and latent heat need to be optimized according to packaging constraints (enclosure sizes and weight of PCMs).

Device and chip level computational models are developed to study the effect of these properties, identify other integration locations, and validate the experimental results. For device level models, metallic solder and graphite based PCMs placed near the chip increase the cutoff time by as much as 20 times relative to organic PCMs. Package level models are built to validate the experimental results and study the effect of PCM without structural components in a mobile device (e.g.middle and back plates, case, surface, and display) (Section 7.4). Only a qualitative fit between the experimental and simulation results is obtained since a linear relationship between between clock frequency and core power consumption is assumed.

These thermal models are a step towards understanding the impact of properties of the PCM and various components, for example, the case, back plate, underfill, and interconnects, on the key metrics including cutoff time and maximum temperature. The effect of integration location of the PCM is more convenient to determine computationally. Thus, design space exploration studies serve as a first level filter and can be used to identify the range of material properties and integration locations, which can be interrogated further using experiments.

This work experimentally and numerically illustrates the improvement in thermal performance expected with a PCM. This improvement depends on a range of parameters including the device geometry, processor power profiles and material properties of the PCM and the device. A preliminary effort is made to identify and establish a link between these parameters which can serve as a stepping stone to develop more comprehensive design guidelines.

8.2 Future Work

Much work is still required before PCMs can be integrated in commercial electronic devices. An important challenge is the need for leak-proof enclosure. PCMs can be impregnated in foams to create a form-stable structure which prevents the leakage due to surface tension effects and eliminates the need for an enclosure [110]. This provides a leak-proof option for integration and their *in situ* thermal performance can be investigated using the experimental framework discussed in Chapter 5. For *in situ* tests, it is essential for the selected benchmark to have a constant runtime, independent of the setup (die only or filled / unfilled enclosure). A repeatability test for LINPACK 2 benchmark with 10 trials showed that the runtimes vary by upto 30 s and depend on the configuration of the experimental setup. However, since the increase in cutoff time in most cases is above 100 s, the trends discussed for *in situ* tests are still valid. However for most Android applications, the temperatures remain below the cutoff temperature, a custom benchmark, that for example, iteratively runs

a video or a computation may be required. Another alternative is to use a thermal test vehicle, which contains heater lines etched on the die rather than a computational architecture. Known heat fluxes and custom power traces can be applied to enable a more rigorous quantification. Additionally, a mock up of a device can be made consisting of all essential components to experimentally investigate integration of PCMs at the device level.

The accuracy of computational models depends on the model geometry among other parameters. A mobile device has numerous relatively thin layers (0.5 mm to 1 mm), for example, for wireless charging, which are often device specific. Also, it is challenging to find accurate dimensions and material properties of these components. The transient temperature profiles in response to a known heat flux can be used to determine the thermal conductivity and specific heat of individual components by using a foil heater which mimics the die as discussed by Gurrum *et al.* [95]. These properties can be used as fitting parameters in computational models to match the steady state temperatures from experiments. Further, the nonlinear relationship between core power consumption and clock frequency can be investigated further by considering effects of leakage current (which is proportional to die temperature), activity factor and change in capacitance [111–114]. The *in situ* tests and results from the computational models provide strong evidence that material properties of PCMs, structural components of the device in which PCMs are integrated and boundary conditions influence the design of PCM-based thermal management system. Since most engineering problems are constrained by cost, packaging, and fabrication constraints, it is useful to determine the relative influence or sensitivity of these variables on a desired parameter (for example, time taken to reach cutoff temperature) which enables a design space exploration. Also, uncertainties regarding these variables due to measurement errors can be quantified via a similar approach to give a better understanding of the impact of measurement errors in the overall design. For example, the thermal conductivity characterization needs to be improved if it has a high error associated with it but also causes a significant impact in the overall design.

Further, the effect of ambient temperatures on cutoff times can be explored. The numerical models in the present work assumed an ambient temperature of 20 °C. However, ambient temperatures can vary depending on the location and time. Higher ambient temperatures imply lower heat dissipation through convection and the PCM will melt faster. The effect of ambient temperatures can be studied experimentally by placing the experimental setup inside a thermally controlled chamber.

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APPENDIX

APPENDIX A. MATERIAL PROPERTIES OF SILICON

Table A.1.
Temperature dependent specific heat capacity of Si chip (See Table 7.5).

Temperature (°C)	Specific heat capacity (J/(kg K))
-73.15	556.9
-23.15	648.7
25	705
76.85	757.7
126.85	788.3
226.85	830.7
326.85	859.9

Table A.2.
Temperature dependent thermal conductivity of Si used for package level models (See Table 7.5).

Temperature (°C)	Thermal Conductivity (W/(m K))
-272.15	6.93
-271.15	45.4
-270.15	138
-269.15	297
-268.15	527
-267.15	823
-266.15	1170
-265.15	1550
-264.15	1950
-263.15	2330
-258.15	4160
-253.15	4980
-243.15	4810
-233.15	3530
-223.15	2680
-213.15	2110
-203.15	1680
-193.15	1340
-183.15	1080
-173.15	884
-123.15	409
-73.15	264
-23.15	191
26.85	148
76.85	119
126.85	98.9
226.85	76.2
326.85	61.9
526.85	42.2
726.85	31.2
926.85	25.7
1126.85	23.5
1326.85	22.1

VITA

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