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Patterned Carbon Nanotube Thin-Film Transistors with Transfer-Print Assembly

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Abstract:

Conditions for the transfer printing of patterned carbon nanotube (CNT) films, along with a Au-gate, a poly methylmethacrylate (PMMA) dielectric layer and Au source-drain electrodes have been developed for the fabrication of thin-film transistors on a polyethylene terephthalate (PET) substrate. Chemical vapor deposition (CVD) grown CNTs were patterned using a photolithographic method.

Transfer printing was used to fabricate devices having both top gate and bottom gate configurations. Replacement of the SiO_2 dielectric with PMMA correlates with a decreased hysteresis in the transconductance behavior. Encapsulation of the CNTs between the polymeric substrate and dielectric layer yields ambipolar behavior. Variations in device performance are also observed as a function of CNT film density and channel length, suggesting changing contributions of the metallic and semiconducting CNTs to the transport mechanism.

I. Introduction:

Carbon nanotubes (CNTs)[1,2] have shown promise both as conducting and semiconducting materials for electronic components in transistors[3, 4] and sensors[5, 6]. Individual semiconducting, single-walled CNTs have been reported to have a mobility as large as 10^5 cm^2/Vs.[7] Circuits consisting of individual CNTs have also been fabricated[8]. However it remains difficult to fabricate devices based on individual CNTs. Techniques such as "find and wire"[7, 8], AFM manipulation[9], mechanical transferring[10], self-assembly[11] or electrophoresis[12] have been employed in the manipulation of individual CNTs and the fabrication of CNT devices. These techniques however are labor intensive and difficult to integrate into large-scale fabrication processes. Additionally, the electronic characteristics of single CNTs are dependent on CNT chirality[13]. This results in non-uniformity of the electronic properties from CNT-to-CNT. Therefore, for some applications, films of CNTs[14] present an interesting alternative to single CNTs as they avoid the difficulties of manipulating individual tubes and should average out the non-uniformities resulting from tube geometry variations.

CNT films can be patterned using various methods such as photolithography[15] and nanotransfer printing[16, 17]. CNT film transistors on inorganic and plastic substrates have both been demonstrated[16, 18, 19]. Such devices on a Si substrate with a SiO_2 dielectric layer have been shown to exhibit large hysteresis and a *p*-type transistor response[18]. On a polyethylene terephthalate (PET) substrate with a poly methylmethacrylate (PMMA) dielectric layer a similar CNT film has been shown to display little hysteresis and an ambipolar transistor response[16]. On plastic substrates these devices have the additional benefit of being flexible and transparent. Additionally, fabrication techniques incorporating flexible substrates have the potential for high volume manufacturing processes such as roll-to-roll printing[20].

For logic circuits it may be desirable to encapsulate the CNTs in order to stabilize them from environmental affects. However for sensors the CNTs need to be in communication with

the environment. Therefore both top gate and bottom gate CNT devices are of technological interest. Previously reported transfer printing methods were used to fabricate CNT thin-film transistor (TFT) devices in the top gate geometry[16]. In this paper the transfer printing method has been expanded to include the fabrication of bottom gate devices. For the fabrication of both top and bottom gate TFTs it is desirable to pattern the CNT films prior to transfer printing in order to isolate devices fabricated in close proximity to each other.

The transfer printing process has been described in detail elsewhere[21]. Briefly, the process relies on the differential adhesion of a printable layer (in this work the CNT film) to the transfer substrate (here a SiO_2/Si wafer) and the device substrate [a PET substrate (for top gate geometry) or a PMMA coated PET substrate (for bottom gate geometry)] as shown in Fig. 1. This means that the CNT film must have stronger adhesion to the plastic substrate than to the SiO_2/Si substrate onto which it was originally grown. Simultaneously, the plastic substrate must not stick to the SiO_2/Si substrate.

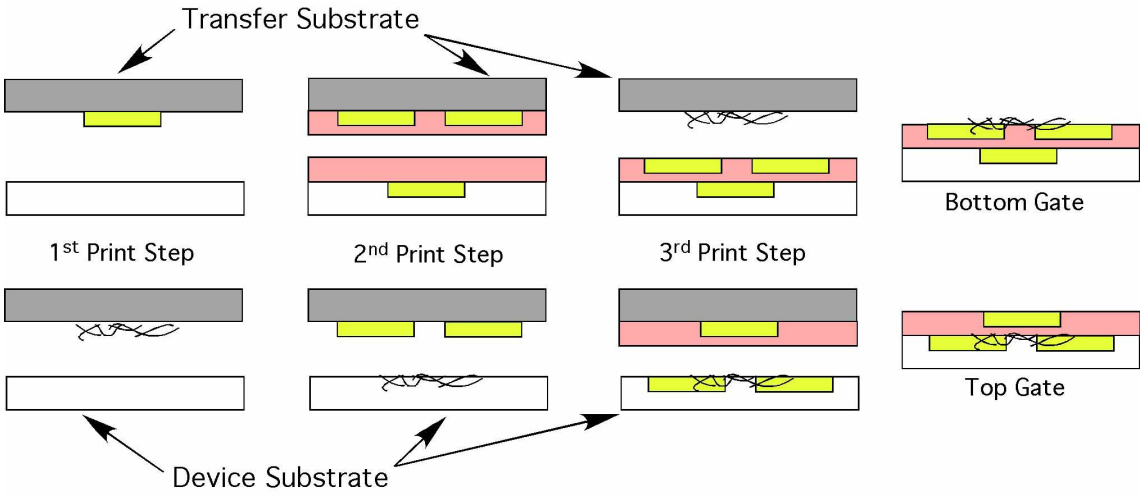

Figure 1. Illustration of the transfer printing steps for the fabrication of both bottom gate (top panel) and top gate (bottom panel) CNT TFT devices.

As a means of controlling the differential adhesion between the transfer substrate and the device substrates, we have developed three techniques for patterning the CNT films prior to transfer printing; (1) photolithographic patterning of chemical vapor deposition (CVD) grown CNTs, (2) CVD-grown CNT films from pre-patterned catalyst and (3) transfer printing of CVD grown CNTs. Bottom gate and top gate devices fabricated from CNT films patterned using technique (1) will be presented and discussed in this paper. Work is also underway to fabricate devices from CNT films patterned using technique (2) and (3). Advantages of these patterning techniques will be briefly noted.

II. Photolithographic patterning of CVD grown CNTs.

Photolithography offers a straightforward way of patterning CNT films. Because the CNT films are not optically visible using a contact aligner, prior to CNT growth Ti alignment markers were fabricated on the SiO_2/Si substrate. The films were then grown on the SiO_2/Si substrate by a CVD process using Ferric Nitrite nanoparticles as the catalyst[9,22]. The concentration of the catalyst determines the density of the CNT film and the CVD growth time

determines the average length of individual tubes in the film. The resulting film consists mostly of single-walled CNTs with an expected ratio of one-third metallic to two-thirds semiconducting[13]. The CNT film covers the entire surface of the substrate and therefore it is desirable to pattern the film prior to transfer printing.

To pattern the CNT film, photoresist was spin coated over the SiO_2/Si substrate surface containing the CNT film. The photoresist was exposed through a photomask to define 200 μm square areas. After developing the photoresist, the film area to be retained was protected by the remaining photoresist. By reactive ion etching (RIE) using an O_2 plasma, the CNTs outside the covered area were removed. Before removing the photoresist that covered the patterned film, the exposed SiO_2/Si surface was treated with a (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane self-assembled monolayer (SAM). This SAM treatment acted as a release layer to decreased the work of adhesion of the SiO_2/Si surface in order to establish a desirable differential adhesion against the plastic substrate[21]. Finally, the remaining photoresist was washed away with acetone and the resulting CNT film was ready to be transfer printed. A possible disadvantage of this patterning technique is that the CNTs have been exposed to various chemical treatments. Because of the SAM layer on the SiO_2/Si surface, the film cannot be annealed to remove possible surface contaminants following photoresist removal. Therefore patterning processes that do not expose the CNT film to resist processing chemicals are being developed. Two such patterning methods are (1) CVD-grown CNT films from pre-patterned ferritin catalyst and (2) transfer printing of CVD grown CNTs. These techniques have the advantage that no chemicals come in contact with the CNTs. Technique (2) has the further advantage that it is a two-step process.

III. CNT Device Fabrication:

After a CNT film was patterned as discussed above, it was incorporated into one of three types of devices. The first type of device is referred to as a control device where the patterned CNT film remained on the SiO_2/Si substrate on to which source/drain (S/D) electrodes were added. A cross sectional representation of such a device is shown as an insert in Fig. 3a. The second type of device is referred to as a bottom gate device on plastic where the patterned CNT film was the last component to be transfer printed onto the plastic substrate (see top panel in Fig. 1). The third type of device is referred to as a top gate device on plastic where the patterned CNT film was the first component to be transfer printed onto the plastic substrate (see bottom panel in Fig. 1). The fabrication steps for each of these three device types are described below.

1. Control devices:

Control devices were fabricated on the SiO_2/Si substrate that contained the as grown, patterned CNT film. 100 nm thick Au S/D electrodes were fabricated in contact with the CNT film using standard photolithography (negative photoresist for good lift-off) and e-beam deposition. The resulting control devices consisted of a doped Si global back-gate, a 500 nm thick SiO_2 dielectric layer and top contact Au S/D electrodes. The S/D electrodes for a control device were of the same geometry as those used in the transfer printed device shown in Fig 2.

2. Bottom gate TFT fabrication:

Bottom gate CNT TFT devices were fabricated using the transfer printing method described previously[21] and illustrated in Fig. 1. However the resulting devices were plagued

with problems of the CNT film shorting to the gate electrode through the 600 nm thick PMMA dielectric layer. This problem was solved by using a thicker dielectric layer.

A schematic representation of the transfer printing process for the fabrication of bottom gate devices is shown in the top panel of Fig. 1. Briefly, the fabrication of bottom gate CNT devices on plastic substrates was as follows. First, a 100 nm thick Au gate electrode was transfer printed onto a PET substrate (step 1 of fig. 1). Second, a 1 μm thick layer of PMMA was spin coated onto both the PET substrate containing the gate electrode and the Si substrate containing 30 nm thick Au S/D electrodes. The resulting S/D electrodes/PMMA dielectric bilayer was then transfer printed onto the PMMA coated PET substrate which contained the gate electrode (step 2 of Fig. 1). The final thickness of the PMMA dielectric layer was ~2 μm. The last step was to transfer print the CNT film so that the film was in contact with the S/D electrodes on the PET substrate (step 3 of Fig. 1). All the printing steps were performed at 500 psi and 170 ˚C for 3 min.

An optical image of an actual bottom gate device is shown in Fig. 2. From SEM and AFM measurements of the transfer and the device substrate it was determined that the CNT film was only partially transfer printed onto the PMMA dielectric surface for these devices.

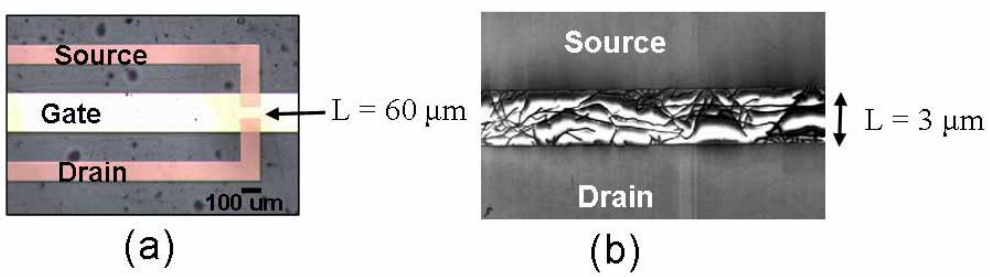

Figure 2. Optical (left panel showing a L = 60 μm device) and scanning electron microscope (SEM) (right panel showing a L = 3 μm device) images of a bottom gate CNT film device. Due to charging of the dielectric layer, the CNTs show up as dark lines in the SEM image. The dark spots in the optical image are from the underlying sample holder.

3. Top gate TFT fabrication:

Top gate CNT TFT devices were fabricated in a similar fashion to that described above for the bottom gate devices but with the order of printing reversed as illustrated in the bottom panel of Fig. 1. Here, the first step was to transfer print the patterned CNT film from the SiO_2/Si transfer substrate onto a PET device substrate (step 1 of Fig. 1). The second step was to transfer print 30 nm thick S/D electrodes onto the PET substrate such that the gap between the electrodes was aligned with the CNT film (step 2 of Fig. 1). Here, however, the self-assembled monolayer (SAM) treatments used previously[21] to improve transfer printing were omitted so that an untreated Au surface was in direct electrical contact with the CNT film. Omission of the SAM treatments (developed for printing involving a SiO_2 surface against a PMMA surface) was found not to be detrimental to the transfer printing of the S/D electrodes onto a PET surface. The last step was to spin coat a 600 nm thick PMMA dielectric layer onto the Si substrate containing a 100 nm thick Au gate electrode and transfer print the bilayer onto the PET substrate such that the gate was directly above the gap between the S/D electrodes (step 3 of Fig. 1). From SEM and AFM measurements of the transfer and the device substrate it was determined that the CNT film was fully transfer printed onto the PET substrate surface.

IV. Result and Discussion:

Fig. 3 shows the transfer characteristics for (a) control, (b) bottom gate and (c) top gate CNT TFT devices with a S/D electrode width of 100 μm and a channel length of 63 μm. The top gate and bottom gate devices, in which the CNT film is in contact with polymeric interfaces, show less hysteresis than the control devices, where the CNTs are in contact with a SiO_2 dielectric layer. Large hysteresis for CNT devices using a SiO_2 dielectric layer has been reported by others and attributed to charging defects in the dielectric layer[23]. The typical *p*-type transistor response is observed for all measured control and bottom-gate devices, whereas all measured top gate devices have shown ambipolar behavior. The origin of this different behavior has not been determined, but a possible explanation is that the CNT film may be doped *p*-type by contact with the SiO_2 dielectric layer[24] and not doped by the polymeric dielectric layer.

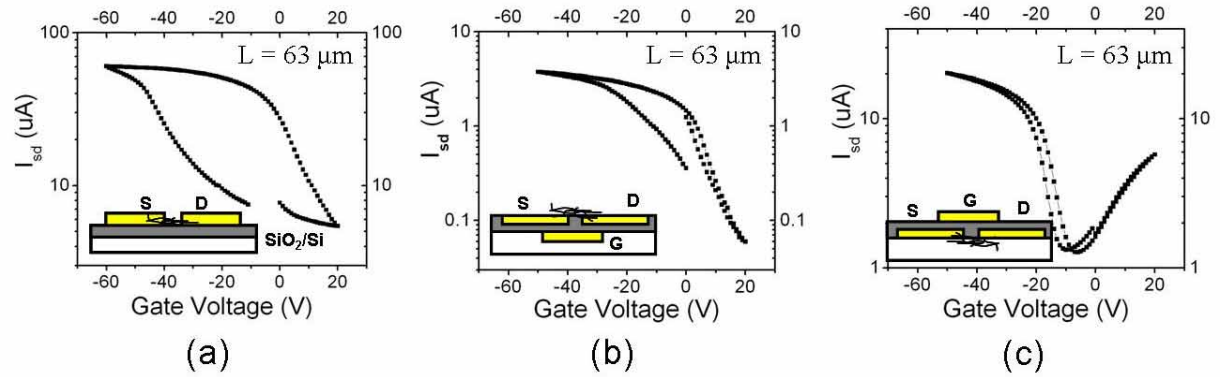

Figure 3. Transfer characteristics of a (a) control, (b) bottom gate and (c) top gate CNT TFT device. These devices have a channel length, L = 63 μm and S/D electrode width, W = 100 μm. Note the variation in vertical scale range in each graph. A cross-sectional schematic showing the device geometry is included for each device.

Transport characteristics were also studied as a function of channel length. Control, top gate and bottom gate devices were fabricated with channel lengths from 12 μm to 100 μm at intervals of 3 μm. Output characteristics of control devices at channel lengths 15 μm, 87 μm and 102 μm are shown in Fig. 4. At shorter channel lengths (< 80 μm, see Fig. 4a) the linear response of the control device resembles a resistor with a weak dependence on gate voltage (on/off ratio on the order of 10). At longer channel length (>80 μm) some devices exhibit output characteristics of a transistor with on/off ratio on the order of 10^2 and effective linear mobility (calculated assuming a uniform film covering the entire device area) on the order of 1 cm^2/Vs (see Fig. 4b) while other devices exhibit a resistive (>1 MΩ), non-linear behavior with weak gate dependence (see Fig. 4c). The output characteristics of top gate devices exhibit a similar qualitative behavior as compared to the control devices. Sheet resistivity (ρ) of control devices (Fig. 4) was observed to increase with channel length (L) from ρ(L = 15 μm) = 0.13 MΩ to ρ(L = 102 μm) = 1.56 MΩ, and those for top gate devices were observed to increase with channel length from ρ(L = 12 μm) = 1 MΩ to ρ(L = 93 μm) = 250MΩ.

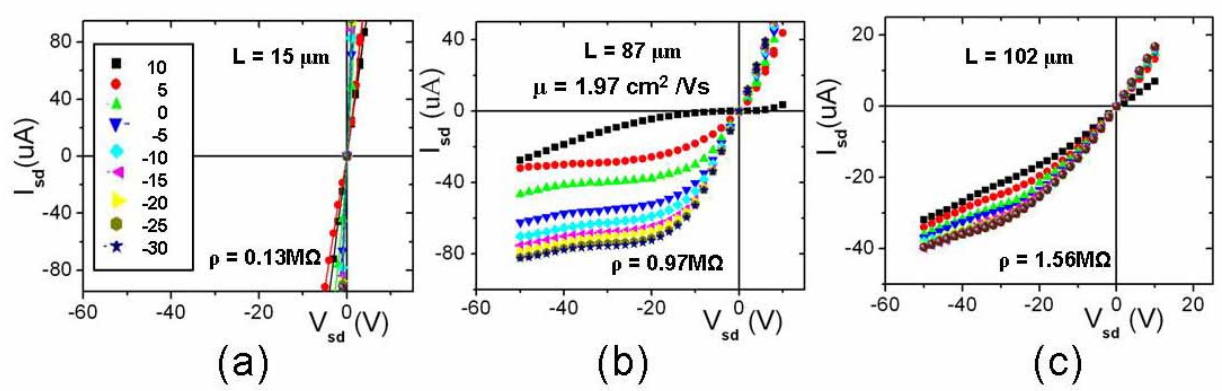

Figure 4. Output characteristics of control devices (SiO_2 dielectric) with electrode width, W = 100 μm and three different channel lengths. The inset in (a) shows the gate voltages corresponding to different curves in all the graphs. (a) Linear I-V characteristics with weak gate dependence is observed and on/off ratio on the order of 10. (b) Semiconducting behavior is observed with mobility of the order of 1 cm^2/Vs and on/off ratio on the order of 10^2. (c) The device acts as a resistive wire with sheet resistivity, ρ > 1.5MΩ.

Output characteristics of bottom gate devices were also measured as a function of channel length. Surprisingly good transistor behavior was observed in bottom gate devices independent of channel length. The average on/off ratio was found to be ~$1x10^3$. This is notably higher than the on/off ratios measured for either the control or the bottom gate devices. The effective linear mobilities were measured in the range from μ = 0.08 cm^2/Vs (for L = 12 μm) to μ = 13.7 cm^2/Vs (for L = 60 μm). Such mobility values are consistent with similar measurements of CNT film devices reported elsewhere[14, 18]. The different behavior of these bottom gate devices as compared to both the control and top gate devices may be related to the lower CNT density caused by the partial transfer print of the CNT film for the bottom gate geometry. Further studies of CNT film devices as a function of tube density and gate length are currently under investigation.

The variations in CNT device performance with channel length may be related to the mixture of approximately one-third metallic CNTs and two-thirds semiconducting CNTs. Such a network has been modeled using percolation theory[25]. It has been shown that for shorter channel lengths, devices are more likely to have purely metallic paths bridging across the gap between the S/D electrodes. As the channel length increases, the number of purely metallic paths between S/D should decrease to zero with such devices exhibiting a typical TFT behavior. In this percolation model, if there is a finite CNT-to-CNT contact resistance then, at some larger channel length the total resistance of the film will be large enough to suppress the TFT behavior. The channel length dependence of both the control and top gate devices reported in this paper are consistent with the qualitative behavior of such a model.

V. Conclusion:

A photolithographic method was used to pattern CVD grown CNT films. Transfer printing techniques were developed to fabricate CNT film devices into thin-film transistors on PET, a flexible, transparent substrate. Differences in device characteristics were observed for different geometries and materials used in the devices. Output characteristics were also found to vary dependent on CNT film density and channel length. Further work to quantify the effects of

the dielectric material, the density and channel length for the CNT films and the effect of exposed vs. encapsulated CNT configurations are in progress.

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