

# **Patterning metal contacts on monolayer MoS<sub>2</sub> with vanishing Schottky barriers using thermal nanolithography**

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**Two-dimensional semiconductors, such as molybdenum disulfide (MoS<sub>2</sub>), exhibit a variety of properties that could be useful in the development of novel electronic devices. However, nanopatterning metal electrodes on such atomic layers, which is typically achieved using electron beam lithography, is currently problematic, leading to non-ohmic contacts and high Schottky barriers. Here, we show that thermal scanning probe lithography can be used to pattern metal electrodes with high reproducibility, sub-10 nm resolution, and high throughput (10<sup>5</sup> μm<sup>2</sup>/h per single probe). The approach, which offers simultaneous in situ imaging and patterning, does not require a vacuum, high energy, or charged beams, in contrast to electron beam lithography. Using this technique, we pattern metal electrodes in direct contact with monolayer MoS<sub>2</sub> for top-gate and back-gate field-effect transistors. These devices exhibit vanishing Schottky barrier heights (around 0 meV), on/off ratios of 10<sup>10</sup>, no hysteresis, and subthreshold swings as low as 64 mV/dec without using negative capacitors or hetero-stacks.**

As conventional electronic devices reach their limits of performance, a search is underway in the microelectronics industry to find new materials<sup>1</sup>, fabrication methods<sup>2</sup>, and architectures<sup>3</sup>. Conventional lithographic techniques are, in particular, problematic in terms of resolution (optical lithography), operational costs (electron beam lithography, EBL), and their ability to pattern novel electronic materials and architectures. Among various novel materials being considered, two-dimensional molybdenum disulfide (MoS<sub>2</sub>) is of particular interest due to its large band gap, low dielectric constant, and heavy carrier effective mass<sup>3-6</sup>. Currently, a key issue in creating high performing field-effect transistors (FETs) based on MoS<sub>2</sub> and other transition metal dichalcogenides (TMDC) films is the poor quality of the metal contacts fabricated on these atomic layers, which gives rise to non-ohmic contacts, high Schottky barriers and large contact resistances<sup>1,7</sup>. Several approaches have been proposed to address these problems<sup>8</sup>, including trying different metallic alloys and doping<sup>9,10</sup>, using a metallic phase of MoS<sub>2</sub><sup>11</sup> or a h-BN layer as interface between the metal contact and the semiconducting MoS<sub>2</sub> layer<sup>12</sup>, and exploiting graphene as contact<sup>13-15</sup>. However, all these strategies are either non-scalable or have not yet been fully developed. They also all rely on conventional fabrication methods, typically EBL, for metal contact patterning.

EBL is currently the most widespread and reliable nanomanufacturing method for metal electrode patterning when nanoscale dimensions are required. The technique requires ultra-high vacuum (UHV) and does not allow in situ imaging. Its scalability is also limited by the costs and complexity of a multi-beam systems. Furthermore, primary and secondary electrons in EBL, as well as ultraviolet (UV) exposure in optical lithography, can damage 2D materials, from graphene to TMDC films<sup>16-20</sup>. Moreover, resist contamination on the surface of the 2D material is a major impediment for the fabrication of high performing electronic devices<sup>21-27</sup>. Among other nanopatterning methods, laser direct writing is a promising technique that offers far-field three-dimensional, maskless and cost-effective optical beam lithography with high throughput, even if the diffraction-limit is a barrier for achieving nanoscale resolution. Laser direct writing has, for example, been shown to be effective in patterning electrodes by direct laser sintering of metal nanoparticle inks deposited on a substrate<sup>25</sup>.

In this Article, we report a strategy to fabricate metal contacts on 2D materials with high reproducibility. Our approach is based on a double polymer stack chemical etching/lift off process combined with thermal scanning probe lithography (t-SPL). Using a commercial system based on t-SPL<sup>2,28-31</sup>, top-gated and back-gated monolayer (a single atomic layer, 1L) MoS<sub>2</sub> FETs are fabricated with different metals as direct contacts on the MoS<sub>2</sub>. The approach does not require vacuum, allows for in situ simultaneous patterning and imaging of a monolayer of MoS<sub>2</sub>, can achieve sub-10 nm resolution, gives rise to no resist contamination, and completely eliminates damage from either electrons or photons. As a result, the t-SPL fabricated FETs exhibit on/off ratios up to 10<sup>10</sup>, Schottky barrier heights (SBH) close to 0 mV, and sub threshold swings as low as 64 mV/dec without using negative capacitors or hetero-stacks, outperforming EBL results in the literature<sup>4,32-36</sup>. Applications to other TMDCs are also reported. The technique,

which currently runs with a single scanning probe, has a throughput similar to EBL and can readily be implemented in a cost-effective manner to multiple probes to increase throughput.

## **MoS<sub>2</sub> FETs fabrication by t-SPL**

Our approach to patterning metal contacts uses a two-layer polymer stack (Fig. 1), uniformly spin coated on MoS<sub>2</sub> films. The top polymer layer is locally thermally decomposed/evaporated in less than 1  $\mu$ s using a heated nano-probe<sup>28-31</sup> in t-SPL (see Supplementary Information, and Supplementary Figure 1, Supplementary Fig. 2, and Supplementary Video 1), while the removal and optimal undercut profile of the exposed bottom polymer layer is obtained by selective chemical etching and prebake conditions (see Methods). Polyphthalaldehyde (PPA)<sup>29</sup> serves as the top layer resist (20 nm thick) due to its remarkable thermal sensitivity, while polymethylglutarimide (PMGI) is used as the sacrificial bottom layer (210 nm thick) for the high yield and high resolution metal lift-off process. Before starting the electrode patterning, the 1L MoS<sub>2</sub> structure is imaged *in situ* underneath the polymer stack via thermal nanoimaging (see Fig. 1a, Supplementary Information, and Supplementary Fig. 1). Single-digit nanometer patterns in PPA, with lateral resolution of less than 10 nm and vertical resolution of 1 nm, can be reproducibly achieved<sup>2,37,38</sup> (see Supplementary Fig. 2). Moreover, the PPA thermally decomposed products evaporate immediately without re-deposition on the substrate or contaminating the nanoprobe, facilitating a complete residual-free and clean patterning process. The patterned PPA does not require any chemical development and can readily be used as an etching mask with high mechanical stability. After t-SPL patterning of PPA (Fig. 1b), the PMGI layer is locally exposed without PPA residuals, and the patterned area can be directly imaged for checking the correct alignment of the pattern (Fig. 1c) before initiating the PMGI chemical etching (Fig. 1d). After PMGI selective removal, the patterned MoS<sub>2</sub> contact region is exposed and ready for metal deposition. The final step consists in the evaporation of the metal electrodes (Fig. 1e) and lift-off (Fig. 1f) (see also Methods). Figures 1g-i show optical images of different examples of t-SPL fabricated FETs on 1L CVD and exfoliated MoS<sub>2</sub> flakes, illustrating that both large pads (Fig. 1g) and fine electrodes (Fig. 1h) can be fabricated by t-SPL.

Imaging by atomic force microscopy (AFM) (see Fig. 1j) indicates that the patterned MoS<sub>2</sub> contact region is completely free of any resist residue, whereas the contact region after the conventional EBL process shows considerable resist residues. Extensive AFM characterization of different locations on MoS<sub>2</sub> flakes after t-SPL and EBL fabrication shows in the case of the EBL process damage of the flakes' edges and presence of residuals (see the Supplementary Section 3 and Fig. S4-S6). Furthermore, X-Ray Photoemission spectroscopy (XPS) indicates that these residuals are indeed residues of the PMMA resist used during the EBL process (see Supplementary Section 4 and Supplementary Fig. 7). Figure 1k shows the Raman spectroscopy characterization of a typical exfoliated 1L MoS<sub>2</sub> flake used for FET fabrication, confirming that the E<sub>2g</sub><sup>1</sup> and A<sub>1g</sub> modes are separated by 19 cm<sup>-1</sup>, characteristic of monolayer flakes<sup>39-41</sup>. The exfoliated<sup>42</sup> and CVD MoS<sub>2</sub> flakes used in this work have been all characterized by Raman spectroscopy to confirm their monolayer nature (see Supplementary Section 6 and Fig. 10).

Representative AFM images of monolayer exfoliated and CVD flakes used in this work are shown in Supplementary Fig. 11. The t-SPL fabricated 1L MoS<sub>2</sub> FETs channel region is also characterized by Raman spectroscopy after fabrication (see Supplementary Section 5 and Supplementary Fig. 9), confirming that the t-SPL process does not damage MoS<sub>2</sub>. We remark that, differently from t-SPL, it has been shown that, during EBL, electron beam irradiation can cause damage in 2D materials<sup>43,44</sup>.

The bottom device layer, in this case monolayer MoS<sub>2</sub>, is not heated ( $T < 50^{\circ}\text{C}$ ) during the t-SPL patterning process, as verified by thermal flow finite element simulations (see Supplementary Fig. 3). Moreover, after each writing line, the non-heated nano-probe reads the written line allowing for *in situ* correction, closed-loop patterning, and self-alignment. t-SPL also allows for imaging the surface before patterning using the same, non-heated probe used for t-SPL, for localizing the area where the patterns need to be fabricated and aligning features with nanometric precision, without the necessity of additional markers. The versatility of t-SPL allows the fabrication on a wide range of materials, as shown in Fig. 1i, where we display the optical image of an aligned top-gate (TG) fabricated by t-SPL on an exfoliated h-BN flake (see discussion of Fig. 2), in the SI we also report on monolayer WSe<sub>2</sub> FETs. Finally, the t-SPL throughput can be scaled up by multiplexing the nanoprobe arrays<sup>30</sup> (see Supplementary Fig. 1e), in contrast to EBL in which multiplexing is complex and costly.

### **t-SPL 1L MoS<sub>2</sub> FETs electrical characterization**

In order to demonstrate the capabilities of t-SPL, we fabricate dual-gate 1L MoS<sub>2</sub> FETs with aligned patterned top-gate. First, Pd/Au source and drain contacts are fabricated as shown in Fig. 1. Then, a 15-20 nm insulating h-BN flake is aligned and transferred on the FET as gate dielectric. After the coating of the PMGI/PPA layers stack, the topography of the system was acquired *in situ* via thermal nanoimaging. This process allows to directly visualize with nanometric precision the source/drain contacts underneath the resist as well as the h-BN flake, and precisely align the top-gate with no need for additional markers (see Supplementary Fig. 12).

Figure 2a shows a schematic of the cross section of a top-gate 1L MoS<sub>2</sub> FET, with the electrical connections used in the measurements. In Fig. 2b, the optical image of the FET is shown. The regular geometry of the rectangular 1L MoS<sub>2</sub> flake (red dashed line in Fig. 2b, see Supplementary Fig. 13 for the optical image of the pristine flake) allows the precise measurement of the channel length  $L = 1.9\ \mu\text{m}$  and width  $W = 3.5\ \mu\text{m}$ . Figure 2c reports on the room temperature transfer curve of the FET for a drain voltage  $V_{\text{ds}} = 2\ \text{V}$ , measured by recording the drain current  $I_{\text{d}}$  as a function of the top-gate voltage  $V_{\text{tg}}$ . It features a nearly-ideal 64 mV/dec subthreshold swing, combined with the highest on/off ratio reported in literature for a 1L MoS<sub>2</sub> FET of  $I_{\text{on}}/I_{\text{off}} = 5 \cdot 10^9$ . In the inset, the top-gate transfer curves are presented as a function of the back-gate voltage ranging from  $V_{\text{bg}} = -20\ \text{V}$  (yellow curve) to  $V_{\text{bg}} = +20\ \text{V}$  (blue curve), demonstrating the full functionality of the dual-gate t-SPL patterned FET. The high quality of the

t-SPL contacts is demonstrated also in Fig. 2d, where the output curves of the FET for small  $V_{ds}$  are presented. The curves, acquired by recording the drain current  $I_d$  as a function of the drain voltage  $V_{ds}$ , are linear, demonstrating the ohmic character of the contacts.

For evaluating the performance of the device in terms of on-current  $I_{on}$ , we performed additional measurements at higher  $V_{ds}$  and  $V_{tg}$  after keeping the device in vacuum for 1 week. In Fig. 2e, we report the  $I_d$  as a function of the  $V_{ds}$  up to 4 V, for different top-gate voltages ranging from  $V_{tg} = -2.5$  V (orange curve) up to  $V_{tg} = 10$  V (black curve). The device features an extremely high  $I_{on}=154$   $\mu$ A, which gives rise to the normalized value of  $I_{on}\cdot L/W= 84$   $\mu$ A, which is among the highest values reported for monolayer MoS<sub>2</sub> FETs (see discussion of Fig. 5). We remark that the corresponding transfer curve, reported in the inset, features a very low off current  $I_{off}$ , leading to the record-high  $I_{on}/I_{off} = 2\cdot 10^{10}$ . The equivalency of the source and drain currents, acquired throughout the whole measurements (see Supplementary Fig. 14), confirms the high quality of the h-BN gate dielectric and fabrication process. Fig. 2f reports the forward and reverse transfer curve at  $V_{ds} = 2$  V, plotted both in the logarithmic and linear scale. Importantly, it demonstrates a hysteresis-free transfer curve across the whole range of  $V_{tg}$ , due to the absence of defects and trapped charges at the dielectric interface. This provides an additional compelling demonstration that t-SPL enables a residue-free and defect-free fabrication process, which in turn preserves an extremely high quality of the materials and interfaces.

The electrical characterization of two back-gate exfoliated 1L MoS<sub>2</sub> FETs with Pd/Au contacts fabricated by t-SPL is shown in Fig. 3. The corresponding optical images of the devices are shown in the insets. The devices feature a channel length and width of  $L = 0.6$   $\mu$ m,  $W = 1$   $\mu$ m (Fig. 3a) and  $L = 1.9$   $\mu$ m,  $W = 3.5$   $\mu$ m (Fig. 3b). Room temperature transfer characteristics (drain current  $I_d$  as a function of the back-gate voltage  $V_{bg}$ ) are measured by sweeping  $V_{bg}$  up to +60 V with drain voltage  $V_{ds} = 2$  V. Both FETs show a considerably large on-current of 132  $\mu$ A and 112  $\mu$ A, which leads to normalized on-current values  $I_{on}\cdot L/W$  of 84  $\mu$ A and 62  $\mu$ A respectively, combined with extremely high  $I_{on}/I_{off}$  of  $3.5\cdot 10^8$  and  $3.4\cdot 10^9$ , respectively. The subthreshold swing is 500 mV/dec and 400 mV/dec respectively, which is remarkably low for a thick global SiO<sub>2</sub> back-gate<sup>45</sup>. The insets show the corresponding room temperature output curves, featuring a linear  $I_d$  ( $V_{ds}$ ) behavior at all  $V_{bg}$ , from -60 V to +60 V, and even at low temperatures (see inset of Fig. 4a), indicating an ohmic contact between the t-SPL patterned electrodes and MoS<sub>2</sub>. We remark that, as reported in the detailed comparison with literature of Fig. 5, these back-gate devices feature state-of-the-art on-current combined with record-high  $I_{on}/I_{off}$ .

In a direct metal-MoS<sub>2</sub> contact there are two main components contributing to the contact resistance, the tunneling barrier between the metal and MoS<sub>2</sub> due to the Van der Waals gap and the Schottky barrier between the contact and the channel region. Schottky Barrier Height values vary from 370-38 meV<sup>33-36</sup> for metals in direct contact with 1L MoS<sub>2</sub>, to 16 meV when using h-BN/MoS<sub>2</sub> stacks<sup>36</sup>. Values obtained between multilayer MoS<sub>2</sub> and contact metals vary between

50 meV with Ti and 30 meV with Sc<sup>46</sup>, larger SBH have been found for monolayer MoS<sub>2</sub> with Ti, precisely 350 meV, in part because of its smaller electron affinity (4.2 eV)<sup>42</sup>. The SBH is related to many factors and it is a complex phenomenon<sup>1</sup> which accounts for the work function difference between metal and MoS<sub>2</sub>, diffusion and doping of the metal atoms in the MoS<sub>2</sub> layer<sup>42,47</sup>, presence of defects<sup>48</sup>, and presence of adsorbates of various origin including resist residuals<sup>1,49</sup>. To evaluate the SBH of the t-SPL patterned electrodes, temperature dependent transfer characteristics are collected on exfoliated 1L MoS<sub>2</sub> FETs with different metal contacts.

First, the transfer curves of the t-SPL patterned FETs with Pd/Au electrodes (as reported in Fig. 3) are obtained at different temperatures at  $V_{ds} = 0.1$  V, as shown in Fig. 4a. For positive gate voltages, the drain current decreases with increasing temperature, indicating a metallic behavior, whereas for negative biases this temperature dependence is reversed, giving rise to insulating characteristics. This transition manifests as a crossing-over at  $V_{bg} \sim 10$  V in Fig. 4a, and it is known as metal-insulator transition (MIT)<sup>50-52</sup>. The corresponding output curves at 48 K are plotted in the inset of Fig. 4a, showing a linear behavior even at low temperatures. Together, the metallic temperature dependence shown in Fig. 4a, and the linearity of the I-V curves at all temperatures (see Fig. 3 and inset of Fig. 4a) indicate a vanishing SBH (also confirmed by the Arrhenius plots as a function of  $V_{bg}$  as described below here) and an ohmic behavior of the t-SPL patterned FET with Pd/Au electrodes.

Moreover, Al/Au contacts are patterned by t-SPL on 1L exfoliated MoS<sub>2</sub> flake. The temperature dependent transfer curves obtained at  $V_{ds} = 2$  V are shown in the inset of Fig. 4b. To evaluate the SBH, the variations of the current through the device as a function of  $V_{bg}$  under different temperatures are used to generate the Arrhenius plots reported in the Supplementary Fig. 15. It is well known that in a FET the current mainly depends on the thermionic emission and the thermally assisted tunneling, and when  $V_{bg}$  is below the flat-band voltage,  $I_d$  can be written as<sup>1,9,12,34</sup>:

$$I_d = A^{2d} T^{3/2} \exp\left(-\frac{q\Phi_B}{k_B T}\right) [1 - \exp(-\frac{qV_{ds}}{k_B T})] \quad (1)$$

where  $A^{2d}$  is the 2D equivalent Richardson constant,  $\Phi_B$  is the SBH,  $T$  is the absolute temperature,  $k_B$  is the Boltzmann constant, and  $q$  is the electronic charge. Since we are considering  $q \cdot V_{ds} \gg k_B T$ , Eq. (1) can be simplified to obtain a linear relationship between  $\ln(I_d/T^{3/2})$  and  $1/T$ . In particular, the SBH is determined from the slope of the Arrhenius plots and plotted as a function of  $V_{bg}$  in Fig. 4b. It can be clearly seen that the thermionic emission current dominates when  $V_{bg}$  is lower than the flat-band voltage, which corresponds to the voltage at which the activation energy stops to depend linearly on  $V_{bg}$ . Therefore, the flat-band Schottky barrier height for t-SPL patterned Al/Au contacts can be readily determined from Fig. 4b to be merely 12.5 meV.

To the best of our knowledge, 12.5 meV and the vanishingly small barrier observed in Pd/Au devices are the smallest SBH ever demonstrated in any EBL patterned direct metal contact on MoS<sub>2</sub> back-gated FETs<sup>1,33-35,42,53,54</sup>. The best value reported for 1L exfoliated MoS<sub>2</sub> direct contacts is 38 meV<sup>36</sup> and for multi-layer MoS<sub>2</sub> is 30 meV<sup>46</sup>. We notice that Al/Au contacts give larger SBH than Pd/Au in our t-SPL patterned FETs. The factors that could potentially influence the contact resistance and the SBH in a given metal contact include<sup>42,47 48 33,55</sup> variations in surface contamination, defect and surface states concentration in the material, field emission, metal/semiconductor wave function overlap (predicted for metals on graphene to result in an effective lowering of the metal work function that may also apply to MoS<sub>2</sub>), metal-induced gap states (MIGS), defect dominated Schottky barrier height, interface dipole formation, metal-semiconductor interaction induced gap states. Also, complex mechanisms which are metal specifics, have been highlighted as important factors in studying the metal/MoS<sub>2</sub> monolayer interface, for example s-electron metals such as Ag, Al, and Au have fully occupied d-orbitals and interact with MoS<sub>2</sub> weakly, whereas the d-electron metals such as Pd interact with MoS<sub>2</sub> strongly. We argue that the observed absence of damage at the edges and the residual-free surfaces observed for the t-SPL process as opposed to EBL (see Supplementary Fig. 4-7) may be the underlying reason for the observed vanishingly small SBH in the t-SPL 1L-MoS<sub>2</sub>-FETs. It is indeed possible that by freeing the metal-MoS<sub>2</sub> interface from polymer residuals, we may change the nature itself of the interface, e.g. by increasing the metal/MoS<sub>2</sub> interaction and the metal-induced-gap-states. Further experiments are required to understand the microscopic origin of the different contact behavior for different metals and for the t-SPL and EBL processes.

## Comparison of t-SPL FETs with literature results

To quantitatively characterize the quality of the t-SPL electrodes and compare them with state-of-the-art electrodes patterned with conventional methods, we have derived the contact resistance ( $R_c$ ) of the different t-SPL fabricated contacts on 1L MoS<sub>2</sub>. Since the contact resistance depends mainly on the quality of the contact interface and on the resistivity of the MoS<sub>2</sub> film itself, a reliable comparison should involve MoS<sub>2</sub> films having similar sheet resistance to separate the effect of the contact from the effect of the material properties<sup>1</sup>. Accordingly, in Fig. 5a we plot the contact resistance of t-SPL fabricated electrodes as a function of the sheet resistance ( $R_\square$ ) for both top-gate and back-gate devices shown in Fig. 2, Fig. 3 (see also Supplementary Fig. 16a and Fig. 17), Fig. 4 and Supplementary Fig. 19 (blue lines and symbols), and compare these values with the EBL results reported in literature<sup>42,56,57</sup> (red-yellow lines and symbols). We remark that the sheet resistance of a MoS<sub>2</sub> film can be modulated by changing the gate voltage in the corresponding FET.

In general, the contact resistance is expected to decrease with the sheet resistance. For example, the international technology roadmap for semiconductors (ITRS) 22-nm-node requirement for low-standby-power silicon-on-insulator FETs<sup>1</sup>, plotted in Fig. 5a (green dashed line), shows that the goal in terms of contacts formation is to reduce the intercept of the linear  $R_c$  vs.  $R_\square$  curves, i.e. to obtain contacts with lower contact resistance for samples having the same sheet resistance.

When analyzing the data related to EBL electrodes on MoS<sub>2</sub>, we notice that the  $R_c$  vs.  $R_\square$  data points for 1L exfoliated flakes follow the same curve, suggesting comparable contact quality (see the shaded stripe in red, as guide to eyes).

Here, by using t-SPL to fabricate the electrodes, we show that we are able to dramatically lower the  $R_c$  vs.  $R_\square$  curves for direct metal contacts on 1L MoS<sub>2</sub> in both top-gate and back-gate configuration. This is clearly demonstrated from the blue symbols reported in Fig. 5a. Data are extracted from transport measurements on transfer length measurement (TLM) structures fabricated on chemical vapor deposited (CVD) 1L MoS<sub>2</sub> (see Supplementary Section 11 and Supplementary Fig. 19 and 20), and using the Y-function method to analyze the data from the electrical measurements on top-gate and back-gate exfoliated 1L MoS<sub>2</sub> FETs as reported in Fig. 2, Fig. 3 and Fig. 4 (for the Y-function method, see the Supplementary Section 12 and Supplementary Fig. 21). It is evident that the t-SPL patterned contacts show one order of magnitude smaller contact resistance compared to EBL patterned electrodes for MoS<sub>2</sub> samples having the same sheet resistance. The lowest contact resistance obtained for a t-SPL FET with CVD 1L MoS<sub>2</sub> is  $\sim 20 \text{ k}\Omega \cdot \mu\text{m}$ <sup>56</sup> while, as expected, the t-SPL FETs with exfoliated flakes show much smaller sheet resistance than CVD MoS<sub>2</sub> with a minimum contact resistance of only  $3 \text{ k}\Omega \cdot \mu\text{m}$  at  $V_{ds} = 2 \text{ V}$ , for the device in Fig. 3a. This is one of the lowest values ever reported for direct metal MoS<sub>2</sub> monolayer contact<sup>1,33,42,56,58</sup> at this  $V_{ds}$ . For example, Liu *et al.* demonstrated a contact resistance of  $3 \text{ k}\Omega \cdot \mu\text{m}$  at  $V_{ds} = 2 \text{ V}$ <sup>42</sup>. We notice that the dependence of the contact resistance on the sheet resistance of the exfoliated MoS<sub>2</sub> t-SPL FETs follows the same line as for CVD MoS<sub>2</sub> t-SPL FETs, indicating that the improvement in contact quality is independent of material source or quality. While these curves represent the present benchmark of the t-SPL patterned electrodes, they can certainly be further improved by using additional strategies recently proposed in literature for improving contacts, such as the use of a dielectric tunneling layer<sup>36</sup>, 1T phase engineering<sup>11</sup>, and the use of graphene for the contacts<sup>15</sup>.

Figure 5b shows the detailed comparison of the on-current  $I_{on} \cdot L/W$  and off-current  $I_{off}/W$  of the t-SPL 1L MoS<sub>2</sub> FETs, with the best values found in literature. In order to compare effectively the contact quality in FETs with different geometries, the normalization to the channel width and length is crucial. In Fig. 5b red-yellow symbols and lines report the data for EBL 1L MoS<sub>2</sub> FETs<sup>3,4,56,59-64</sup>, while blue lines and symbols represent t-SPL 1L MoS<sub>2</sub> FETs presented in this work. Noteworthy, the great majority of the EBL FETs are characterized by relatively low normalized  $I_{on}$  below  $10 \text{ }\mu\text{A}$ , and the FETs characterized by higher on-current feature a correspondingly larger off-current, leading to a significant reduction of the  $I_{on}/I_{off}$ . Remarkably, t-SPL FETs feature a normalized  $I_{on}$  current which is among the best reported, combined with an extremely low  $I_{off}$  current leading to record-high  $I_{on}/I_{off}$  between  $10^9$ - $10^{10}$  for 1L MoS<sub>2</sub> FETs in both the top-gate and back-gate configuration.

In Figure 5c we report the comparison of the performance of t-SPL devices with the best results in literature concerning on-off ratio  $I_{on}/I_{off}$ , subthreshold swing SS and normalized on-current

$I_{\text{on}}$ <sup>4,58,60,62,64,65</sup>. We remark that, here, the comparison is extended to multilayer MoS<sub>2</sub> FETs, which are usually characterized by higher on-currents, and to different strategies for improving the FETs performances, such as the use of negative capacitor gate dielectrics. Moreover, the comparison between FETs fabricated by t-SPL and the best EBL results in literature<sup>4,33-36,42,58,64</sup> for only direct metal contacts on monolayer MoS<sub>2</sub> is summarized, as shown in Table 1. Finally, as an additional test, the back-gate t-SPL devices based on exfoliated 1L MoS<sub>2</sub> is compared with equivalent EBL devices fabricated in our laboratory, with the same contact metals and device geometry. The obtained results confirm the superior performance of the t-SPL devices and are shown in Section 9 (Supplementary Fig. 16-18) and Supplementary Table 1 of the Supplementary Information. Noteworthy, the results of this work, obtained by simple metal patterning via t-SPL, show remarkably better performances in terms of combination of 10<sup>9</sup>-10<sup>10</sup> on-off ratio, nearly ideal subthreshold swing of 64 mV, high normalized  $I_{\text{on}}$  and zero hysteresis. We anticipate that by combining the t-SPL metal patterning approach with the aforementioned methods, even higher performance MoS<sub>2</sub> FETs can be envisioned.

To demonstrate the generality of the approach also for other 2D semiconductors, back-gated FETs are fabricated via t-SPL on monolayer WSe<sub>2</sub> exfoliated on Si/SiO<sub>2</sub> substrates. The results are reported in the SI, in Supplementary Fig. 24. Along with these results we also include Table S3 where we compare the performances of a back gated monolayer WSe<sub>2</sub> FET fabricated by t-SPL with data from literature on FETs based on the same type of material. In particular, for a meaningful comparison, we compare the previously published transfer characteristics performances of n-FET WSe<sub>2</sub> with our data, by reporting both maximum on current and on/off ratio for monolayer and few-layer (< 5) n-FET WSe<sub>2</sub>. As clear from this Table, t-SPL can produce FETs with transfer characteristics having the highest on/off ratio and on current among n-type monolayer or few-layer WSe<sub>2</sub> FETs.

## Conclusions

We have shown that thermal scanning probe lithography can be used to fabricate high-quality metal contacts on 2D materials with high reproducibility. Electron beam lithography is typically used for metal nanopatterning when high resolution is needed, but the need for ultra-high vacuum and high-energy electrons limits its wider application. Compared to EBL, our approach offers advantages in terms of device performance and capabilities, including not requiring a vacuum, even for 14 nm-length channels, and simultaneous in situ imaging and patterning with an overlay accuracy better than 5 nm. We have used our t-SPL-based scheme to fabricate top-gated and back-gated FETs on 1L MoS<sub>2</sub> and 1L WSe<sub>2</sub>. By eliminating resist contamination, and damage from either electrons or photons, our MoS<sub>2</sub> FETs show linear I-V curves even at low temperatures, record low Schottky barrier heights (~0 mV), record high on/off ratios (10<sup>9</sup>-10<sup>10</sup>), and exceptionally low SS (64 mV/dec). t-SPL is compatible with standard etching procedures and could potentially be pushed to single-digit-nm spatial resolution, and, by multiplexing with thermal nanoprobe arrays<sup>30,66</sup>, to higher throughput. The approach could thus lead to low-cost, no-vacuum, one-step industrial metal nanomanufacturing.

364

## 365 **METHODS**

### 366 **Materials**

367 We use monolayer exfoliated MoS<sub>2</sub> flakes (from bulk MoS<sub>2</sub>, SPI) and monolayer  
 368 monocrystalline CVD MoS<sub>2</sub> triangular structures (from 2Dlayer) on highly doped Silicon  
 369 substrate covered with 285 nm of thermally grown Silicon Oxide. Exfoliated MoS<sub>2</sub> samples are  
 370 dipped for 2 h in Acetone to remove tape residuals, and then rinsed with Isopropyl alcohol  
 371 (IPrOH) before starting the fabrication. For the top-gated FETs, we use as top-gate dielectric h-  
 372 BN flakes mechanically exfoliated on SiO<sub>2</sub>/Si, which are annealed (300°C, 2h), and then  
 373 transferred onto the target 1L MoS<sub>2</sub> FET (back-gated) with a dry stamp-assisted pick-and-place  
 374 process. The thickness of the h-BN flake for the FET shown in Fig. 2 is 15 nm, as measured by  
 375 AFM. The t-SPL patterning scheme is then used to image and pattern *in situ* the top-gate without  
 376 markers.

### 377 **Device fabrication by t-SPL**

378 All MoS<sub>2</sub> samples are kept in contact with HMDS vapors for 90 s to promote polymer adhesion.  
 379 First, a solution of pure PMGI (Polymethylglutarimide, Sigma) is spin-coated on the samples  
 380 surface (2000 rpm, 35 s) followed by a quick baking. For device fabrication this step is repeated  
 381 three times; then, a PPA (Polyphthalaldehyde, Sigma) solution (1.3 wt % in Anisole) is spin-  
 382 coated on PMGI (conditions: 2000 rpm at 500 rpm/s for 4 s and then 3000 rpm at 500 rpm/s for  
 383 35 s) followed by a quick baking. With these conditions, a 20 nm thick PPA film on top of a 210  
 384 nm thick PMGI film is deposited on the samples surface. Patterning of PPA is performed using a  
 385 commercial NanoFrazor t-SPL tool (SwissLitho AG), which uses hot probes to locally heat a  
 386 resist<sup>37</sup> with nanoscopic resolution (more details are reported in the SI). During the lithographic  
 387 writing the tip is heated to reach about 200°C at the PPA surface. Finite element simulations of  
 388 the heat flow from the hot tip through PMGI, after all PPA is evaporated, have been performed  
 389 with the FEniCS platform to evaluate the heat temperature underneath PMGI on the MoS<sub>2</sub> layer,  
 390 as reported in the Supplementary Section 2 and Supplementary Fig. S3. Patterns are performed  
 391 with a pixel time in the range of 30-70 μs. For patterning large pads (size: 100 x 100 μm<sup>2</sup>) the  
 392 overlay and stitching routine is used<sup>66</sup>. For the chemical etching of PMGI after patterning,  
 393 samples are immersed in a solution of TMAH in deionized water (Tetramethylammonium  
 394 hydroxide AZ726 MIF, MicroChemicals) (0.17 mol/L) for 400 s, then rinsed with deionized  
 395 water (30 s), IPrOH (30 s) and finally dried with N<sub>2</sub>. Metal deposition is performed using an AJA  
 396 Orion 8E e-beam evaporator (Pressure ~10<sup>-8</sup> torr, evaporation rate: 1 Å/s). Finally, metal/resist  
 397 lift-off is performed by dipping samples in Remover PG (MicroChem) for a few hours, then  
 398 rinsing (IPrOH) and drying (N<sub>2</sub>). The back-gate t-SPL FETs presented in this paper have been  
 399 fabricated using different metals: Pd/Au (10 nm/10 nm), Pd/Au (10 nm/20 nm), Al/Au (10 nm/10  
 400 nm), and Pt/Au (10 nm/10 nm) for exfoliated MoS<sub>2</sub> (see Fig. 3, 4, Supplementary Fig. 15, 16, 17,  
 401 18, 21 and Supplementary Table 1), and Cr/Au for CVD MoS<sub>2</sub> (10 nm/20 nm) (see  
 402 Supplementary Fig. 19 and 20). Cr/Au (10 nm/20 nm) is used as metal for the top-gate.

### 403 **Electrical measurements**

Electrical characterization of CVD monolayer MoS<sub>2</sub> is carried out using a parameter analyzer and a home built shielded probe station working in vacuum (10<sup>-4</sup> Torr) with micro-manipulated probes. A 7651 Agilent DC source, a Keithley KE2400 source-meter and a 34401A Agilent Multimeter are used respectively for applying the gate voltage, the source-drain voltage and to read the drain current. Electrical measurements on exfoliated flakes are carried out following the standard routines for FETs by either using an Agilent 4155C semiconductor parameter analyzer in a vacuum probe station at a pressure of 10<sup>-3</sup> Torr, or a Keithley 4200-scs semiconductor characterization system in a Lakeshore probe station at a pressure of 10<sup>-5</sup> Torr. To avoid the capacitive coupling between the back and top-gates during the measurements of the top-gate devices, the back-gate is either grounded or biased.

#### **Samples characterization**

Tapping mode AFM images are collected in different areas of CVD monolayer MoS<sub>2</sub> flakes after EBL and t-SPL fabrication and resist removal, in order to systematically investigate the cleanliness of the samples and the presence of residuals from fabrication. The results are shown in the Supplementary Section 3 and in the Supplementary Fig. 4-6. Tapping mode AFM images are also collected to verify the monolayer nature of the CVD and exfoliated MoS<sub>2</sub> samples used in this work (see Supplementary Fig. 11), and before and after electrodes deposition in t-SPL fabrication to assess the resolution of the t-SPL technique (see Supplementary Fig. 2). Images are collected using a Multimode 8 AFM (Bruker) and PPP-NCH tips (Nanosensors).

Raman spectroscopy is used to establish the monolayer nature of all the exfoliated and CVD MoS<sub>2</sub> flakes used for t-SPL fabrication (see the Supplementary Section 6 and Fig. 110) and to investigate the contact and channel region for the t-SPL and EBL fabrication (see Supplementary Fig. 8 and 9). Raman spectra are collected using a Horiba LabRAM HR800 system coupled with an Olympus BX41 inverted optical microscope, and using a laser source with excitation wavelength of 532 nm. Laser power is adjusted to avoid sample damage, or any sample modification, as observed by optical microscopy. Spectra are acquired between 100-900 cm<sup>-1</sup> with 1s exposure time and as an average of 10 different measurements. The peak at 520.7 cm<sup>-1</sup> from the Silicon substrate is used as a reference for the position of the MoS<sub>2</sub> peaks. Reported spectra in Fig. S8, S9 and S10 are normalized with respect to the MoS<sub>2</sub> A<sub>1g</sub> peak.

XPS spectroscopy is used to investigate the residuals from EBL fabrication, as reported in Supplementary Section 4 and Fig. S7. XPS measurements are performed with a Physical Electronics VersaProbe II system (UHV pressure < 10<sup>-6</sup> Pa) and using Al K $\alpha$  radiation (1486.6 eV). The sample is mounted on a steel sample holder and grounded. The following conditions are used: analyzer acceptance angle = 20°; take-off angle = 45°; beam size = 200  $\mu$ m; pass energy = 11.75 eV (C1s); integration time = 200 ms/step; step size = 0.05 eV/step.

#### **DATA AVAILABILITY STATEMENT**

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request

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## **AUTHOR CONTRIBUTION STATEMENT**

X.Z., A.C., E.A., and X.L. patterned the metal electrodes by t-SPL. A.S.M.A. performed the electronic measurements on the t-SPL FETs. X.Z., E.A., X.L., A.S.M.A., D.S. and E.R. designed the electronic experiments and analysed the data on the t-SPL FETs. G.A., and X.L. fabricated and measured the EBL FETs. X.Z., M.S., and E.R. developed the two-polymer stack t-SPL method. W.J.Y. and J.H. designed and analysed the EBL data. T.T. and K.W. provided the h-BN samples. C.A. analysed the XPS data. A.C. and A.K. provided the WSe<sub>2</sub> samples and contributed to corresponding data analysis. B.S.L. and M.L. deposited Pd electrodes on t-SPL FETs. E.R. conceived and analysed all the experiments on t-SPL FETs. X.Z., A.C., E.A., G.A., J.H., D.S. and E.R. contributed to write the article.

## **FINANCIAL AND NON-FINANCIAL COMPETING INTEREST STATEMENT**

The authors declare no competing financial interests.

## **ADDITIONAL INFORMATION**

Supplementary information is available for this paper at <https://>

**Figure 1. The t-SPL fabrication process.** **a.** *In situ* thermal nanoimaging of the sample topography (see also Supplementary Section 1). Image of a monolayer MoS<sub>2</sub> flake underneath the PMGI/PPA polymer stack (230 nm). Scale bar: 4 μm. **b.** The PPA polymer film is locally evaporated by scanning a heated scanning probe on its surface at a throughput of 10<sup>5</sup> μm<sup>2</sup>/h. **c.** *In situ* thermal nanoimaging of the t-SPL pattern on PPA. Scale bar: 4 μm. **d.** Chemical etching of the now exposed PMGI polymer film, which uncovers selected areas of the MoS<sub>2</sub> surface. **e.** Metal contacts are deposited via evaporation. **f.** The PMGI and PPA films are removed via a lift-off process. **g, h.** Optical images of final devices fabricated on exfoliated and CVD monolayer MoS<sub>2</sub>, respectively. Scale bars: 50 μm (**g**) and 5 μm (**h**). **i.** Optical image of a top-gate contact fabricated on exfoliated h-BN flakes. Scale bar: 4 μm. **j.** Comparison between the exposed contact region after the chemical etching step and before metal deposition in t-SPL (left panels) and EBL (right panels) fabricated FETs on monolayer CVD MoS<sub>2</sub>, acquired inside (top panels) and at the boundaries (bottom panels) of monolayer CVD MoS<sub>2</sub>. Scale bars: 500 nm. **k.** Typical Raman spectra of monolayer exfoliated MoS<sub>2</sub> used for the fabrication of FETs via t-SPL.

**Figure 2. Aligned top-gate FETs on exfoliated 1L MoS<sub>2</sub> flakes patterned by t-SPL.** **a.** Schematic cross-section and electrical connections of a top-gate FET. Both the source-drain contacts and the aligned top-gate are patterned via t-SPL. The structure comprises the degenerately doped Si substrate as global back-gate, a 285 nm thermal SiO<sub>2</sub> as back-gate dielectric, and a 15 nm h-BN layer as top-gate dielectric. **b.** Optical image of the 1L MoS<sub>2</sub> FET, showing the source-drain Pd/Au electrodes (S-D) fabricated on the 1L MoS<sub>2</sub> (red dashed line) and the aligned top-gate Cr/Au contact (TG) fabricated on the h-BN dielectric. Channel length  $L = 1.9$  μm, channel width  $W = 3.5$  μm. Scale bar: 5 μm. **c.** Room temperature transfer curve of the top-gate FET measured at  $V_{ds} = 2$  V. Subthreshold swing = 64 mV/dec,  $I_{on}/I_{off} = 5 \cdot 10^9$ . In the inset, transfer curves at different back-gate voltages ranging from  $V_{bg} = -20$  V (yellow curve) to  $V_{bg} = 20$  V (blue curve). **d.** Small voltage  $I_d$  ( $V_{ds}$ ) curves at different top-gate voltages showing ohmic behavior of the contacts. **e.**  $I_d$  as a function of  $V_{ds}$  up to 4 V, at different top-gate voltages ranging from  $V_{tg} = -2.5$  V (orange curve) up to  $V_{tg} = 10$  V (black curve), showing a maximum  $I_{on} = 154$  μA. In the inset, transfer curve at  $V_{ds} = 4$  V, features an  $I_{on}/I_{off} = 2 \cdot 10^{10}$ . **f.** Forward (blue dashed line) and reverse (orange line) transfer curves in logarithmic and linear scales. The curves are hysteresis-free in the whole top-gate voltage range.

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645 **Figure 3. Back-gate FETs fabricated via t-SPL on exfoliated 1L MoS<sub>2</sub> flakes. a-b.** Room 648  
temperature transfer curves at  $V_{ds} = 2$  V of FETs with Pd/Au electrodes, fabricated on exfoliated 649  
1L MoS<sub>2</sub>. The Si/SiO<sub>2</sub> 285 nm substrate was used as global back-gate and gate dielectric, 650  
respectively. The devices feature  $I_{on}$  up to 132  $\mu$ A (**a**) and  $I_{on}/I_{off} > 3 \cdot 10^9$  (**b**). Scale bars: 2  $\mu$ m 651  
(panel **a**), 5  $\mu$ m (panel **b**). Insets: corresponding room temperature output curves at different 652 back-  
gate voltages  $V_{bg}$ .

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655 **Figure 4. Schottky barrier height (SBH) characterization of t-SPL FETs on exfoliated 1L 656**  
**MoS<sub>2</sub>.** **a.** Temperature dependent transfer curves of the t-SPL FET with Pd/Au electrodes 657  
reported in Fig. 3a ( $V_{ds} = 0.1$  V). Inset: corresponding output curves of the same FET at 48 K. **b.** 658  
Gate voltage dependence of the barrier height for a t-SPL patterned FET on 1L exfoliated MoS<sub>2</sub> 659  
with Al/Au electrodes, at  $V_{ds} = 2$  V. The deviation from the linear response at low  $V_{bg}$  (dashed 660  
red line) defines the flat band voltage and the SBH. Inset: corresponding temperature dependent 661  
transfer curves at  $V_{ds} = 2$  V.

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666 **Figure 5. Comparison of t-SPL MoS<sub>2</sub> FET performances with literature. a.** Contact 667  
resistance  $R_c$  of the electrodes as a function of the sheet resistance  $R_r$  of 1L MoS<sub>2</sub> FETs. The red, 668  
orange and yellow lines and symbols represent values extracted from literature for FETs 669  
fabricated by EBL. The blue lines and symbols show the results of t-SPL fabricated FETs which 670  
are extracted (right to left) from three back-gated FETs fabricated on 1L CVD (see 671  
Supplementary Fig. 19), 1L exfoliated MoS<sub>2</sub> flakes (as shown in Fig. 3 and Fig. 4), and a top- 672  
gate FET fabricated on 1L exfoliated MoS<sub>2</sub> flake (as shown in Fig. 2). The shaded stripes show 673  
the range of data corresponding to EBL data from literature (red) and t-SPL data from this work 674  
(blue). The green dashed line represents the ITRS 22-nm-node requirement for low-standby- 675  
power silicon-on-insulator FETs with the contact resistance down to 20% of the total resistance. 676  
**b.** On-current normalized to the channel width  $W$  and length ( $I_{on} \cdot L/W$ ), as a function of the  $I_{off}/W$ , 677  
for 1L MoS<sub>2</sub> FETs. The red-yellow symbols and lines represent EBL data extracted from 678  
literature. The blue symbols and lines show the t-SPL results presented in this work for 1L MoS<sub>2</sub> 679  
FETs in the back-gate (Fig. 3) and top-gate (Fig. 2) configurations. **c.** In-depth comparison of the 680  
performances of the best MoS<sub>2</sub> FETs presented in literature with the t-SPL results presented in 681  
this work.

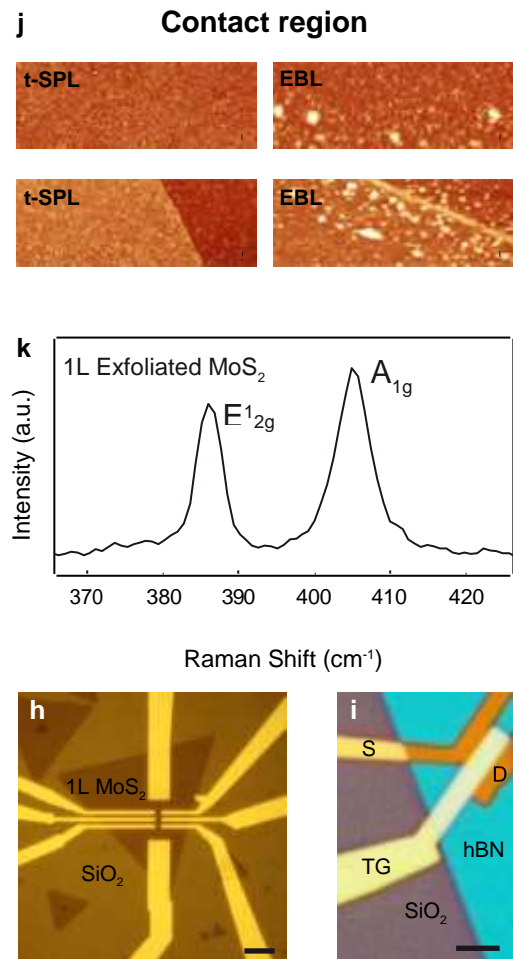
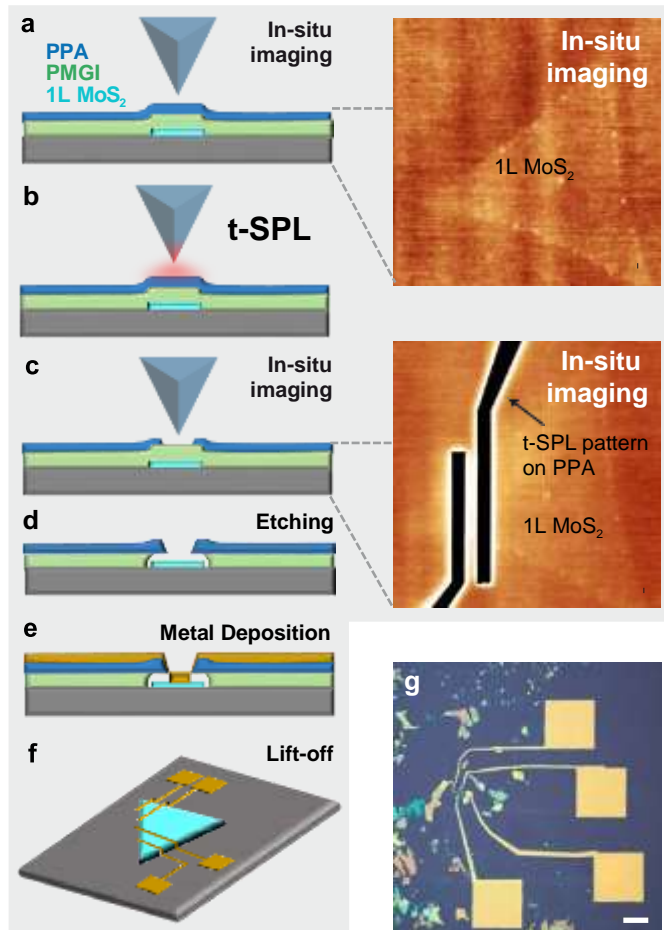
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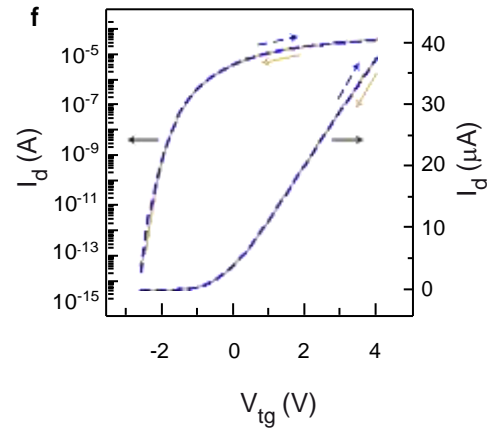
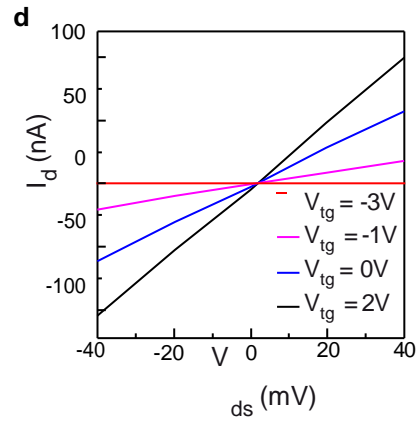
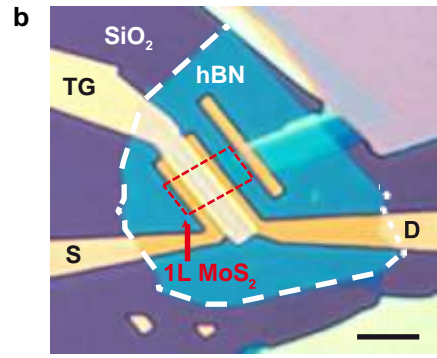
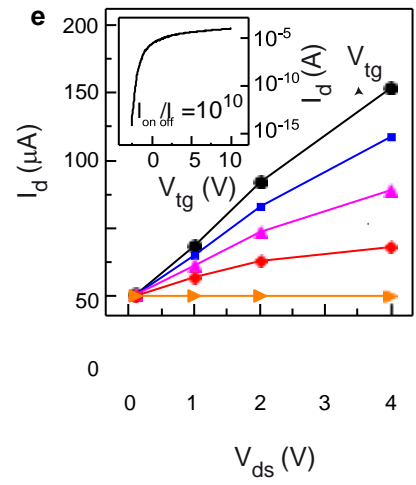
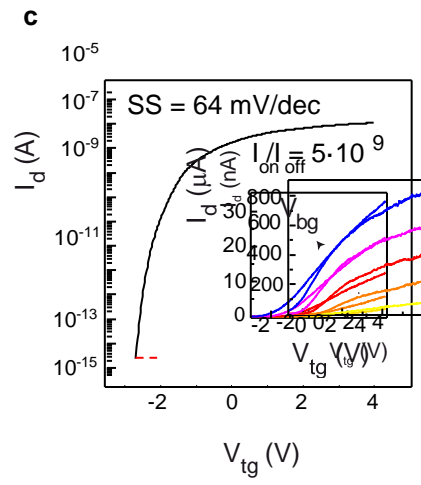
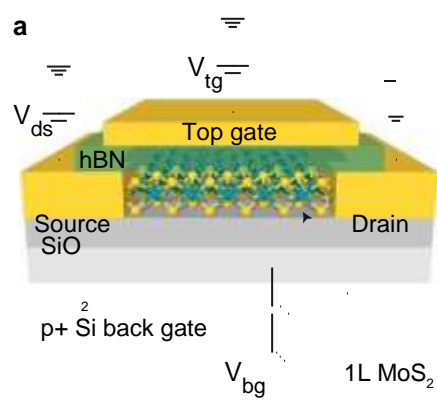
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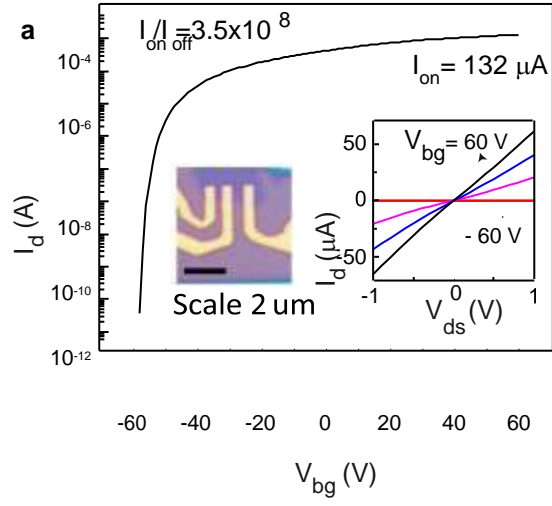
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	SBH	Rc	$I_{ON} / I_{OFF}$	SS	Requires UHV	Simultaneous imaging/patterning	Throughput	Resolution
t-SPL	~ 0 meV	3-6 kW mm (Back gate) 10 kW mm (Top gate)	$10^{10}$	64 mV/dec	NO	YES	$10^5 \mu\text{m}^2/\text{h}$	~ 10 nm
EBL	38 meV [36] 55 meV [35]	3 kW mm	$10^7$ [33]	74 mV/dec [4]			$5 \times 10^2 \mu\text{m}^2/\text{h}$	
in literature	60 meV [34] 110 meV [33]	(UHV) [58] 7 kW mm [33]	$10^8$ [4]	178 mV/dec [64] 410 mV/dec [42]	YES	NO	$10 \mu\text{m}^2/\text{h}$	~ 10 nm

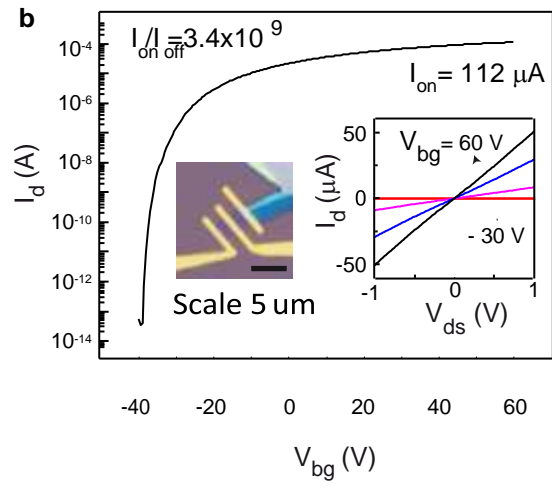
**Table 1.** Comparison of FETs based on monolayer MoS<sub>2</sub> with metal electrodes in direct contact with MoS<sub>2</sub> (no graphene contacts, h-BN tunneling layers or NC dielectrics).



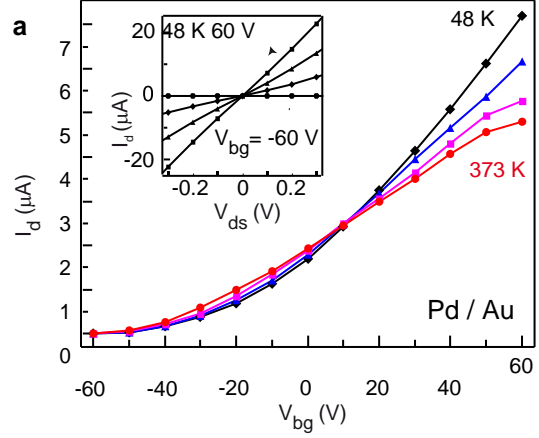




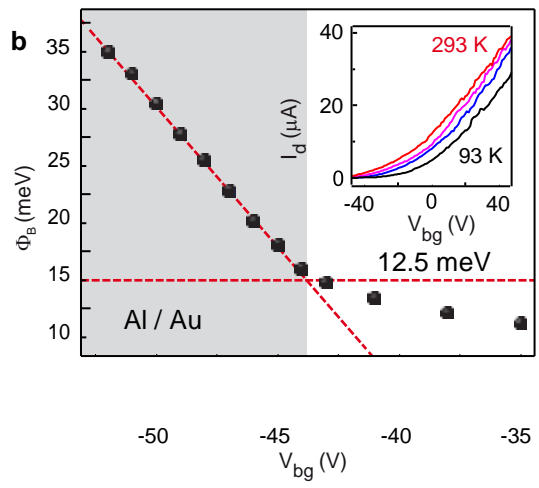
$V_{\text{ds}} = 2 \text{ V}$   
 $W = 1 \mu\text{m}$   
 $L = 0.637 \mu\text{m}$



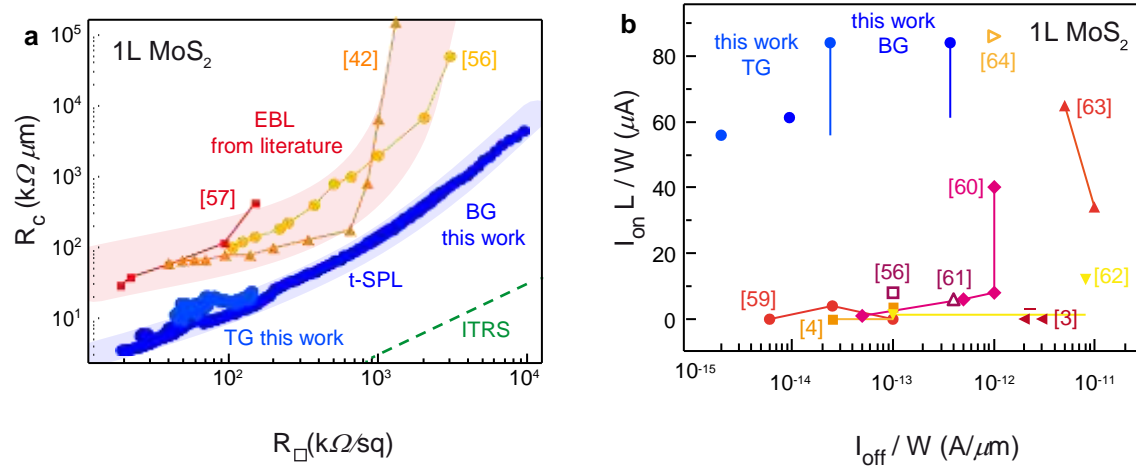
$V_{\text{ds}} = 2 \text{ V}$   
 $W = 3.4 \mu\text{m}$   
 $L = 1.9 \mu\text{m}$



$V_{ds} = 2$  V  
 $W = 1$   $\mu\text{m}$   
 $L = 0.637$   $\mu\text{m}$



$V_{ds} = 2$  V  
 $W = 3.4$   $\mu\text{m}$   
 $L = 1.9$   $\mu\text{m}$



**c**

Layers	Configuration	$I_{on}/I_{off}$ , S (mV/dec)	$I_{on} \cdot L / W$ ( $\mu$ A)	Ref.
Multilayer	Bottom Gate Negative Capacitor	$10^6 - 10^7$ , < 60	50	[60]
Multilayer	Bottom Gate (SiO <sub>2</sub> ) UHV Contacts	N.A.	45	[58]
1L	Top Gate	$10^6$ , 500	11	[65]
1L	Aligned Bottom Gate (Graphene contact)	$10^7$ , 64	1.5	[62]
1L	Top Gate	$10^8$ , 74	3.75	[4]
1L	Top Gate	$10^8$ , 178	86	[64]
1L	Top Gate	$10^9 - 10^{10}$ , 64	84	This work
1L	Bottom Gate (SiO <sub>2</sub> )	$10^9$ , 400	62 - 84	This work