PCB Thermal Design Improvement Through Thermal Vias

NADEZHDA KAFADAROVA, ANNA ANDONOVA
Department of Microelectronics
Technical University of Sofia
1797 Sofia, 8, Kl. Ohridski str.
BULGARIA
n_kafadarova@yahoo.com; ava@ecad.tu-sofia.bg

Abstract: - An approach based on design of different experiments for improvement the thermal paths in PCB through thermal vias is offered. An efficient thermal via placed on the PCB decreases the junction temperature of the package. In this paper elaborate study has been done in analyzing the effect of thermal vias and the ways to decrease the junction temperature by given number of computations. Thermal enhancement has been achieved by running the thermal simulations with and without thermal vias. Temperature profiles have been plotted in FLOTHERM. The thermal enhancement study focuses on the importance of thermal vias to a great extent. The simulation models are validated with experiments.

Key-Words: - **Thermal simulation, CFD, PCB, Thermal vias, Thermal resistance, Thermography**

1 Introduction

As thermal problems become more evident, new physical design paradigms and tools are needed to manage them. Such problems as increased interconnect delays, power consumption and temperature, all of which can have serious implications on reliability, performance, and design effort. The thermal resistance between junction-to-ambient (θ_{JA}) is highly dependent on the PCB (Printed Circuit Board) design factors. This becomes more critical for packages having very low thermal resistance between junction-to-case. θ_{JA} is used to characterize the heat dissipation ability of a package/board system from the die through the PCB board to the ambient environment. As the thermal resistance from PCB board to ambient is much larger than that from die to board, it is more significant to study the effect of the PCB board design on the thermal resistance θ_{JA} in detail.

The idea of using thermal vias to solve thermal problems is not new [1]. The use of thermal vias in packaging is implemented by two different methods. The first one is that the one end of via is attached to the bottom substrate, and the other is attached to the top substrate with a hole through to the substrate. The other is that the one end of via is attached to the top die, and the other is attached to the bottom die with a hole to the die. The thermal solution of vias depends on the thermal resistance. The various via configurations based on the first method of packaging will be analyzed.

The relationships between design parameters and the thermal resistance of thermal via clusters in PCBs were determined by simplifying the via cluster into parallel networks.

It has become of particular interest to design efficient heat conduction paths right into a PCB/MCM/chip to eliminate localized hot spots directly. Despite all the work that has been done in evaluating thermal vias, thermal via placement algorithms are lacking even with 2D PCB. As circuits and temperature profiles increase in complexity, efficient algorithms are needed to accurately determine the location and number of thermal vias [2].

An approach based on design of different experiments for improvement the thermal paths in PCB through thermal vias is offered.

2 CFD Simulations of Conduction Paths for Thermal Vias Impovement

It is well known that the thermal resistance of the package, especially, θ_{JA}, is highly dependent on the PCB in which the parts are mounted for thermal testing. The effect of the PCB is more critical when the package has extremely low θ_{JC} (or thermal resistance between junction-to-case) because the thermal resistance between case to PCB, and PCB to ambient air, becomes more dominant than that between die to package case [3].

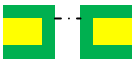
The remaining conduction paths extend from the device into the rest of the layers (both copper and dielectric) through the thermal vias underneath the device. These conduction paths, if optimized through proper design of the thermal via array, are the most efficient paths in the structure for removing heat from the device.

When considering the design of the thermal via array, it is helpful to first identify an ideal structure for the purpose of heat conduction. After the theoretical ideal is established, the system designer can attempt to design in a more practical structure that will closely replicate the ideal structure.

All of the vias arrays are arranged to be on a regular pitch on a matrix pattern. The vias matrices vary from no

vias (0 x 0) to a large 4 x 4 array and the vias numbers vary from 0 to 16. Different location of thermal vias and the vertical and horizontal distances between the thermal vias are studied: once with the same distances of 0,8 mm between the thermal vias and other with different vertical of 2 mm and horizontal of 0,8 mm distances between the thermal vias respectively.
In Table1 are given different types of thermal via structures.

Table.1. The thermal via structures for the purpose of heat conduction investigations of PCB

Stucture	Ideal type copper slug	First type solder slug	Second type air slug
View with two Cu laers			

In Table 2 the design of experiment parameters for CFD simulation are shown.

Table.2. Parameters for CFD simulation
(K_{Cu}=385W/mK; K_{Ni} =59W/mK; K_{FR4}=0,4 W/mK; K_{Sn63}= 50,9W/mK)

PCB area 576 mm^2 (24 mm x 24 mm) FR4 thickness 1,2 mm Device dimensions 20mm x 20 mm x 1,5 mm			
Diameter of the via, mm	0,8	1	2
Vias array, XxY	2x2	3x3	4x4
Copper thickness, mm	0,04	0,08	0,12
Power dissipated,W	1	2	3
Ambient temperature, ^{0}C	20	40	60
Number of Cu layers	2	3	4

The number and size of the vias are limited by the size of the thermal pad and the capabilities of the PCB manufacturer, making their design relatively straightforward. For reliability in the manufacturing process, the drill diameter of the vias should be no less than 0,25 mm, and the center-line of the vias should remain 0,9 mm away from the edge of the thermal pad and from each other. It would seem that, since the purpose of adding this via structure is to replicate a solid copper slug, the designer should add as many vias as possible.
The value of the thermal conductivity, *K*, in any particular direction corresponds to the density of thermal vias that are arranged in that direction. Increasing the number of thermal vias in one direction increases the thermal conductivity in the other directions but in the direction of the smaller magnitude. For simplicity, the interdependence can be considered to be negligible, and the *K*'s in the *x*, *y*, and *z* directions can be considered to be independent to a certain extent.

The percentage of thermal vias, *m*, (also called thermal via density) in a thermal via region is given by the following equation:

$$m = \frac{nA_{via}}{wh} \quad (1)$$

where *n* is the number of individual thermal vias in the region, A_{via} is the cross sectional area of each thermal via, *w* is the width of the region, and *h* is the height of the region. The relationship between the percentage of thermal vias and the effective vertical thermal conductivity is given by:

$$K_{eff}{}^{z} = mK_{via} + (1-m)K_{layer}{}^{z} \quad (2)$$

where K_{via} is the thermal conductivity of the via material and $K_{layer}{}^{z}$ is the thermal conductivity of the region without any thermal vias.
The effective lateral thermal conductivity can be found using the percentage of thermal vias:

$$K_{eff}^{x} = K_{eff}^{y} = (1-\sqrt{m})K_{layer}^{lateral} + \frac{\sqrt{m}}{\frac{1-\sqrt{m}}{K_{layer}^{lateral}} + \frac{\sqrt{m}}{K_{via}}} \quad (3)$$

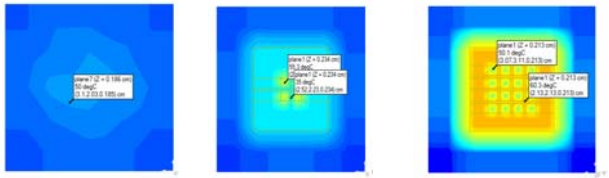
More often this lateral thermal conductivity is negligible value and it may be ignored.
The number of layers in a PCB has a very large impact on how well heat conducts away. While it is probable that the layer count of a design will be chosen for reasons other than thermal mass, this consideration should not be overlooked by the system designer.
One way to decrease the resistance of each layer is by increasing the copper weight of the layer. For cost-sensitive designs, increasing the copper weight provides an opportunity to get more thermal margin without having to incur the costs of additional board layers. As is the case with the number of thermal vias used, there is a law of diminishing returns for increasing copper weight. However, even a small change in copper weight has a large impact on the thermal performance of the PCB.
The effect of adding layers of copper and the impact of higher copper weight are examined by digital simulation of 4x4 vias array in both 2- и 4- layer design, as well as for two copper weight of 0,07 and 0,035mm.

3 Results

When considering the design of the thermal via array, it is helpful to first identify an ideal structure for the purpose of heat conduction. After the theoretical ideal is established, the system designer can attempt to design a more practical structure that will closely replicate the ideal structure.
Thermal via densities are increased from their minimum to maximum values, and the change in the temperatures and thermal gradients is observed. The thermal via regions are given the same minimum, midrange, and maximum thermal conductivity values. The minimum values correspond to the case where no thermal vias are

used. The maximum values correspond to maximum thermal via usage. In the midrange case, thermal via regions are given thermal via densities that are the average of the minimum and maximum values. The temperatures and thermal gradients in the minimum and maximum cases define the bounds on the thermal values that can be obtained from adjusting the thermal via densities. At the midrange with an average thermal via density of 24% in the thermal via regions, the maximum temperatures are 47% lower and the average temperatures are 28% lower than in the case where no thermal vias are used.

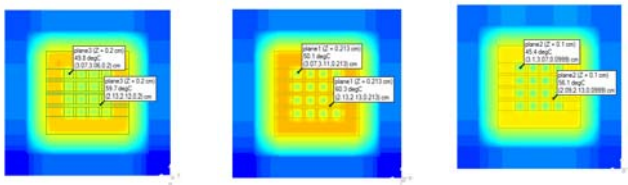
The number and size of the vias are limited by the size of the thermal pad and the capabilities of the PCB manufacturer, making their design relatively straightforward. For reliability in the manufacturing process, the drill diameter of the vias should be no less than 0.25 mm, and the center-line of the vias should remain 0.9 mm away from the edge of the thermal pad and from each other. It would seem that, since the purpose of adding this via structure is to replicate a solid copper slug, the system designer should add as many vias as possible. However, a law of diminishing returns makes the addition of a large numbers of vias somewhat unnecessary.



without vias 4 vias 16 vias

Fig.1. Effect of Number of Vias on PCB Thermal Resistance (at dissipated power of 1 W)

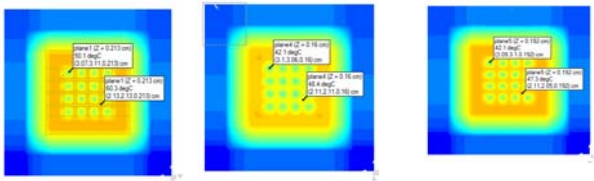
The effect of adding additional layers of copper can be seen in Fig. 2. This thermal model was created to predict the performance of a 4 x 4 via array in a 1-, 2-layer and 3-layer design, given a power dissipated of 1W and 0,04 mm copper layer. The thermal contour indicates that the heating in the 2-layer design is much more localized into the device. However, in the 4-layer design, the heat continues to progress towards the edges of the board. This is due to the parallel combination of the spreading resistance of the individual copper layers and the temperature field is the most equable in the area.



a)one Cu-layer b) two Cu-layer c)3 Cu-layer

Fig.2. Effect of PCB layer count on heat dissipation

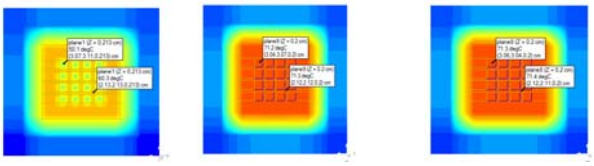
The effect of increasing the thickness of the copper layers is shown in Fig.3. The impact the higher copper weight has on the spreading resistance is readily seen from the simulation. These plots show the effects of higher spreading resistance on the designs with lower copper weight. The heat flow between the source (the outer regions of the PCB) and the ambient air is minimal, and the PCB's capability as a heat sink is restricted to the small region directly around the device.



thickness 0,04mm thickness 0,08mm thickness1,2mm

Fig. 3. Effect of PCB layer thickness on heat dissipation

Results of thermal simulation show that if thermally conductive fill material is not a viable option for the design, the vias can be optimized by specifying the thickness of the copper covering the internal walls of the via (Fig.4). If this specification is not directly described in the specification drawing for the PCB, the thermal conductivity of the via may be compromised by having a thin internal wall. It is only necessary to specify a minimum wall thickness, as any thickness over this range will only improve the thermal conductivity of the via. A good starting point is to specify a 0,035mm copper wall thickness, which should result in no cost increase to the design since this is a common practice. Increasing the inner wall thickness beyond this minimum requirement should be decided based upon the manufacturing capabilities of the PCB manufacturer.



a) air b) Ni c) Solder Sn63

Fig. 4. Effect of PCB via fill material

On the lower layers of the PCB, it has be greater control over the routing of the traces. In order to maximize the thermal performance of the device and PCB structure, it should keep the traces on the lower layers of the PCB as far away from the vias array as possible. This ensures that the solid area of copper under the device is as large as possible for maximum heat conduction away from the part. An illustration of this point is found in Fig.5.

The first trace, marked with number 1, runs parallel to the vias array. As heat flows out of the vias, it encounters a large thermal resistance created by the trace cutting across the copper plane. The second trace

configuration is better than the first because it is as far away from the thermal via array as possible.

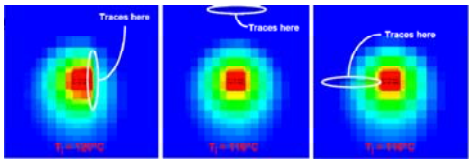
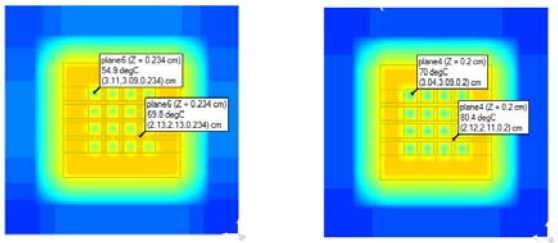


Fig.5. Effect of trace location and directions on heat conduction within the lower PCB layers

This ensures that heat conduction is only limited by the inherent spreading resistance of the copper layer itself. If it is not possible to avoid having traces close to the device, the third routing method can be used to limit the impact of the traces on heat conduction. Traces running perpendicular to the center of the device present a smaller crosssectional profile of thermal resistance to heat conducting away from the device.

On the Fig. 6 the effect of ambient temperature is shown.



$T_A = 25\ ^0C$ $T_A = 60\ ^0C$

Fig.6. Effect on ambient temperature at $T_j=100^0C$

θ_{jT} is defined as $\theta_{jT} = (T_j - T_{top})/P_{diss}$ where T_j and T_{top} are the junction temperature and the temperature at the top center of the package, respectively. θ_{jT} is often used to predict the junction temperature at the end user environment based on the temperature T_{top}. The temperature T_{top} can be measured by a IR camera at the top center of the package and is dependent on the PCB conductivity [4, 5]. The PCB with higher effective conductivity will give a lower value of θ_{jT}. The resultant of θ_{jT} measurement is shown in Fig.7.

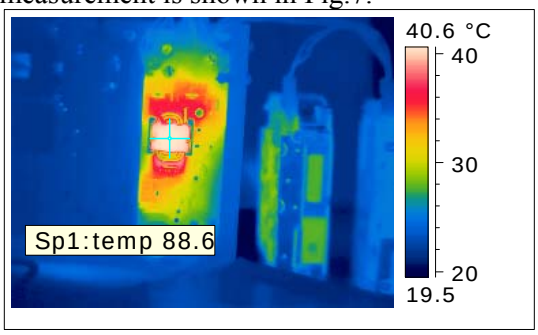


Fig. 7. The image of IR FLIR P640 camera shows the measured values at the top center of the package ($P_{diss} = 3W$, $T_A = 21{,}6^0C$, $T_j = 98{,}3^0C$ and $\theta_{jT} = 3{,}23\ ^0C/W$)

4 Conclusion

Thermal vias are generically added to PCB to achieve the desired thermal conductivities. The goal is to satisfy given thermal requirements using as few thermal vias as possible, i.e., keeping the thermal conductivities as low as possible. Furthermore, with the thermal via regions being oriented vertically, lateral thermal vias will have little effect. The thermal gradients in the vertical (z) direction are almost two orders of magnitude larger than in the lateral directions.

The important thing to remember concerning heat flow through the PCB and into the ambient is that the thermal resistance between the heat source and the cooler outer regions of the PCB must be kept as low as possible.

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