Peak Detector Effect in Low-Dropout Regulators

C. Palomar, F. J. Franco, I. López-Calle, J. G. Izquierdo, and J. A. Agapito

Abstract—The peak detector effect is a phenomenon that makes single event transients much longer once an error amplifier switches from linear to saturation zone due to the presence of external capacitors. This is so-called since it was discovered in a simple voltage reference in which a parasitic lossy peak detector was unwillingly built in the output stage. In this paper, peak detector effect is generalized to explain the appearance of long duration pulses in typical low dropout voltage regulator built with discrete devices. This effect has been related to the way in which the negative feedback loop is closed and to the kind of pass device in the output stage. Thus, if the linear voltage regulator consists in an error amplifier the output of which controls a current source, the peak detector effect will occur if the current source is unidirectional, the output load does not drain enough current and is in parallel with an external capacitor.

Index Terms—Long duration pulses, lossy peak detector effect, operational amplifiers, single event transients, voltage regulators

I. INTRODUCTION

T O THE authors' knowledge, one of the first reports of long duration pulses (LDPs) appeared in 2004 providing evidence of the existence of single event transients (SETs) on the order of 1 ms in an operational amplifier (op amp) [1]. During the following years, other authors confirmed the possibility of this kind of events [2]–[4]. Of particular importance was the work of Zanchi *et al* [4] who attributed the appearance of LPDs to external devices rather than internal components, i.e., LPDs in a band-gap BiCMOS voltage reference were related to an external capacitor used to stabilize the system and remove high frequency noise. The drawback of this approach was that the emitter-follower output stage of the reference was converted into a circuit very similar to that of a peak detector. For a better understanding, one must know that the structure of the device tested by Zanchi is very similar to that depicted in Section III-A2. In fact, the only difference between this typical regulator and some accurate peak detectors based on operational amplifiers is that the stable reference voltage of a linear regulator, V_{REF}, is a variable input signal in peak detectors, V_{IN}. Usually, this is not a drawback since in typical electronic systems nobody expects sudden changes in the

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reference voltage. However, if the voltage regulator is exposed to ionizing radiation, single event transients inside the error amplifier can create positive peaks at the voltage regulator output. These peaks will be captured by the parasitic peak detector the lasted until the capacitor is discharged through the load or the feedback resistors. The mechanism responsible for LPDs is more general since it is based on circuit topology.

In this paper we show that phenomena similar to the peak detector effect can occur in other kinds of voltage regulators and we will provide a mathematical framework for a better understanding of the problem. Finally, we will support the deduced theoretical properties with experimental results from several voltage regulators, built with discrete devices and tested in a pulsed laser facility.

II. GENERALIZATION OF THE PEAK DETECTOR EFFECT

A. Depiction of the phenomenon

Fig. 1 shows a block diagram of a generalized linear voltage regulator. An error amplifier, built with a simple op amp, sets the output voltage, V_{OUT}, to $\beta \cdot V_{REF}$ with a feedback loop through a voltage-controlled current source, $I_S \approx I_{OUT}$, that provides the current biasing the load impedance, Z_L.
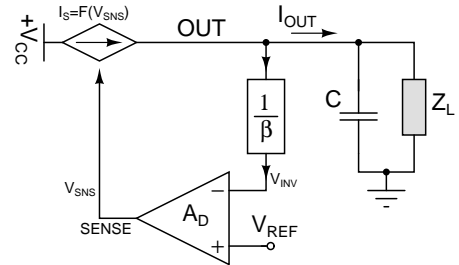

Figure 1. A generalization of how to build a linear voltage regulator.

Now, let us assume the following:
1) The current source is positive or even null if the value of V_{SNS} is low enough. In other words, the current can flow only in one direction. Besides, the function relating I_S & V_{SNS} is increasing so, at the bias point, its small-signal model is just $i_s = G_M \cdot v_{sns}$, $G_M > 0$. An important consequence of this assumption is that the path gain is positive so the loop must be closed at the inverting input to avoid positive feedback.
2) At the bias point, $V_{INV} \cong V_{REF}$ but, if somehow $V_{INV} > V_{REF}$ for a critical interval (T_{SW}), the error amplifier stops working in the linear zone, behaves as a comparator and jumps to negative saturation.
3) The impedance load is either a resistor, R_L, or a device with an almost constant quiescent current. In the first case, $I_{OUT} = V_{OUT}/R_L$ and, in the second, $I_{OUT} =$
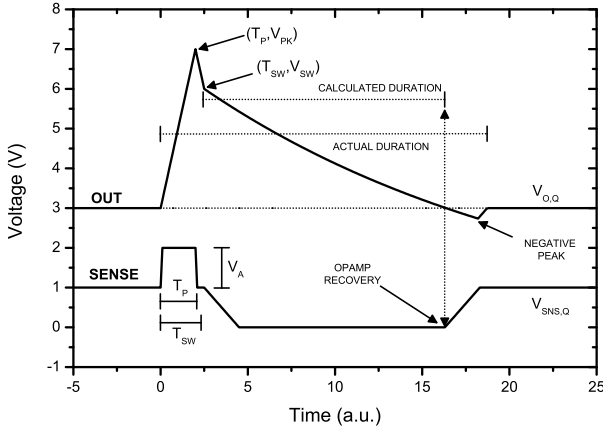
Figure 2. Stages and critical parameters during an LDP due to peak detector effect.

$I_Q + V_{OUT}/R_Q$. At any rate, both models converge to a simple resistor, r_o, in the small-signal model.

In this situation, the voltage regulator is prone to undergo LDPs *if the load is not good at draining current*. Let us suppose that an ion hits the error amplifier and a positive peak appears at $SENSE$. This pulse propagates to the current source and induces a positive current transient. If the current that must flow to ground through the load impedance is sufficiently large, the impedance cannot handle it and excess charge is stored on the capacitor. This stored charge leads to an increase of V_{OUT} and, in consequence, of V_{INV}. If this excess charge is not removed before T_{SW}, the op amp goes to negative saturation and switches off the current source until the capacitor is finally discharged through the load. For a better understanding of the parameters, Fig. 2 is included to visualize specific times and voltages.

This behavior of the op-amp switch is what distinguishes LPDs associated with the peak detector effect and other kinds of single event transients.

In some voltage regulator structures, like that of Section V-B3, $G_M < 0$. In this case, the feedback loop is closed at the non-inverting input and, as simmetry considerations predict, negative peaks instead of positive ones will create an excess of charge in the capacitor so the op amp output quickly goes to positive saturation. If, moreover, the current source switches off with high enough values of V_{SNS}, peak detector effect occurs.

B. Duration of the transients

As a first approximation, The duration of the transient is approximately the time required to discharge the capacitor. Assuming that at the bias point $V_{OUT} = V_{O,Q}$, and that $V_{OUT} = V_{SW} > V_{O,Q}$ when the op-amp blocks the current source, the capacitor voltage decreases until the output voltage again reaches the value at the bias point. At this point the op-amp operates in the linear mode and the regulator resumes proper operation. The equation controlling the discharge of the capacitor is given by:

$$C \cdot \frac{dV_{OUT}}{dt} = -I_Q - \frac{V_{OUT}}{R_X} \tag{1}$$

R_X being any kind of resistance connecting OUT to ground: Load, feedback resistors, parasitic resistances in the current source,... The exact solution of this equation is an exponential function that allows estimating the transient duration as:

$$T_{DUR} \approx R_X \cdot C \cdot \ln\left(\frac{V_{SW} + R_X \cdot I_Q}{V_{O,Q} + R_X \cdot I_Q}\right) \tag{2}$$

For a purely resistive load, R_L, with $I_Q = 0$, the duration is roughly estimated as:

$$T_{DUR} \approx R_L^* \cdot C \cdot \ln\left(\frac{V_{SW}}{V_{O,Q}}\right) \tag{3}$$

R_L^* being the equivalent of R_L in parallel with any resistor found in the circuit. After incorporating this little correction, $R_L \rightarrow R_L^* \equiv R_X$, as it is shown in Eq. 3. If the load is successfully modeled as a constant current sink, I_Q, the discharge process lasts for

$$T_{DUR} \approx \frac{C}{I_Q} \cdot (V_{SW} - V_{O,Q}) \tag{4}$$

C. Estimation of peak and switch-off voltages, V_{PK} & V_{SW}

Unlike the duration of the transient, the following section makes use of a very idealized version of the devices. In particular, until the trigger of the op amp, transients are considered as perturbations around the bias point so small-signal models are used.

Let us suppose that an ion hits the op amp and a transient appears at its output. In other words, $V_{SNS}(t) = V_{SNS,Q} + v_{sns}(t)$. This perturbation is amplified by the current source ($I_S(t) = I_{S,Q} + i_s(t) = I_{S,Q} + G_M \cdot v_{sns}(t)$) and reaches the output node. The DC component, drained by the load, is neglected and the perturbation must be studied with the small-signal model of the capacitor and the load. It is easily shown that the equation controlling $v_{out}(t) = V_{OUT}(t) - V_{O,Q}$ is:

$$i_s(t) = G_M \cdot v_{sns}(t) = C \cdot \frac{dv_{out}}{dt} + \frac{v_{out}}{r_o} \tag{5}$$

In actual networks, r_0 is the equivalent resistor for an array of three components in parallel: The load itself, derived form Fig. 1 (R_L, R_Q), the feedback network resistors and the output resistance of the voltage-controlled current source. In case of purely resistive loads, the third (and sometimes the second) component can be neglected. However nothing can be inferred for the current sink without knowing how it is implemented.

To solve Eq. 5, the transient will be modeled as a square pulse with a height, V_A, and a duration, T_P. In other words,

$$v_{sns}(t) = \begin{cases} V_A & if\ t \in [0, T_P] \\ 0 & if\ t \notin [0, T_P] \end{cases} \tag{6}$$

Actually, the initial transient should be modeled as a triangular spike rather than a square pulse. However, solving the equation is extremely difficult and the derived results hard to interpretet. Accepting Eq. 6, Eq. 5 is easily solved:

$$v_o(t) = \begin{cases} 0 & t < 0 \\ V_L \cdot \left(1 - \exp\left(-\frac{t}{r_o \cdot C}\right)\right) & 0 < t < T_P \\ v_o(T_P^-) \cdot \exp\left(-\frac{t - T_P}{r_o \cdot C}\right) & t > T_P \end{cases} \tag{7}$$

$$V_L = r_o \cdot G_M \cdot V_A$$

Obviously, the output cannot go beyond the positive power supply, $+V_{CC}$. If LDPs are liable to occur, $r_o \cdot C$ is much larger than the range of time of the initial transient at SENSE. Therefore, the previous equation becomes:

$$v_o(t) = \begin{cases} 0 & t < 0 \\ \frac{G_M \cdot V_A}{C} \cdot t & 0 < t < T_P \\ \frac{G_M \cdot V_A \cdot T_P}{C} \cdot \exp\left(-\frac{t - T_P}{r_o \cdot C}\right) & t > T_P \end{cases}$$

$$(8)$$

However, one must not forget that this evolution, following the assumption that the bipolar transistors are in forward-active zone, is suddenly altered at $t = T_{SW}$ when due to the op amp goes to negative saturation. In general, $T_P < T_{SW}$ so the output transient will show a peak value at

$$V_{PK} - V_{O,Q} = \frac{G_M \cdot V_A \cdot T_P}{C} \qquad (9)$$

and a switch-off voltage of:

$$V_{SW} - V_{O,Q} = v_o(T_{SW}) = \frac{G_M V_A T_P}{C} \cdot \exp\left(-\frac{T_{SW} - T_P}{r_o \cdot C}\right)$$

$$= (V_{PK} - V_{O,Q}) \cdot \exp\left(-\frac{T_{SW} - T_P}{r_o \cdot C}\right) \qquad (10)$$

Assuming $V_{PK}, V_{SW} \leq V_{CC}$.

D. Existence of negative peaks

Long duration pulses due to lossy peak detector effect are always bipolar since since the capacitor continues to lose charge until the op-amp recovery is complete (Fig. 2). In general, the value of this peak depends on the load and the output capacitor. Low capacitor or high DC output current values lead to larger negative peaks during the last stage of the transient.

III. PRACTICAL IMPLEMENTATION

A. From ideal blocks to actual devices

1) Typical low drop-out regulator: The network depicted in Fig. 3 is a practical implementation of Fig. 1. Throughout the paper, it will simply be called *TLDOR*. In this network, the voltage-controlled current source is the subcircuit containing Q1 and Q2. This block has every property listed in Section II-A: In fact, if V_{SNS} grows, so do I_{B1} & $I_{C1} = I_{B2}$ and this ends up with an increase of $I_S = I_{C2}$. Besides, if $V_{SNS} \to 0$, Q1 goes to cutoff state and blocks the Q2 base current. On the other hand, the β-block consists of two resistors, R_1 & R_2, so $\beta^{-1} = 1 + R_1/R_2$.

This structure is that of a typical low dropout voltage regulator [5] and similar structures have been tested under ionizing radiation [6], [7] and single events [2], [7]. In these two papers, LDPs due to peak detector effect were not reported, probably due to the use of very low load resistance values (2.2 Ω). D1 & D2 were added in series with the Q1 emitter to work as a DC shifter and place $V_{SNS} \sim 2 - 2.5\,V$. Thus, the output of the op amp is far enough from the dangerous negative saturation voltage ($V_{SAT,N} \sim 0.2\,V$).
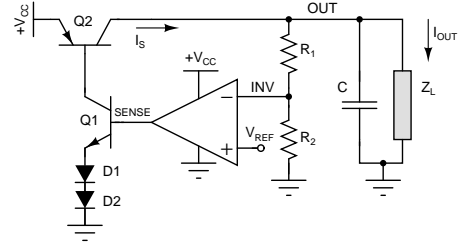

Figure 3. Practical implementation of a low dropout regulator.

Using the small-signal model of the transistors and diodes, it is easy to calculate the trasconductance of this network:

$$G_M = \frac{i_s}{v_{sns}} = \frac{h_{fe1} \cdot h_{fe2}}{h_{ie1} + N \cdot (h_{fe1} + 1) \cdot r_D} \qquad (11)$$

h_{ie}, h_{fe} being parameters of the small-signal common-emitter model, r_D the diode-equivalent resistance and N the number of diodes (In this case, $N = 2$). Now, let us assume the typical identification $h_{fe} \equiv h_{FE}$ and suppose ideal the discrete devices. In this situation, Eq. 11 can be related to the parameters of the bias point:

$$G_M \simeq \frac{I_{OUT,Q}}{V_T \cdot (1 + N)} \qquad (12)$$

$V_T \approx 26\,mV$ at room temperature. The relations among the transient characteristics and $I_{OUT,Q}$, C,... are developed in Section IV-B. On the other hand, the presence of N in Eq. 12 shows a way of decreasing the size of the peaks without making the transient longer. This agrees with previous papers, which reported that adding serial resistors to this configuration make the transients smaller and shorter [7]. Actually, diodes and resistors are alike in small-signal circuits.
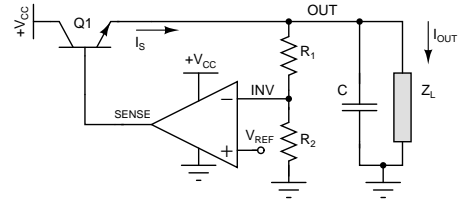

Figure 4. Practical implementation of a voltage regulator using an NPN transistor in common collector mode (Q1). This transistor can be replaced by a Darlington pair or by a discrete NMOS transistor.

2) Linear regulators based on emitter/source followers: Another option is using an output transistor in emitter follower configuration as Fig. 4 shows. This structure, previously studied in the HS-117 voltage regulator [8], will be called *"E/S-F"* in the paper and offers several advantages: First, the system is usually stable even without the output capacitor. Moreover, the transistor can be replaced by an NMOSFET extending this topology to technologies other than bipolar. However, drawbacks are also important: First, the drop-out voltage is higher than in the TLDOR. Also, the structure is too similar to a peak detector. In fact, the first observation of this effect was done in an integrated device with a similar topology. The

Function	Device	Function	Device
NPN	2N2222A	PNP	2N2907A
Darlington NPN	BDX53C	Darlington PNP	BDX54C
NMOS	IRFD014	Diode	1N4148

transconductance in this structure is:

$$G_M = \frac{i_s}{v_{sns}} = \frac{g_m + g_\pi}{1 + r_0 \cdot (g_m + g_\pi)} \qquad (13)$$

r_0 being the the small-signal equivalent device of the load and g_m, g_π the transistor small-signal parameters, either NPN or NMOS transistors. For bipolar transistors, $g_\pi = h_{ie}^{-1}$ and $g_m = h_{fe} \cdot h_{ie}^{-1}$ so:

$$G_M = \frac{h_{fe} + 1}{h_{ie} + r_0 \cdot (h_{fe} + 1)} \approx \frac{1}{r_0} \qquad (14)$$

This equation is also valid for Darlington NPN transistors. In case of using an NMOS transistor, $g_\pi = 0$ so:

$$G_M = \frac{g_m}{1 + r_0 \cdot g_m} > 0 \qquad (15)$$

B. Test set-up

The error amplifier is just an LM124J which has been widely studied in the literature. Additional devices for both configurations are listed in Table I. There were three versions of E/S-F structure, each one with a kind of pass transistor (Q1 in Fig. 4): NPN, Darlington NPN and NMOS. The other structure, TLDOR, made use of two kinds of pass transistors (Q2 in Fig. 3): PNP and Darlington PNP. That means that five kinds of voltage regulators were tested. Finally, $V_{REF} = 1.25\,V$, $R_1 = 10\,k\Omega$, $R_2 = 33\,k\Omega$ so $V_{OUT} = 5.38\,V$ in both circuits.

The load was purely resistive (0.1, 0.47, 1 & 4.7 kΩ,) or a current sink ranging from 0.47 to 21.7 mA. The structure of Fig. 3 was tested with output capacitors from 0.47 to 10 μF while the other one was tested with lower values (0-1 μF). This difference is just a matter of stability. Finally, the only power supply, $+V_{CC}$, was set to 12.1 V.

The LM124J was unpackaged and tested working as voltage regulator at the UCM laser facility ($\lambda = 800\,nm$, $T_{PULSE} = 80\,fs$, $E = 75 - 100\,pJ$, $f = 1\,kHz$) [9]. Such an energetic pulsed laser releases more free charge than typical heavy ions but has the advantage of making the transient quite independent of the random energy fluctuations. Thus, the change in the transient shape can be attributed only to electrical parameters. Besides, as the pulsed laser frequency is 1 kHz, transients longer than 1 ms are not correctly registered since a new laser hit occurs before the previous transient vanishes.

Laser parameters were chosen to induce reallistic single event transients aiming at characterizing electric structures and the hypothetical relation between laser and LET is not sought in this paper. As an example of positive peak, we chose to hit QR1, an open-base NPN transistor in the gain stage, that is well-known for inducing positive transients at the output. Besides, another transistor in the gain stage, Q09, was chosen

to obtain negative transients (Fig. 5). In general, transients induced in this spot are not interesting since the effect is that the pass transistor switches to cutoff state so the current must be provided by the capacitor. The higher the capacitor, the lower the decrease of the output voltage as it is expected from a capacitor discharge.
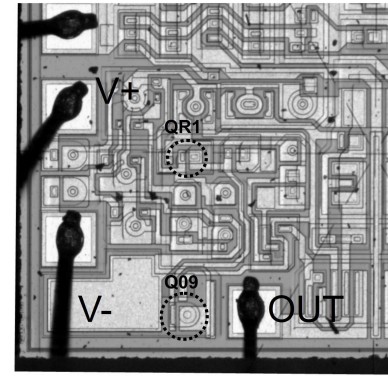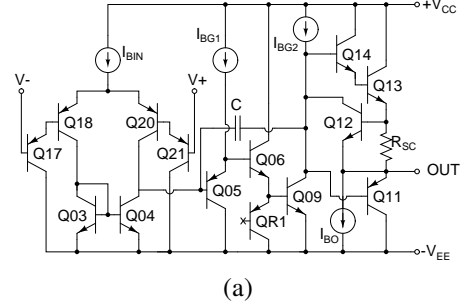

(a)

(b)

Figure 5. LM124A schematics (a) and layout (b). Interesting transistors are highlighted.

IV. RESULTS

Data were taken with a Yokogawa DLM6000 oscilloscope, triggered by a signal coming from the laser, and smoothed with numerical filters to remove quantization noise. This section will focus only on positive transients, where LDPs are liable to occur.

A. Experimental evidence of peak detector effect

First of all, let us demonstrate that peak detector effect actually occurs. Fig. 6 shows the transients in the TLDOR structure. Here, one can see that, after the initial growth of V_{SNS} and V_{OUT}, the op amp output suddenly falls down to 0 V. Only when the regulator output reaches the bias point during the capacitor discharge, the op amp output can return to its stable value, around 2 V. Fig. 7, corresponding to the E/S-F configuration, is even more interesting. This network is stable without output capacitor so one can see the effects of the identical laser hits with and without the capacitor. Thus, an initial transient no longer than 15 μs becomes a 200-μs LDP after including the capacitor.

Another interesting feature deduced from these graphs is the difference between the peak voltage, V_{PK}, and the output
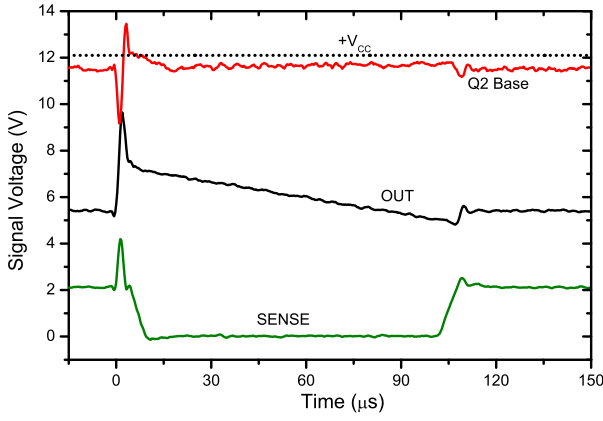
Figure 6. Transients at different nodes in the low-dropout voltage regulator of Fig. 3 after a positive transient. The regulator was built with a 2N2907A pass transistor, a current sink of 22 mA and a 1.0-μF capacitor.
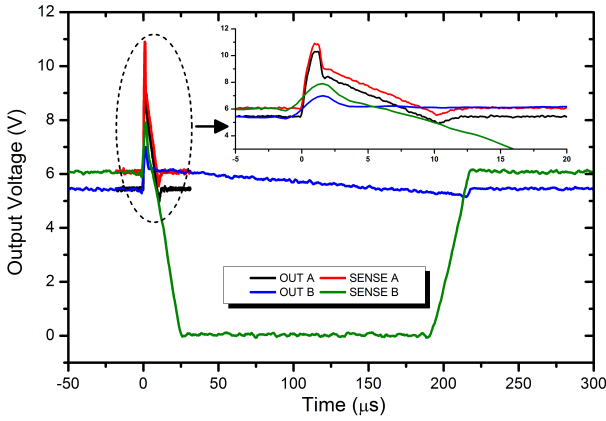

Figure 7. Transients at different nodes in the voltage regulator with emitter follower (2N2222A) after a positive peak. The regulator was biased with a 3.8-mA current sink. In case A, there was a 1-μF output capacitor and no output capacitor in case B.

voltage when the pass transistor is blocked (V_{SW}). Their relative situations are consistent with the initial hypothesis exposed in Section II-C.

B. Characteristics of the transients

In spite of the strong simplification done in Section II-A, the influence of the external parameters is difficult to evaluate. Thus, small capacitors and large values of output current lead to lower values of discharge time. However, this trend is partially compensated by the increasing value of the peak voltage. Therefore, it is not trivial to find out the optimal capacitor value.

1) Duration of transients: According to Eqs. 2-4, the duration of the transients basically depends on external parameters, namely C, R_L^* & I_Q but also on an unpredictable parameter, V_{SW}. This fact leads to a paradox shown in Fig. 8. According to Eq. 2, the transient duration is proportional to the output capacitor value. However, in that graph, one can see that the duration of the transients are in a narrow range (0.75-0.95 ms) even though the output capacitor changed from 1 to 10 μF. The reason was that the value of V_{SW} also depends on this parameter. Therefore, the experimental value of V_{SW}
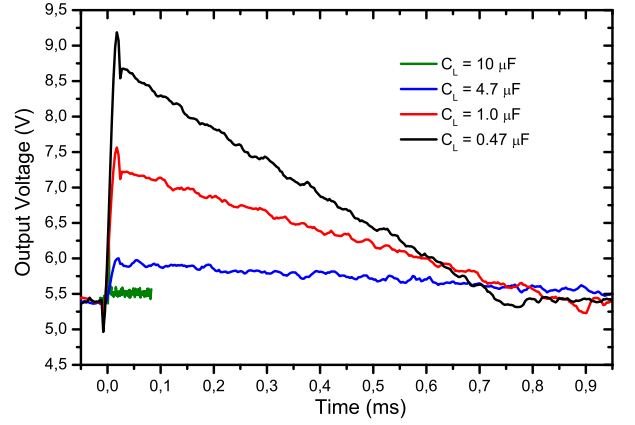

Figure 8. Increase of peak voltage as a function of the output capacitor in the TLDOR with 2N2222A. The load was a current sink of 2.2 mA.

TABLE II
LINEAR FIT PARAMETERS OF THEORETICAL VS. ACTUAL TRANSIENT DURATION.

Structure	a	b (μs)	r
TLDOR - 2N2907A	1.14 ± 0.04	14 ± 31	0.99
E/S-F - 2N2222A	0.89 ± 0.05	3 ± 24	0.97
E/S-F - BDX53C	0.90 ± 0.05	0 ± 25	0.98
E/S-F- IRFD014	0.92 ± 0.07	20 ± 21	0.99

was measured in every transient to be used in calculating the theoretical duration.

Defining the experimental transient duration, T_{AD}, as the first time that the transient reaches the bias point value after the negative peak, we observed that there was a linear relation between T_{AD} and T_{DUR} calculated from Eq. 2. The parameters of the linear regression, $T_{AD} = a \cdot T_{DUR} + b$ are shown in Table II. As expected, experimental values of a are close to 1. In the case of the Darlington pair, there was a pair of integrated resistors between the emitter and the base with a total value of 8.3 kΩ. This value is not negligible so it was incorporated to calculate R_Q in Eq. 2. Besides, in the case of the TLDOR structure with Darlington pair, only the 10-μF capacitor was able to stabilize the output and the transients usually reached the saturation voltage. In consequence, the theoretical duration of the transients was of some milliseconds so no actual transient duration could be included in the table.

2) Peak and switch-off voltages: Fig. 8 accounts for the fact that, as predicted by Eq. 9, the higher the capacitor value, the lower the peak voltage. Eq. 9 predicts that, in the ideal voltage regulator, $(V_{PK} - V_{O,Q}) \propto C^{-1}$. This trend is clearly observed in Fig. 9 since, in fact, experimental values seems to fit a hyperbola. There are some interesting details mainly related to the E/S-F configuration with Darlington pair. First of all, this configuration and that with NMOS transistor shows a maximum with very small values of the output capacitor but not at $C = 0$, against predictions from Eq. 9. Another fact is that, in the E/S-F structure with Darlington pair, the output voltage exceeds the power supply value. However, this excess is about 0.6-0.7 V and, due to the existence of a protection diode connecting the emitter and the collector of the Darlington pair, we believe that the excess is related to the activation of this device during the transient.
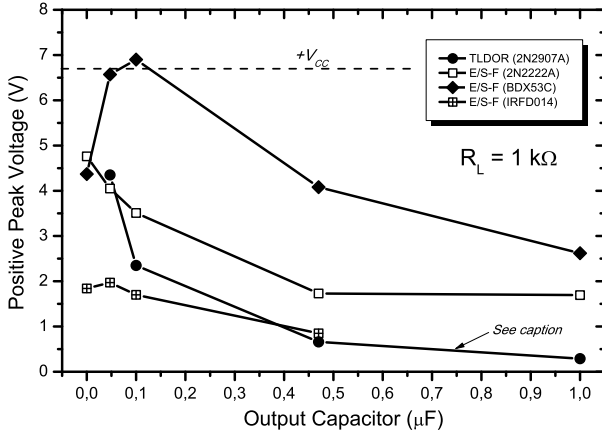
Figure 9. Increase of peak voltage ($V_{PK} - V_{OUT,Q}$) as a function of the output capacitor using a 1-kΩ resistor load. Capacitor values related to the TLDOR with 2N2907A pass transistors are 10 times smaller in the graph so that all the dots could be shown.
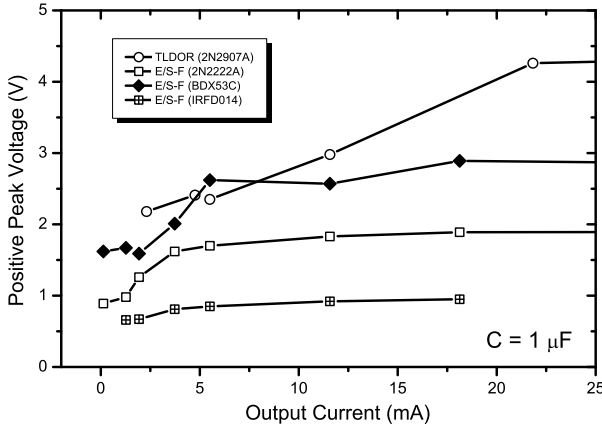

Figure 10. Increase of peak voltage ($V_{PK} - V_{O,Q}$) as a function of the output current using a 1-μF output capacitor. Loads were resistors and current sinks. Lines shows saturation at high values and an extra point at $I_{OUT} = 53.6\ mA$ was omitted to make the graphs clearer.

Concerning the load effects on V_{PK}, one can see that the key parameter is the DC output current. Eq. 12, related to the TLDOR structure, is a clear example but the dependence is also implicit in most versions of Eq. 13. In case of a bipolar pass transistor, this equation becomes $G_M = r_0^{-1}$. If the load is resistive, $r_0^{-1} \approx R_L^{-1} = I_{OUT,Q}/V_{O,Q}$ so $G_M \propto I_{OUT,Q}$. On the other hand, the current sink was built with an active cascode stage in which the output current is proportional to $I_{OUT,Q}$. This also works for the output resistance of the pass transistor $\left(h_{oe}^{-1} \right)$. In consequence, G_M is proportional to I_{OUT} even taking into account the load effects of the feedback network. Finally, Eq. 15 brings identical conclusions if $g_m r_0 >> 1$.

In summary, it is expected that $(V_{PK} - V_{O,Q}) \propto I_{OUT}$. According to the results shown in Fig. 10, positive peaks actually increases as the output current does but the predicted linear relation seems to be valid only with low output current values. This restriction is attributed to effects not included in simple models: Parasitic resistances in the pass transistor, load effects in the original transient, etc. The investigation of the

way that the external devices affect the transients in linear voltage regulators is still in progress [10].

Finally, no clear conclusion could be extracted from the experimental data to determine the value of V_{SW}. This factor depends on T_{SW}, which is not constant since it depends on the bias point of the operational amplifier. The only thing we can say is that the factor $\alpha = (V_{PK} - V_{O,Q})/(V_{SW} - V_{O,Q})$ was between 1.3-1.6 in most cases although it could reach values on the order of 2.5 with high output capacitor values.

V. DISCUSSION

A. Peak detector effect in actual implementations

The peak detector effect is a mechanism that leads to long duration pulses if the excess charge cannot be drained out of the output capacitor. Is this situation liable to occur in real-life systems? Unfortunately, we believe it is. A good example of this situation are logic systems with optional sleep mode. Let us suppose that a voltage regulator such as those of Fig. 3 & 4 biases a microprocessor and other logic CMOS devices and, sometimes, the system is switched off to stand-by in order to save energy. If an ion hits the voltage regulator during this period in such a way that a positive spike occurs, the system will not manage to drain the charge and the overvoltage could seriously damage the CMOS devices.

B. Peak detector effect in other linear voltage regulators

Long duration transients due to peak detector effect were observed and characterized in previous sections. However, when LDPs should be expected? Now, we will discuss some configurations and examine if they are liable to exhibit this kind of transient. Data came from the laser facility but other results were obtained from SPICE simulations.
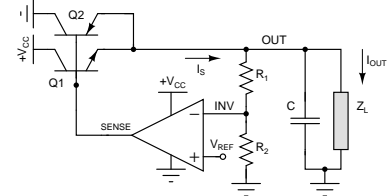

Figure 11. Modification of the emitter-follower voltage regulator with an extra PNP transistor.

1) Class B emitter follower: This structure is derived from the original class-A emitter follower configuration (Fig. 4) adding another transistor (Fig. 11). Thus, the original class-A output stage becomes class-B. In this situation, the controlled current source $I_S(V_{SNS})$ is:

$$I_S = I_{S1} \cdot \exp\left(\frac{\Delta V}{V_T}\right) - I_{S2} \cdot \exp\left(\frac{\Delta V}{V_T}\right) \qquad (16)$$

ΔV being $V_{SNS} - V_{OUT}$ and I_{SX} a DC transistor parameter, not to be confused with the current source, I_S. This function, $I_S = f(\Delta V)$, is increasing so the feedback loop is closed by the inverting input but unlike the current source in Fig. 1 is *positive for $\Delta V > 0$ and negative for $\Delta V < 0$*. Therefore, it does not accomplish the mathematical conditions to trigger
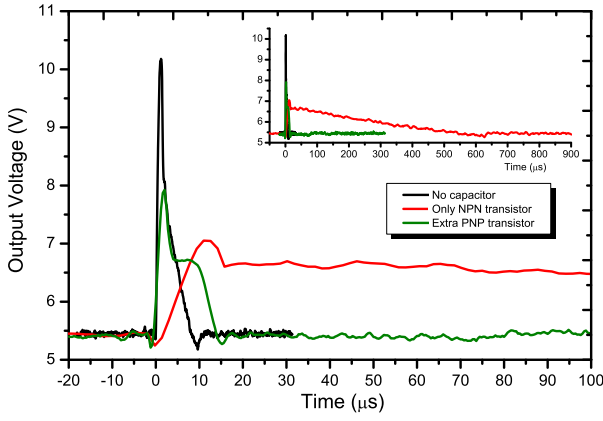
Figure 12. Mitigation of LDPs in the E/S-F structure with 2N2222A by means of an additional PNP transistor (2N2907A). The inset shows the LDP until the end of the transient. $R_L = 4.7\,k\Omega$, $C = 1\,\mu F$.
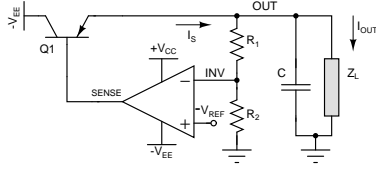

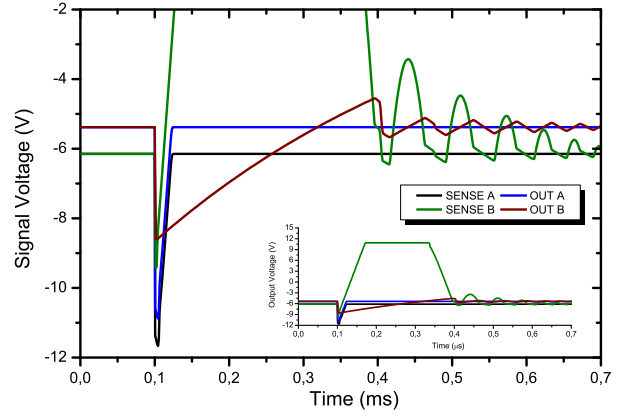Figure 13. Negative emitter-follower voltage regulator.

Figure 14. SPICE simulation of transients in a negative E/S-F with 2N2907A, without capacitor (A) and with it (B). The inset shows full-range transients. $R_L = 1\,k\Omega$, $C = 0.47\,\mu F$.
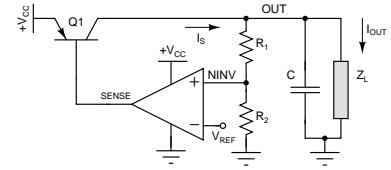

Figure 15. Positive voltage regulator with simple PNP.

peak detector effect: To be a strictly positive or negative function. Another simple way to understand this behavior is the following: If the op amp output falls to negative saturation, the PNP transistor, in cut-off state during normal operation, switches on and the capacitor be quickly drained. Fig. 12 shows the effects of placing this transistor. In this graph, the original transient after hitting QR1 without an output capacitor is painted in black. The addition of the output capacitor (red) dramatically transforms the original transient into an smaller but much longer pulse. Finally, a PNP transistor makes the LDP duration on the order of that of the original transient (green).

2) Negative emitter-follower regulators: Let us look for a structure similar to Fig. 4 but with negative output voltage and working as a sink. To achieve this goal, the reference voltage is negative and the pass NPN transistor must be replaced by a PNP one (Fig. 13). In this situation:

$$I_S = -I_{S1} \cdot \exp\left(\frac{V_{OUT} - V_{SNS}}{V_T}\right) \quad (17)$$

This function is negative-definite but increasing since:

$$G_M = \frac{\partial I_S}{\partial V_{SNS}} = \frac{I_{S1}}{V_T} \cdot \exp\left(\frac{V_{OUT} - V_{SNS}}{V_T}\right) > 0 \quad (18)$$

Therefore, it is suitable for the diagram in Fig. 1. The only modification is that, as $I_S < 0$, the peak detector effect will occur *after a negative transient*. Transient simulations were run with a LM124 SPICE micromodel [9] working in this configuration and injecting a current pulse into Q09 base (Fig. 14). As expected, an LDP occurs.

3) Positive regulator with simple PNP: Fig. 15 shows a well-known structure to build positive linear voltage regulators

[2], [7], [10]. In this structure, the output current is calculated from V_{SNS} following:

$$I_S = I_{S1} \cdot \exp\left(\frac{V_{CC} - V_{SNS}}{V_T}\right) \quad (19)$$

so the current gain is:

$$G_M = \frac{\partial I_S}{\partial V_{SNS}} = -\frac{I_{S1}}{V_T} \cdot \exp\left(\frac{V_{CC} - V_{SNS}}{V_T}\right) = \quad$$

$$= -\frac{I_{OUT,Q}}{V_T} \quad (20)$$

that is always negative. This is why the feedback loop is closed at the non-inverting op amp input. Finally, if V_{SNS} is high enough, $Q1$ goes to cutoff state so $I_S = 0$. In summary, this structure fits the simmetric version of Fig. 1, with negative transconductance. SPICE simulations, not included in the paper for length considerations, account for this prediction. Besides, the shape of some transients shown in recent papers [10] shares striking details with those reported in the present work.
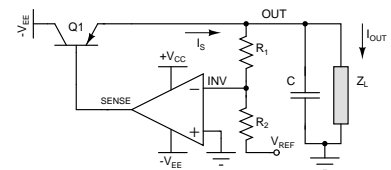

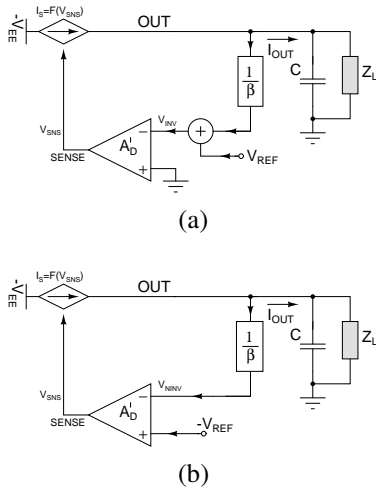Figure 16. Negative voltage regulator with inverter feedback network.

(a)

(b)

Figure 17. Block diagram for a linear regulator built from an inverter (a) and equivalent diagram after reworking the equations (b). $\beta = R_1/R_2$ and $A_D' = A_D \cdot \frac{\beta}{\beta+1}$, A_D being the op amp open loop gain.
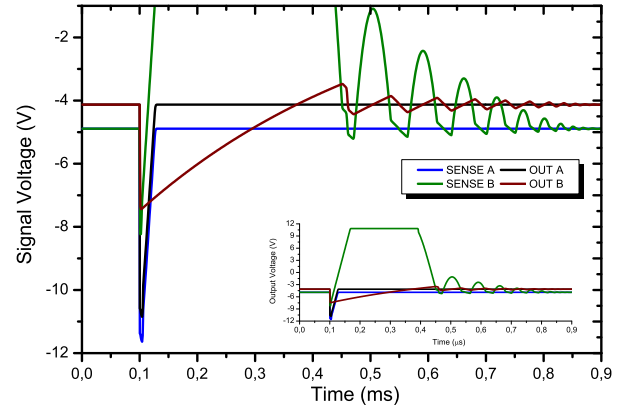

Figure 18. SPICE simulation of transients in an inverter configuration with 2N2907A, without (A) and with capacitor (B). The inset shows full-range transients. $V_{REF} = 1.25\ V$, $R_1 = 33\ k\Omega$, $R_2 = 10\ k\Omega$ $R_L = 1\ k\Omega$, $C = 0.47\ \mu F$.

4) Negative regulators with inverting feedback network: In this case, the regulator is built with a positive voltage reference to create a negative one (Fig. 16). After a fast inspection, it is easy to conclude that $V_{O,Q} = -\frac{R_1}{R_2} \cdot V_{REF}$ and that the output current flows through Q1, the PNP pass transistor.

The equations controlling the evolution of the node voltages are:

$$I_{OUT} \simeq I_S = -I_{S1} \cdot \exp\left(\frac{V_{OUT}-V_{SNS}}{V_T}\right)$$
$$V_{SNS} = -A_D \cdot V_{INV}$$
$$V_{INV} = \frac{R_1}{R_1+R_2} \cdot \left(\frac{R_2}{R_1} \cdot V_{OUT} + V_{REF}\right)$$
$$V_{OUT} = Z_L\left(I_S\right)$$

This set of equations can be used to build a feedback block diagram after discussing the nature of I_S. This current source depends on $\Delta V = V_{OUT} - V_{SNS}$ but V_{OUT} implicitly depends on V_{SNS}. Therefore, I_S can be expressed somehow as $F\left(V_{SNS}\right)$. As Q1 is a PNP emitter-follower, Eq. 14 is valid so I_S can be estimated as $I_S(V_{SNS}) = I_{S,Q} + (V_{SNS} - V_{SNS,Q})/r_0$, it is increasing but negative definite. Then, a block diagram can be built (Fig. 17a), apparently being different from that of Fig. 1. However, this block can be reworked to obtain another version that provides the same set of equations but with an interesting feature: It is identical to the regulator of Fig. 13 and, in consequence, sensitive to peak detector effect, as SPICE simulations show (Fig. 18).

VI. CONCLUSION

The peak detector effect has been generalized for a wider range of linear voltage regulators than that predicted by the discoverers and observed in typical low dropout voltage regulators built with discrete devices. In general, the voltage peak is higher as the bias output current grows and the output capacitor decreases. However, the observed trend is that this evolution also helps the transients to be shorter. An electronic designer must be aware of both trends to determine the less risky situations in which the networks can be involved and, this way, to make a correct selection of the output capacitor.

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