Pentacene based Thin Film Transistors with High-k Dielectric Nd_2O_3 as a Gate Insulator

R. Sarma
Thin Film Laboratory, Department of Physics, J B College, Jorhat, Assam, India

D. Saikia
Thin Film Laboratory, Department of Physics, J B College, Jorhat, Assam, India and Dibrugarh University, Dibrugarh, Assam, India

Puja Saikia,* P.K.Saikia, and B.Baishya
Dibrugarh University, Dibrugarh, Assam, India
(Received on 19 June, 2010)

We have investigated the pentacene based Organic Thin Film Transistors (OTFTs) with High-k Dielectric Nd_2O_3. Use of high dielectric constant (high-k) gate insulator Nd_2O_3 reduces the threshold voltage and sub threshold swing of the OTFTs. The calculated threshold voltage -2.2V and sub-threshold swing 1V/decade, current ON-OFF ratio is 1.7×10^4 and mobility is 0.13cm^2/V.s. Pentacene film is deposited on Nd_2O_3 surface using two step deposition method. Deposited pentacene film is found poly crystalline in nature.

Keywords: Pentacene, Organic Thin Film Transistors, Low Threshold voltage, Rare earth oxide Nd_2O_3, Two Step Deposition.

1. INTRODUCTION:

Organic Thin Film Transistors(OTFTs) have received considerable attention from the standpoint of developing low-cost or large-area electronics applications like electronic paper displays, flexible sensors, and disposable radio frequency identification tags [1]. In recent years, many studies have been devoted to improving the characteristics of organic thin-film transistors (OTFTs) [2]. Pentacene organic semiconductors have become one of the most promising materials for future thin, light, and flexible display applications. However, there are many problems still unresolved such as low mobility, high driving voltages, etc. There have been many investigations for improving mobility and other performances of OTFTs. The performance of the OTFTS can be improved by proper selection of Gate dielectric material and metal electrodes (metals which can give good ohmic contact) [3]. Most successful gate dielectric for pentacene based OTFTs is thermally grown silicon dioxide but the operating voltage of these silicon dioxide insulated OTFTs is large, above 20 V. For portable applications, especially for radio frequency identification devices requiring low power consumption, it is necessary to reduce the operating voltage to below 5 V. The key to low voltage operation is reduction of threshold voltage and sub threshold swing. The use of a high dielectric-constant (k) gate dielectric lowering the operation voltage of TFTs is one of the main technical trends [4,5]. Therefore researchers all over the world worked on the way to reduce operating voltage of pentacene based OTFTs using various high dielectric constant insulators Al_2O_3 [4], $HfLaO$ [5,6], $HfSiO_x$ [7], Pr_6O_{11} [8], La_2O_3 [9] etc. However, though the dielectric capacitance and strength of the gate dielectric are incredibly important properties, the surface characteristics of the gate dielectric can also play a vital role. High dielectric-constant (k) gate dielectric are characterized by a relatively rough surface morphology upon deposition in a vacuum chamber. The rough surfaces result in an inferior channel/dielectric interface along with poor crystalline growth of the pentacene channel, and thus OTFTs fabricated on such dielectric surfaces usually exhibit undesirable device characteristics with low current ON-OFF ratio. Very thin or high-k gate dielectrics generally may bring about high leakage current and low dielectric strength in the utilization of OTFTs.

The rare earth oxides (Nd_2O_3), Er_2O_3, Pr_2O_3,ZrO_2 etc., are reported with very high dielectric constant and low leakage current reliable for gate dielectrics in microelectronics [10,11]. One of us Baishya [12] study the suitability of rare earth oxides in thin film transistors. One of the above neodymium oxide (Nd_2O_3) as high-k gate dielectric has been under intense investigation recently for replacing conventional SiO_2 due to its high dielectric constant and low leakage current. The properties of grown film and interface show a pronounced dependence upon the deposition process and the precise deposition parameters. Many techniques such as chemical vapor deposition, atomic layer deposition, sol-gel techniques, electron beam deposition etc. are used to deposit thin films on the aforementioned rare earth oxides. Each technique has their own set of advantages and disadvantages. However, most of these techniques show some or other kind of interface damage [13]. Sputtering and e-beam assisted depositions create radiation induced surface damage during film growth. Thermal evaporation is a well known technique that does not produce any kind of surface damage [13,14]. Because this technique is a rather gentle process it creates very little or no damage to the interface [13].

Inorganic TFTs with thermally evaporated Nd_2O_3 oxide insulating layer reported successfully from this laboratory [15,16]. Structure and Electrical Properties of Thermally Evaporated Nd_2O_3 thin films was studied by Kannan et al. [17,18] and reported that the thermally deposited films thickness bellow 2650$\AA$ shows well amorphous structure. Amorphous dielectric films are usually insensitive to impurities and [7,19] and more stable owing to the absence of grain boundaries hence suitable for gate insulator.

Further in this work we use two-step-deposition technique [20,21] to improve the film quality of semiconduc-

*Electronic address: puja.saik@gmail.com

tor layer over Nd_2O_3 dielectric surface. The two-step-deposition (TSD) technique, based on controlling deposition rate (DR) [22,23]. This technique enables us to control the channel conductivity in the depletion and accumulation regime as well as to improve the film continuity [20,21]. The substrate temperature is kept at 27^0C during deposition because it is found that [24] at that temperature best poly crystalline thin films of pentacene can be grown.

The performance of the OTFT also depends on the contact electrode [25]. We have [8,9,26] already studied pentacene and tetracene based OTFTs using Al contact electrode and it is found that that best result cannot be obtained with Al-source drain electrode. As a source/drain (S/D) electrode, currently, gold has been mainly used as a contact metal in pentacene based OTFTs because gold has a work function of 5.1 eV, which is close to the highest occupied molecular orbital(HOMO) level of pentacene (5.0 eV). As a result hole injection barrier is low so that carriers can move easily in each direction between electrode and pentacene. Therefore in this work we use Au as source drain contact electrode.

2. EXPERIMENTAL DETAILS

OTFTs were fabricated in staggered electrode structures by a series of vacuum evaporations using suitable masks. The order of the deposition is shown in Fig. 1. In the fabrication process first Al-gate electrodes of thickness 1010$\AA$ is deposited over ultrasonically cleaned (with acetone, ethanol and de-ionized water) glass substrate, above which a layer of Nd_2O_3 of thickness 650$\AA$ is deposited. The oxide was properly degassed in vacuum for a long time prior to deposition. Following the oxide layer a layer of pentacene (Aldrich of 99.9%purity), thickness 380$\AA$ is deposited using the two-step deposition method. First monolayer of 120$\AA$ was growth using 0.5 $\AA$/s deposition rate and the next layer of thickness 260$\AA$ deposited with the rate 0.1 $\AA$/s. Finally the source drain electrodes of Au (thickness 1430$\AA$) are deposited using shadow mask having a channel of length 50μm and width 0.14 cm. All the depositions are done at room temperature (27^0C) and at a vacuum better than 5×10^{-6} torr using thermal evaporation method. The experimental arrangement to study the electrical properties of the OTFTs is shown in figure 2.

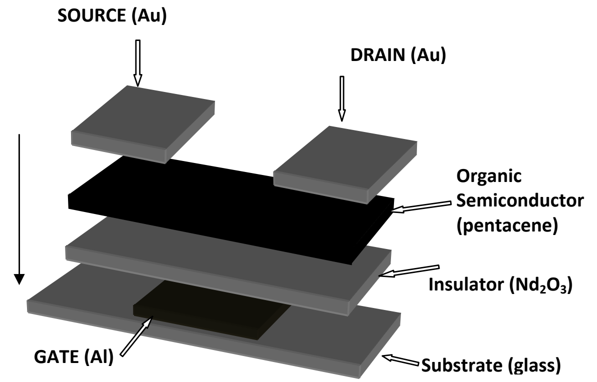

FIG. 1: Deposition order of the OTFT.

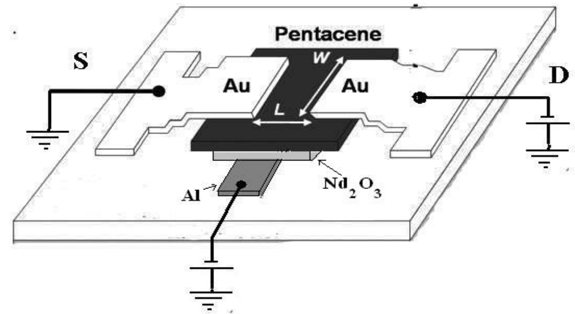

FIG. 2: Experimental arrangement.

3. RESULTS AND DISCUSSION

Drain current I_D versus drain voltage V_D at various V_G are plotted in Figure 3, The graphs established that the OTFTs operate in the accumulation mode and Pentacene is p-type semiconductor. In saturation region $V_D = V_G - V_T$; drain current is given by Eq. 1 [3] -

$$I_{Dsat} = \frac{w}{2L}\mu c_i (V_G - V_T)^2 \tag{1}$$

where w is the channel width, L is channel length, c_i is the capacitance per unit area of the gate insulator, V_T is the threshold voltage and μ is the mobility.

Plot of $(I_{Dsat})^{1/2}$ versus V_G is shown in the Figure 4. The field effect mobility μ is calculated from the slope of this plot. The threshold voltage V_T is estimated by the extrapolation of the linear portion of the graph to the V_G axis [3]. Plot of Log (I_D) versus V_G at a constant drain voltage(-15V) is shown in the Figure 5. The sub-threshold swing is calculated from the

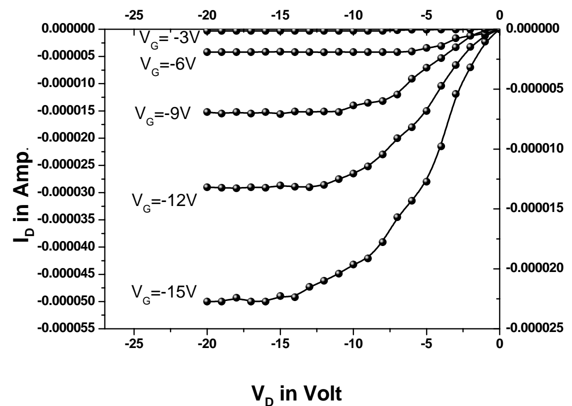

FIG. 3: Variation I_D *vs* V_D at various Gate voltages

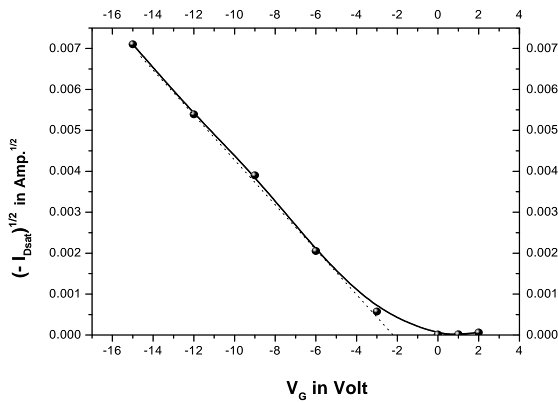

FIG. 4: Plot of $(-I_{Dsat})^{1/2}$ versus V_G

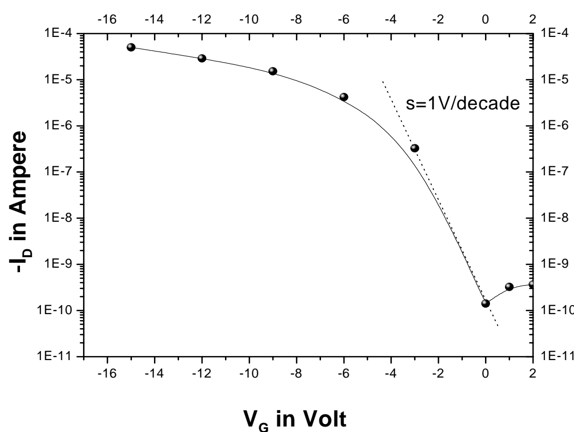

FIG. 5: $Log_{10}(I_D)$ $vs.$ V_G plot at $VD = -15V$.

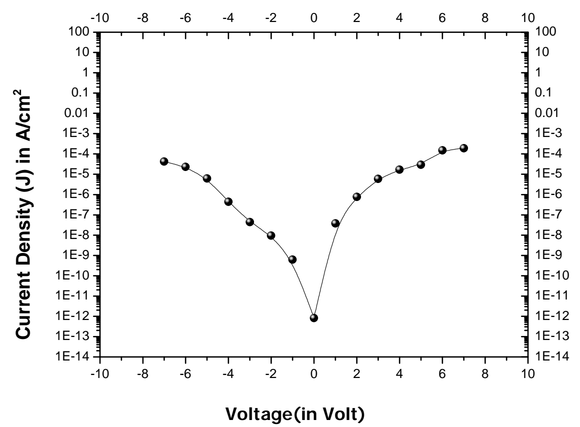

FIG. 6: $J-V$ characteristics.

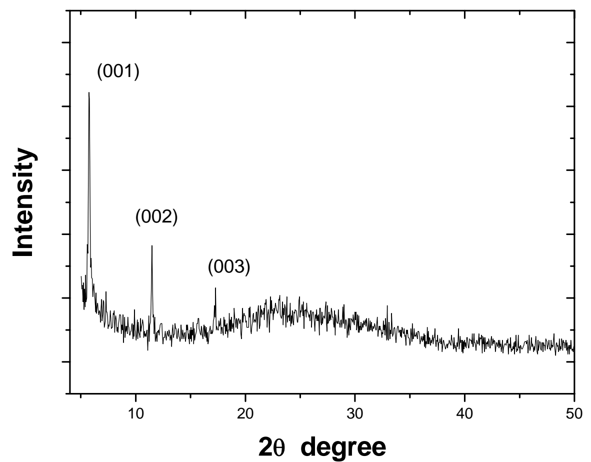

FIG. 7: XRD of the pentacene film deposited on Nd_2O_3.

slope of this graph using the relation (2) [27]-

$$s = \left(\frac{\delta(\log I_D)}{\delta V_G}\right)^{-1} \quad (2)$$

The current ON-OFF ratio is estimated from the relation (3) [3]

$$\frac{I_{ON}}{I_{OFF}} = \frac{c_i \mu (V_G - V_T)^2}{\sigma d V_D} \quad (3)$$

The J-V characteristics of the dielectric film in $Al/Nd_2O_3/Au$ configuration is shown in the figure 6. The films shows very low leakage current and hence suitable for OTFTs. In Figure 7 the XRD pattern of the pentacene film deposited over Nd_2O_3 is shown. The observed diffraction peaks established that thin films of Pentacene grown over Nd_2O_3 by two step deposition method at 27^0C is poly crystalline in nature and consist of only thin film phase. The various parameters used and evaluated in this work are tabulated in table 1. In table 2 a comparative study with the previous works is done. From the comparative study it is clear that Nd_2O_3 will be better insulator for low voltage pentacene based OTFTs. Though the mobility of the OTFTs with SiO_2 insulator is a little better, the threshold voltage is considerably less in our case.

TABLE 1: The various parameter used and evaluated are shown in the Table bellow.

Channel width(w)	0.14 cm
Channel length(L)	0.005 cm
Capacitance per unit area (c_i)	0.0016 F/m^2
Channel thickness(d)	380A^0
Threshold voltage(V_T)	-2.2V
Channel Mobility(μ)	0.13 cm^2/V.s
Sub threshold swing(s)	1V/decade
ON-OFF ratio	1.7 x10^4

TABLE 2: Comparison of present work with previous works.

Oxide	Mobility ($cm^2/V.s$)	ON-OFF ratio	Threshold voltage (in Volt)	Year	
SiO_2	0.182	$2.8x10^4$	−8.75	2005	ref. 25
HfSiOx	0.02	$2.6x10^3$	-3	2008	ref.7
Nd_2O_3	0.13	$1.7x10^4$	-2.2	2010	This work

low threshold voltage OTFTs have been reported but in those works complicated fabrication techniques some times more than one fabrication technique and insulating layers are used. In this work we use traditional fabrication technique which is widely applied in commercial fabrications of TFTs, now a days. The comparative study in the table 2 established the superiority of the present work over the others. Using this method fabrication of low cost OTFT will become possible so that the traditional Si-TFTs can be replaced.

4. CONCLUSIONS

Using two step deposition on Nd_2O_3 dielectric we fabricate low threshold voltage OTFTs. The threshold voltage and sub threshold swing of the OTFTs are low enough so that they can be used in portable devices. Numbers of works on low threshold voltage OTFTs have been reported but in those works complicated fabrication techniques some times more than one fabrication technique and insulating layers are used.

Acknowledgement

The authors R. Sarma and D. Saikia are thankful to University Grant Commission, New Delhi, India for financial support under major research project program Grant No.: 34-20/2008 (SR). Special thanks to Google Research Help Group.

[1] Howard E. Katz and Jia Huang, *Annu. Rev. Mater. Res.* **39,** 71 (2009).
[2] M.J. Malachowski and J. Żmija, *Opto Electron. Rev.*, **18**(2), 121 (2010).
[3] B.C. Shekar, Jiyeon Lee and Shi-Woo Rhee, *Korean J Of Che. Eng,* **21** (1) 267(2004).
[4] Xiao-Hong Zhang, Benoit Domercq et al., *Organic Electronics* **8**, 718 (2007).
[5] M.F. Chang, P.T. Lee, S.P. McAlister, and Albert Chin, *IEEE Electron Device Lett,* **30** (2), 133, (2009).
[6] M.F. Chang, P.T. Lee, S.P. McAlister, and Albert Chin, *IEEE Electron Device Lett.* **29**(3), 215(2008).
[7] Hu Yan, Tsubasa Kagata, Susumu Arima, Hiroshi Sato, and Hidenori Okuzaki, *phys stat sol (a),* **205** (12), 2970(2008).
[8] R. Sarma, D. Saikia, and B. Barua , Organic Thin Film Transistor with Pr_6O_{11} dielectric layer (pp- 42), *In*: Indo-Russian Workshop on Nanotechnology and Laser Induced Plasma Proceedings (IRNANO-**2009**).
[9] R. Sarma and D. Saikia, K. Konwar and B. Baishya , *Indian J. Phys.* **84** (**5**), 547 (2010).
[10] Markku Leskela and Mikko Ritala, *Journal of Solid State Chemistry* **171**, 170 (2003).
[11] Markku Leskela, Kaupo Kukli and Mikko Ritala, *Journal of Alloys and Compounds,* **418,** 27(2006).
[12] P. Singh, B. Baishya , physica status solidi (a), **104,** 885 (1987).
[13] M. Bhaskaran, P.K. Swain and D. Misra, *Electrochemical and Solid-State Letters*. 7 (6), F38 (2004).
[14] R. Garg, D. Misra and P.K. Swain **,** *J. Electrochem Soc.* **153** (2), F29 (2006).
[15] P. Singh, B. Baishya *Thin Solid Films,* **147,**25(1987).
[16] P. Singh, B. Baishya *Thin Solid Films,* **141**,179(1986).
[17] M.D. Kannan, S.K. Narayandass, C. Balasubramanian and D. Magalaraj, *phys stat sol (a),* **128**, 427(1991).
[18] M.D. Kannan, S.K. Narayandass, C. Balasubramanian and D. Magalaraj, *phy stat sol (a),* **121**,515 (1990).
[19] N.F. Mott, *Adv Phy,* **16,** 49 (1967).
[20] Sung Hun Jin, Cheon An Lee et al., *IEEE Elect. Dev. Lett.* **26** (12), 903(2005).
[21] Tossapol Tippo1, Chanchana Thanachayanont et al. *Journal of Microscopy Society of Thailand,* **23**(1), 130(2009)
[22] R. Ruiz, D. Choudhary, B. Nickel et al. *Chem. Mater,* 16 (23), 4497(2004).
[23] Frank-J. Meyer zu Heringdorf, M.C. Reuter & R.M. Tromp, *Nature*, **412**, 517 (2001).
[24] C.D. Dimitrakopoulos and D.J. Mascaro , *IBM J. Res. & Dev.* **45** (**1**), 11(2001).
[25] Chih-Wei Chu, Sheng-Han Li, Chieh-Wei Chen, Vishal Shrotriya, and Yang Yanga, *Appl. Phys. Lett.* **87**, 193508 (2005)
[26] R. Sarma and D. Saikia, *Indian J Pure & Appl Phys,* **47**,876 (2009)
[27] Jung Hoon Seo, Jae-Hong *et al. Semicond. Sci. Technol.* **22,** 1039 (2007).
[28] A. Rollend, J. Richard *et al.*, *J of Electrochem Soc,* **140**, 3679(1993)