Fast Organic Thin-Film Transistor Circuits

Hagen Klauk, *Student Member, IEEE,* David J. Gundlach, *Student Member, IEEE,* and Thomas N. Jackson, *Member, IEEE*

***Abstract*—We have fabricated organic thin-film transistors and integrated circuits using pentacene as the active material. Devices were fabricated on glass substrates using low-temperature ion-beam sputtered silicon dioxide as the gate dielectric and a double-layer photoresist process to isolate devices. These transistors have carrier mobility near 0.5 cm^2/V-s and on/off current ratio larger than 10^7. Using a level-shifting design that allows circuits to operate over a wide range of threshold voltages, we have fabricated ring oscillators with propagation delay below 75 μs per stage, limited by the level-shifting circuitry. When driven directly, inverters without level shifting show submicrosecond rise and fall time constants.**

I. Introduction

THIN-FILM TRANSISTORS (TFT's) using organic semiconductors as the active material have made impressive progress over the last ten years, and it appears increasingly likely that organic TFT's will find application, not only as pixel access elements in low-cost active matrix displays [1]–[3], but also to integrate logic circuitry and memory arrays into low-cost electronic products such as smart cards, smart price and inventory tags, and large-area sensor arrays [4], [5].

Organic TFT's based on vacuum-deposited films of the fused-ring aromatic hydrocarbon pentacene have previously shown electrical characteristics comparable to those obtained with hydrogenated amorphous silicon devices, including field effect mobility as large as 1.5 cm^2/V-s and on/off current ratio larger than 10^8 [6]. For simplicity, these early devices were fabricated on single-crystal silicon wafers. To allow integrated TFT circuits on glass or plastic, we have developed a device process using selective metal gates and a low-temperature (80 °C), ion-beam sputtered silicon dioxide gate dielectric [7]. Using this process and a level-shifting circuit design, we have fabricated all-organic ring oscillators with minimum propagation delay below 75 μs per stage. These are the fastest organic TFT circuits reported to date.

II. Device Structure and Fabrication Process

All transistors and circuits were fabricated on borosilicate glass (Corning 7059) substrates using the device structure shown in Fig. 1. Gate metal, gate dielectric, and source/drain contacts were deposited by ion-beam sputtering and patterned by photolithography and lift-off. Pentacene was purchased from commercial sources, purified by temperature-gradient vacuum sublimation, and thermally evaporated to form the active TFT layer. During the pentacene deposition, the substrate was held at 60 °C to improve molecular ordering [8]. Transistors fabricated as described typically have carrier field-effect mobility near 0.5 cm^2/V-s, on/off current ratio larger than 10^7, and subthreshold slope around 1 V/decade.

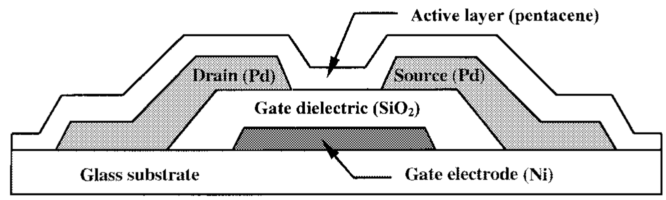

Fig. 1. Schematic cross section of a pentacene TFT on a glass substrate.

Although bulk pentacene is an excellent insulator with resistivity near 10^{14} Ω-cm, our pentacene TFT's often have positive threshold voltage, indicating that a carrier channel is present in the pentacene, even with no gate field applied, and a positive gate voltage is necessary to deplete the channel. Wiring pentacene TFT's in a circuit without introducing unacceptable current leakage therefore requires that the active TFT areas be isolated. Patterning of the active layer is problematic, however, since TFT characteristics tend to degrade significantly when the organic film is exposed to solvents such as those commonly used in photolithographic processes.

To address the leakage problem, we have applied an active-layer patterning technique that does not require the organic film to be exposed to process chemicals. Before the pentacene layer is deposited, the substrate is coated with a layer of polymethylmethacrylate (PMMA), followed by a layer of novolac-based photoresist. Near-UV exposure through a mask is used to define the active areas in the novolac layer. The pattern is then transferred to the PMMA layer using a flood deep-UV exposure during which the novolac layer acts as a conformable mask. Finally, the PMMA is developed in toluene to open the active device areas. By optimizing the exposure and development process for both layers, a reentrant double-layer profile is created [9]. When the pentacene is deposited, the active layer breaks along the resist edges to leave isolated device areas and eliminate current leakage in the pentacene film outside the active device areas.

III. Pentacene Integrated Circuits

By integrating two transistors in a circuit configuration such that one of them is acting as a voltage-controlled switch (or driver) and the other as an active load, a simple voltage inverter can be made. However, since our pentacene TFT's often have

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The authors are with the Center for Thin Film Devices, and the Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, Pennsylvania State University, University Park, PA 16802 USA (e-mail: Hagen@jerg.ee.psu.edu).

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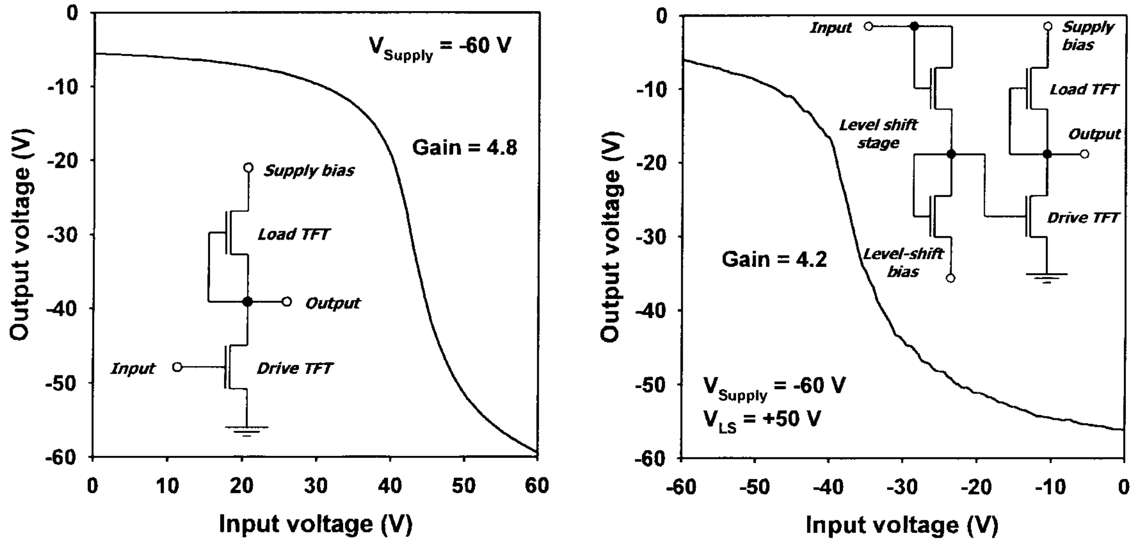

(a) (b)

Fig. 2. Schematic diagrams and voltage transfer characteristics of pentacene inverters (a) without level shifting and (b) with integrated level-shift stage. The inverters have a driver gate length of 5 μm, a driver gate width of 800 μm, a load gate length of 30 μm, and a load gate width of 300 μm. The inverter supply bias is -60 V, and the level-shift bias V_{LS} in Fig. 2(b) is $+50$ V.

positive threshold voltage, a simple enhancement-mode circuit layout will typically not yield useful inverter operation. This is demonstrated in Fig. 2(a), which shows the schematic diagram and the voltage transfer characteristics of a pentacene inverter based on an enhancement-mode layout, but using TFT's with threshold voltage near $+30$ V. The circuit shows usefully large voltage gain, but the input and output levels are not compatible due to the positive threshold voltage of the drive TFT.

To adjust the logic levels so that they correspond properly to the on- and off-states of the drive TFT, we have integrated a level-shift stage with each logic gate. The level-shift stage requires two additional TFT's, which act as saturated loads in a voltage divider configuration. An additional power supply (the level-shift bias) is used to adjust the output of the level-shift stage, thus allowing inverter operation over a wide range of threshold and supply voltages. The schematic diagram and the voltage transfer characteristics of a depletion-mode inverter circuit with integrated level-shift stage are shown in Fig. 2(b). Large voltage gain is obtained, and the input and output levels are compatible. The increased noise in the transfer characteristics is a result of the low current level selected for the level-shift stage design.

Using inverters with integrated level-shift stage we have fabricated 5- and 7-stage ring oscillators. These circuits function over a wide range of supply and level-shift voltages. Fig. 3 shows the output signal of a 5-stage pentacene ring oscillator with output buffer operating with a supply bias of -80 V and a level-shift bias of $+50$ V. Fig. 4 shows how the propagation delay per stage changes as a function of supply voltage for the 5-stage pentacene ring oscillators. For each supply voltage, the level-shift bias is adjusted for best performance. As expected, the propagation delay decreases with increasing supply voltage, and a minimum propagation delay of 73 μs per stage is obtained. To our knowledge, this

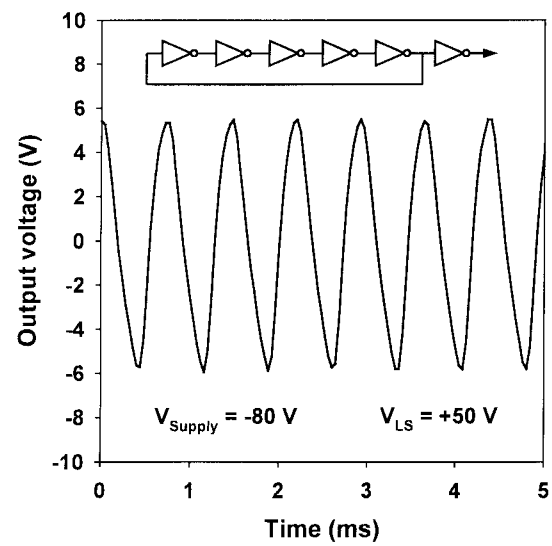

Fig. 3 Schematic diagram and output signal of a 5-stage pentacene ring oscillator with output buffer at a supply bias of -80 V and a level-shift bias of $+50$ V.

result is the fastest switching speed reported for all-organic circuits and is about five times faster than the previous best result [10].

The propagation delay in our pentacene ring oscillators is not limited by the intrinsic inverter speed, but by the low current level chosen for the level-shift stage. To estimate the intrinsic inverter speed, we have used a pulse generator to directly drive a pentacene inverter with no level-shift stage. Fig. 5 shows the response of a pentacene inverter driven without level shifting at 200 kHz. The rise and fall time constants—extracted from the inverter output by fitting exponential functions to the output waveform—are 0.5 and

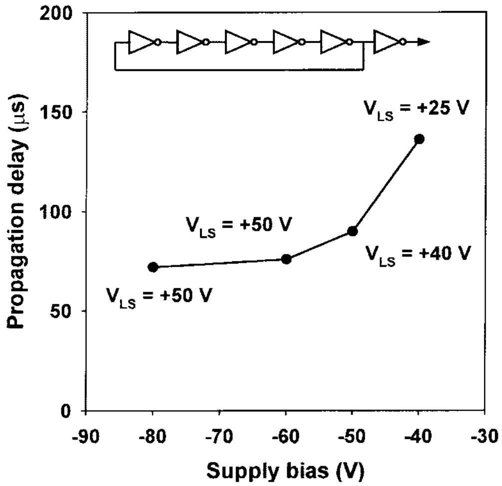

Fig. 4. Schematic diagram and propagation delay per stage as a function of supply bias of a 5-stage pentacene ring oscillator with output buffer (level-shift bias V_{LS} adjusted for best performance).

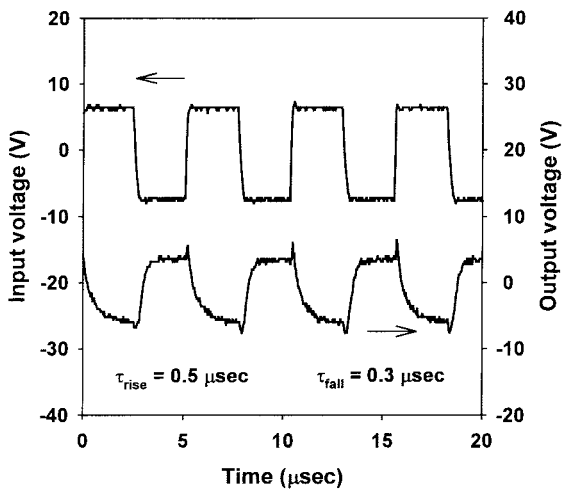

Fig. 5. Input and output signals of a pentacene inverter without level shifting directly driven at 200 kHz.

0.3 μs, respectively. In this measurement the inverter output voltage is driven over a relatively small range, and it is not simple to extrapolate to an intrinsic inverter propagation delay. However, we have recently fabricated integrated inorganic/organic complementary circuits using hydrogenated amorphous silicon n-channel devices and pentacene p-channel devices [11]. These circuits have propagation delay as low as 5 μs per stage, measured using ring oscillators, which also indicates that circuits using organic TFT's can be quite fast.

IV. Conclusion

We have demonstrated integrated circuits based on pentacene organic TFT's. Devices were fabricated on glass substrates using low-temperature ion-beam sputtered silicon dioxide as the gate dielectric. Using a level-shifting circuit design to allow circuit operation with depletion-mode TFT's and applying a simple technique to pattern the organic active layer, we have demonstrated pentacene inverters with large voltage gain and ring oscillators with sub-75-μs propagation delay, limited by the level-shifting circuitry. When driven directly, pentacene inverters show sub-microsecond rise and fall time constants.

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