Pentacene thin film transistors with a poly(methyl methacrylate) gate dielectric: Optimization of device performance

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The electrical characteristics of pentacene-based organic thin film transistors (OTFTs) using poly(methyl methacrylate) (PMMA) as the gate dielectric are reported. Uniform pinhole-free and crack-free films of PMMA could be obtained by spin coating, with a lower limit of thickness of about 150 nm. The effects of the insulator thickness and channel dimensions on the performance of the devices have been investigated. Leakage currents, which are present in many polymeric gate dielectrics, were reduced by patterning the pentacene active layer. The resulting devices exhibited minimal hysteresis in their output and transfer characteristics. Optimized OTFT structures possessed a field-effect mobility of 0.33 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of -4 V, a subthreshold slope of 1.5 V/decade, and an on/off current ratio of 1.2×10^6. © *2009 American Institute of Physics*.
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I. INTRODUCTION

Organic thin film transistors (OTFTs) possess two key advantages over structures fabricated from inorganic semiconductors: mechanical flexibility and low-cost manufacture. Various organic semiconductor materials have been used as the active layer in OTFTs. These include molecular crystals such as pentacene, which can be deposited in thin film form by thermal evaporation, and conductive polymers, which can be conveniently processed by solution-based methods, such as spin coating and inkjet printing.[1] The gate dielectric layer also plays a crucial role in determining the performance of organic transistors;[2] the benefits of OTFTs can easily be lost if inappropriate insulators are used. For example, the inorganic insulator SiO_2, a common gate dielectric in OTFTs, will crack under stresses caused by the bending of plastic substrates. Certain organic gate insulators, such as benzocyclobutene, need a very high curing temperature, which precludes the use of many organic substrates.

A range of different organic materials has been investigated for the gate dielectric. These include poly(vinyl alcohol), poly(vinyl phenol), and poly(styrene).[1] Hybrid organic/inorganic insulators have also been used.[3] The high resistivity ($>2\times10^{15}\ \Omega$ cm) and low dielectric constant (approximately 3, similar to that of silicon dioxide) of poly(methyl methacrylate) (PMMA) make it potential candidate as the dielectric layer in OTFTs.[2,4] Furthermore, this polymer contains hydrophobic methyl radical groups, which can play a role as moisture inhibitors, as well as encourage good ordering of the active organic overlayer as it is deposited on the surface.[5] To date, pentacene-based OTFT devices using PMMA as the gate dielectric have shown low field-effect mobilities (generally less than 0.1 $cm^2\ V^{-1}\ s^{-1}$) due to the relatively thick film of PMMA used, low on/off current ratios (10^3) resulting from large leakage currents, and high threshold voltages (-15 to -25 V).[6–9] However, one encouraging result is that of Huang *et al.*,[10] who reported a mobility of 0.24 $cm^2\ V^{-1}\ s^{-1}$ using a 300 nm thick PMMA layer.

In this work, spin coating has been used to produce high quality thin layers of PMMA. These have been incorporated into pentacene OTFTs and the electrical characteristics have been studied as a function of the insulator thickness. It is shown that leakage currents can be reduced significantly by pattering the active layer, leading to a good on/off current ratio. Finally, the influence of scaling of the channel length and width on the transistor characteristics is reported.

II. EXPERIMENT

In this work, top-contact OTFTs were fabricated using the structure shown schematically in Fig. 1. The device fabrication was undertaken in a class 1000 clean room. Glass slides were used as the substrates and an aluminum gate (thickness: 30 nm) was defined by thermal evaporation through a shadow mask. An anisole (methoxybenzene; obtained from MicroChem) solution of PMMA (M_w=93 000, obtained from Sigma-Aldrich) was spin coated on top and cured for 1 h at 120 °C. The thickness of the PMMA film was varied from 100 to 2000 nm by changing the solution concentration and spin-coating speed. Following this, pentacene (Sigma-Aldrich and used without further purification) was thermally deposited at room temperature to a thickness

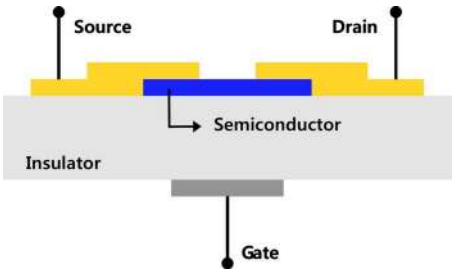

FIG. 1. (Color online) A schematic cross section of the pentacene-based OTFT with a PMMA gate dielectric.

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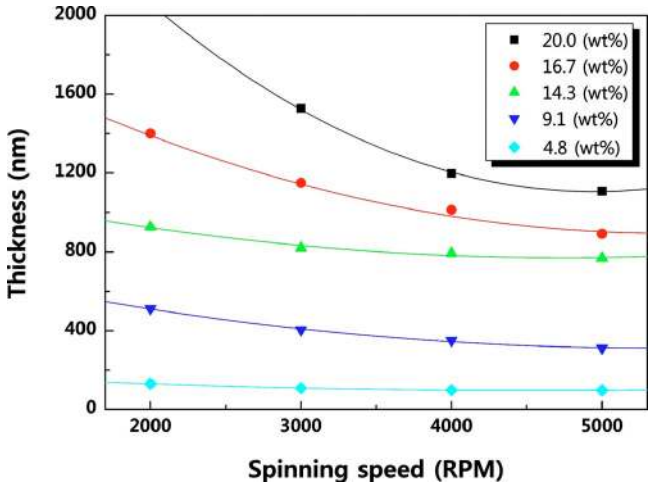

FIG. 2. (Color online) Thickness of spin-coated PMMA films as function of spinning speed and solution concentration.

of 30 nm. To explore the effects of patterning the active layer, the pentacene was deposited with and without the use of a shadow mask. The deposition rate was 0.05 nm s^{-1} at a chamber pressure of approximately 1×10^{-6} mbar. A further shadow mask was used to define source and drain contacts, formed by the thermal evaporation of 30 nm of gold. The thicknesses and morphologies of the various layers were studied using a Digital Instruments Nanoscope IV atomic force microscope.

The OTFT current I versus voltage V characteristics were measured using a Keithley 485 picoammeter and 2400 source meter. The capacitance C versus voltage behavior was monitored with an HP4192A impedance analyzer.

III. RESULTS AND DISCUSSION

A. PMMA thickness

Figure 2 shows the thickness of PMMA as a function of spinning speed and solution concentration. Above 15 wt % polymer, the film thickness was inversely proportional to the spinning speed. For lower PMMA concentrations, the solution concentration was much more effective than spinning speed for controlling the thickness of the polymer. Uniform pinhole-free and crack-free films of PMMA could be obtained by spin coating, with a lower limit to the thickness of about 150 nm. Atomic force microscope images of the surfaces of a 150 nm PMMA film and of a 30 nm pentacene film, which was subsequently evaporated onto the PMMA, are shown in Fig. 3. A relatively smooth surface is evident for the PMMA [Fig. 3(a)]. The rms roughness was 0.30 nm; this can be contrasted with figures of 0.45–0.76 nm reported by Shin *et al.*[11] for a 140–160 nm thick PMMA layer. The grain size for the pentacene was greater than 1 μm [Fig. 3(b)], with a rms roughness of 13 nm. These figures are similar to those reported by Huang *et al.*[10] for pentacene evaporated onto PMMA: grain size of 1.0–1.5 μm and rms roughness of 11 nm.

A parallel plate capacitor structure (Al/insulator/Au) was fabricated to investigate the dielectric properties of the PMMA. The area of the top Au electrode was 2.25

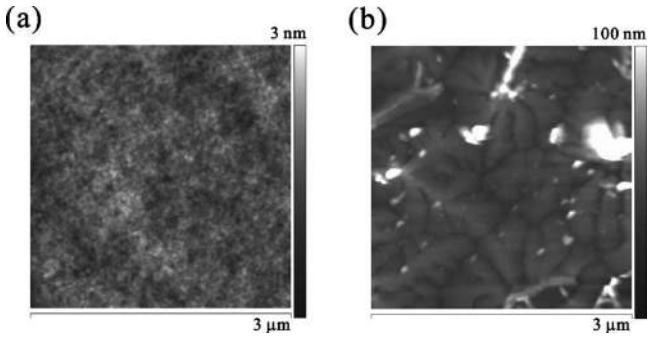

FIG. 3. Atomic force microscope images of (a) 150 nm thick PMMA film spin coated onto a glass slide and (b) 30 nm thick pentacene film thermally evaporated on top of the PMMA.

$\times 10^{-2}$ cm^2. Figure 4 shows the current density J versus the electric field F for a 150 nm thick PMMA film. These data were similar for either polarity of voltage applied to the top electrode. The leakage current density is less than 10^{-8} A cm^{-2} for fields of up to 0.4 MV cm^{-1} and this remained below 10^{-6} A cm^{-2} for fields of up to 2 MV cm^{-1}. Such current densities are sufficiently small to allow the use of the 150 nm PMMA film as a gate dielectric in an OTFT.

Physical processes that might account for the current versus voltage behavior in the presence of high electric fields are Schottky emission and the Poole–Frenkel effect.[12,13] The former process occurs at the interface between the electrode(s) and the dielectric and has an I versus V dependence of the form

$$I \propto T^2 \exp\left(\frac{\beta_{Sc} V^{1/2} - \Phi_{Sc}}{k_B T}\right), \tag{1}$$

where Φ_{Sc} is the Schottky barrier height, β_{Sc} is the Schottky coefficient, T is the temperature, and k_B is the Boltzmann constant.

Poole–Frenkel conductivity is a similar process to Schottky emission, but it results from the lowering of the potential barriers around impurity centers in the bulk of the insulator. The I-V relationship is given by

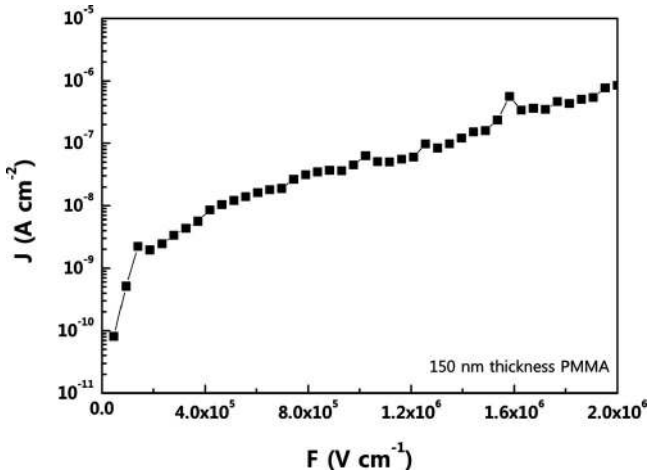

FIG. 4. Current density vs applied electric field for an Al/PMMA/Au structure. The PMMA film thickness=150 nm.

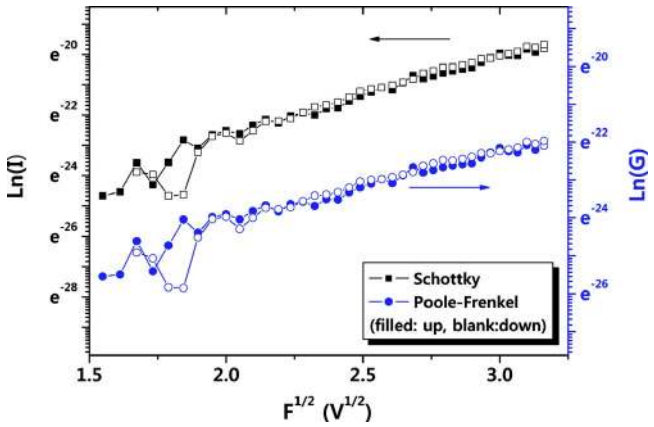

FIG. 5. (Color online) Schottky [$\ln(I)$ vs $F^{1/2}$] and Poole–Frenkel [$\ln(I/V)$ vs $F^{1/2}$] plots for an Al/PMMA/Au structure. The PMMA film thickness $=150$ nm.

$$I \propto V \exp\left(\frac{\beta_{\mathrm{PF}} V^{1/2} - \Phi_{\mathrm{PF}}}{k_B T}\right), \tag{2}$$

where Φ_{PF} is the potential barrier height and β_{PF} is the Poole–Frenkel coefficient. Figure 5 shows the conductivity data obtained for the 150 nm PMMA film plotted in the form of the Schottky [$\ln(I)$ versus $V^{1/2}$] and Poole–Frenkel [$\ln(I/V)$ versus $V^{1/2}$] equations. Data are shown for both increasing and decreasing applied voltages. In each case, the fit to theory is very good. Either process (or both) might be responsible for the currents in the PMMA at high electric fields. Further work (e.g., variation in the insulator thickness and measurements at different temperatures) is clearly needed to distinguish between these electrical conduction processes.

Figure 6 shows the measured capacitance per unit area as a function of frequency for an 810 nm thick PMMA layer sandwiched between the Au and Al electrodes. The dielectric constant of the PMMA decreases over the frequency range of the measurements and was calculated to be 3.66 ± 0.10 at 1 kHz and 2.89 ± 0.10 at 1 MHz. These values agree well with other literature reports.[4,6,9,14] The C versus V characteristics, measured at 1 MHz and a voltage scan rate of 1 V s^{-1}, of

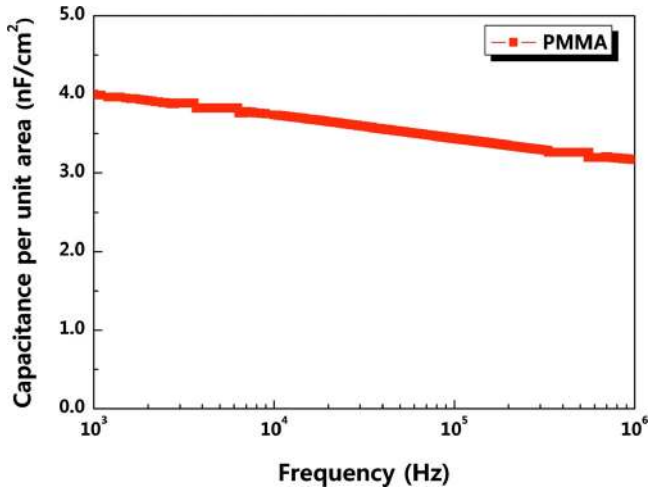

FIG. 6. (Color online) Capacitance vs frequency characteristics of a spin-coated PMMA layer; thickness=810 nm.

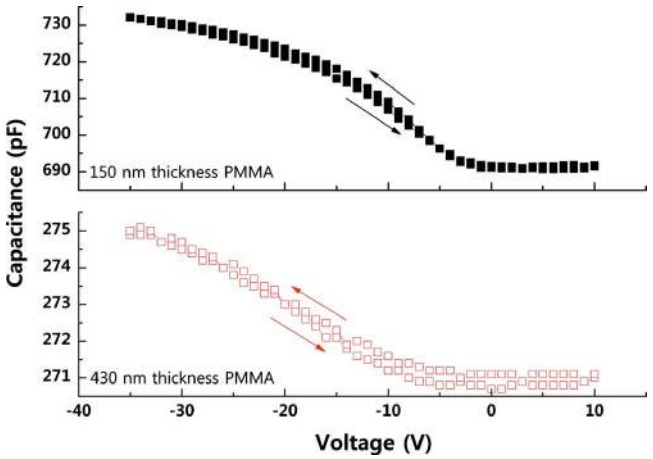

FIG. 7. (Color online) Capacitance vs voltage characteristics, measured at 1 MHz and voltage scan rate of 1 V s^{-1} for Al/PMMA/pentacene/Au structure for two different thicknesses of PMMA. Pentacene thickness=30 nm.

two Al/PMMA/pentacene/Au metal-insulator-semiconductor (MIS) structures are shown in Fig. 7. The C-V data for both samples (PMMA thicknesses of 150 and 430 nm) reveal the accumulation (large negative voltage applied to Al), depletion, and inversion behavior that is typical of MIS devices. Little hysteresis is evident on reversing the direction of the voltage scan. The anticlockwise direction of this may be related to the charging and discharging of interface traps located at, or close to, the PMMA/pentacene interface.[15] The accumulation capacitance values for the two MIS structures scale with the PMMA thickness and the calculated dielectric constant is consistent, within experimental errors, with the value calculated from the Au/PMMA/Al structure (Fig. 6).

In this study, 14.3 wt % (810 nm), 9.1 wt % (427 nm), and 4.8 wt % (152 nm) solutions of PMMA, spin coated at 3000 rpm, were used to investigate the dependence of the electrical behavior of the transistors on the PMMA thickness. Figure 8 shows (a) the dependence of the drain-source current I_{DS} on the drain-source voltage V_{DS} (the OTFT output characteristics) and (b) the dependence of I_{DS} on the gate-source voltage V_{GS} (transfer characteristics) for the devices on the different thicknesses of PMMA; forward and reverse voltage scans are shown. The gate-source voltage was -30 V for the output characteristics and the drain-source voltage was -30 V for the transfer characteristics. The channel width W to length L ratio was 40 (channel length=50 μm; width=2000 μm).

These data agree with simple thin film transistor theory.[1] For low V_{DS} ($V_{\mathrm{DS}} < V_{\mathrm{G}}$), the drain-source current is related to the drain-source voltage by

$$I_{\mathrm{DS}} = \frac{WC_i}{L}\mu\left[V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}\right]V_{\mathrm{DS}}, \tag{3}$$

where V_T is the threshold voltage, C_i is the insulator capacitance per unit area, and μ is the field-effect mobility. The threshold voltage represents the value of the gate-source voltage beyond which a conductive channel forms at the pentacene surface (i.e., the transistor is turned on). This defines the linear region of device operation. As the gate insulator thickness is reduced, C_i will increase, accounting for the

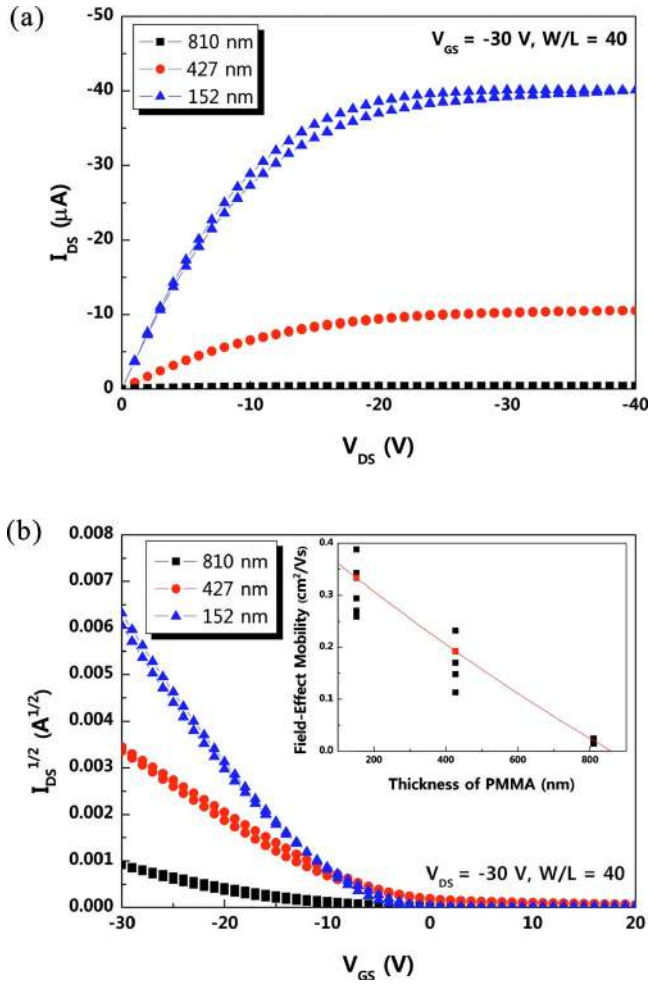

FIG. 8. (Color online) (a) Output and (b) transfer characteristics with different thicknesses of PMMA. Inset: field-effect mobility as a function of the thickness of PMMA.

larger drain-source currents evident in Fig. 8.

For high V_{DS}, the drain-source current saturates as the conductive channel becomes "pinched off," and the saturated drain-source current $I_{DS(sat)}$ is given by

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu(V_{GS} - V_T)^2. \quad (4)$$

The value of μ may therefore be evaluated from a plot of $(I_{DS(sat)})^{1/2}$ versus V_{GS}. The intercept of this plot can be used to determine the device threshold voltage. The inset of Fig. 8(b) shows the variation in the field-effect mobility with insulator thickness for a number of different devices. A clear trend showing an increase in μ with the decrease in the thickness of the gate insulator is evident. Averaged data reveal that μ increased by about 13 times for a fivefold reduction in the PMMA thickness.

This effect has been reported previously for pentacene OTFTs (see, for example, Ref. 16), and there are now a number of different explanations for the dependence of carrier mobility on gate insulator thickness. For example, the phenomenon might be due to a variation in the gate dielectric constant of the film with the concentration of the PMMA solution.[17] Veres *et al.*[2,18] suggested that a higher dielectric constant induces a broadening of the density of states (DOS) at the polymer/insulator interface. This results in a decrease in the DOS at the Fermi energy and subsequently causes a lower hopping probability, leading to a suppression of the carrier mobility. This effect can occur for OTFTs based on both polymers and low molecular weight materials such as pentacene. More recent work suggests that a mobility dependence for pentacene transistors can result from the viscoelastic properties of the organic dielectric.[19] It is certainly possible that our very thin PMMA spin-coated layers possess different surface chain dynamics. Alternatively, the morphological properties of the thinner PMMA films may provide for improved growth of the thermally evaporated pentacene, resulting in larger grains and higher carrier mobilities.

A theory described by Necliudov *et al.*[20] incorporates a gate-voltage dependent mobility. According to this model, in pentacene-based OTFTs operating above threshold, most of the charge induced by the gate-source voltage is trapped in numerous traps and only a fraction of the carriers participate in the current conduction. The effect of the charge trapping is accounted for by the gate-voltage dependent field-effect mobility given by[20–22]

$$\mu = \mu_0\left(\frac{V_{GS} - V_T}{V_{AA}}\right)^{\gamma}, \quad (5)$$

where γ and V_{AA} are empirical parameters, which can be extracted from the transfer characteristics, and μ_0 is a constant. The number of accumulated carriers at the pentacene surface will depend on V_{GS}; an increase in V_{GS} will result in an increase in the number of surface carriers. The same effect will be obtained if V_{GS} is held constant and the gate insulator thickness is reduced, due to an increase in the electric field in the insulator. Hence, for the same gate-source voltage, there will be more surface carriers available to fill the traps for a thinner insulator. Increasing the permittivity of the gate insulator will produce similar results.[16] The thinnest PMMA layers used in our work were 150 nm, limited by the quality of the spin-coated film. So far, we have been unable to use thinner gate dielectrics to explore if even higher mobility devices could be achieved.

We have also used the plot of $(I_{DS(sat)})^{1/2}$ versus V_{GS} to determine the values of the threshold voltages for our OTFTs with different PMMA thicknesses. The trend was a decrease in V_T with a decrease in the thickness of the gate dielectric, from about -11 V for 810 nm gate insulators to approximately -4 V for the OTFTs with PMMA thicknesses of 152 nm. However, there was much variability between the samples (a full table showing all the parameters for our devices is shown later on, in Sec. III C) and these figures represent average values for a number of devices. The theoretical dependence of V_T on the thin film transistor parameters is quite complex. Assuming that there is no work function difference between the gate metal and the semiconductor, the magnitude of V_T can be approximated by[23]

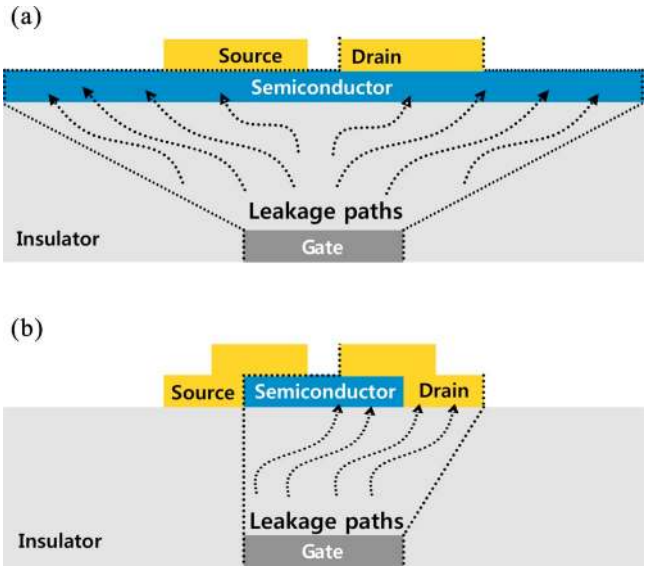

FIG. 9. (Color online) Possible leakage paths in (a) unpatterned pentacene OTFT and (b) patterned pentacene devices.

$$V_T = \left| \frac{Q_s}{C_i} \right|, \tag{6}$$

where Q_s is the effective total charge per unit area at the insulator/semiconductor interface at zero gate voltage. This charge (which may be positive or negative) will be made up from a number of contributions: mobile and fixed charges in the insulating layer and interface state charge. Our results reveal that the value of V_T decreases by a factor of approximately 3 for a fivefold decrease in the gate insulator thickness. This suggests that Q_s probably also varies with the thickness of the PMMA in our OTFTs.

B. Patterning the organic semiconductor

A further problem with OTFTs using PMMA as the gate dielectric has been a low on/off current ratio. This can be related to the drain offset current, which is defined as the drain current at different gate biases when the drain-source bias is zero. For an ideal device, $I_{DS}=0$ A for $V_{DS}=0$ V. The I_{DS} offset is closely related to I_{GS} and is a convenient indicator of gate induced leakage in OTFTs. Jia *et al.*[24] reviewed the possible origins of I_{DS} offset and concluded that the effect is related to the expansion of the source and drain electrodes by the semiconductor accumulation layer. The latter provides leakage paths and more current flows through the insulator as a result of these, as shown in Fig. 9(a). The leakage paths can be eliminated by patterning of the active layer [Fig. 9(b)]. This was confirmed by Jia *et al.*,[24] who reported a substantial reduction in the I_D offset following patterning of the organic semiconductor (poly-3-hexylthiophene).

We have explored the effects of patterning the pentacene layer using shadow masks. Figure 10 shows a photograph of one of the patterned pentacene/PMMA devices. The pentacene is visible between the gold source and drain electrodes. The electrical behavior of the patterned OTFTs is shown in Fig. 11. Figure 11(a) depicts the drain current at different

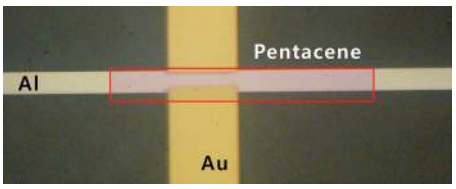

FIG. 10. (Color online) Optical micrograph of a patterned pentacene-based OTFT with PMMA gate dielectric (channel length=50 μm; channel width=500 μm).

gate biases when the drain-source bias (V_{DS}) was zero. For the unpatterned OTFT, it is evident that the offset in the drain current increased with increasing gate voltage. Patterning markedly decreases this effect. The gate leakage can be seen more clearly in the transfer characteristics [Fig. 11(b)], for which $V_{DS}=-25$ V. There is a large gate leakage in the unpatterned device, but again, this effect is much reduced in the OTFT in which the pentacene film is confined to the region between the source and drain electrodes.

C. Effect of channel dimensions

Figure 12 shows the relationship between $I_{DS(sat)}$ and the ratio W/L for a number of our OTFTs with a fixed 50 μm channel length and $V_{GS}=-25$ V; the PMMA thickness was

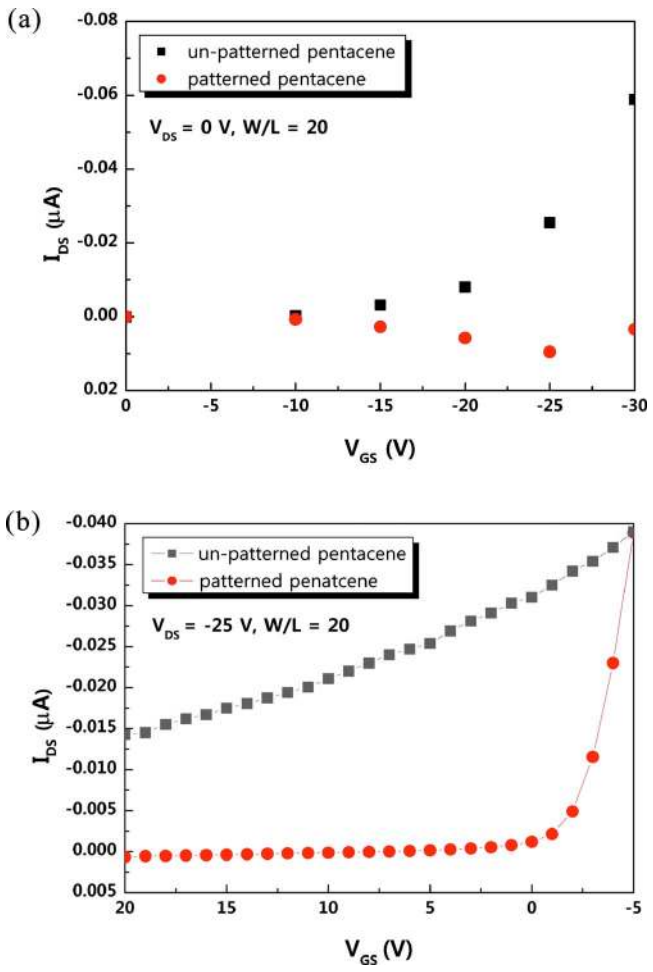

FIG. 11. (Color online) (a) I_{DS} offset ($V_{DS}=0$ V) and (b) leakage currents ($V_{DS}=-25$ V) in patterned and unpatterned pentacene OTFTs.

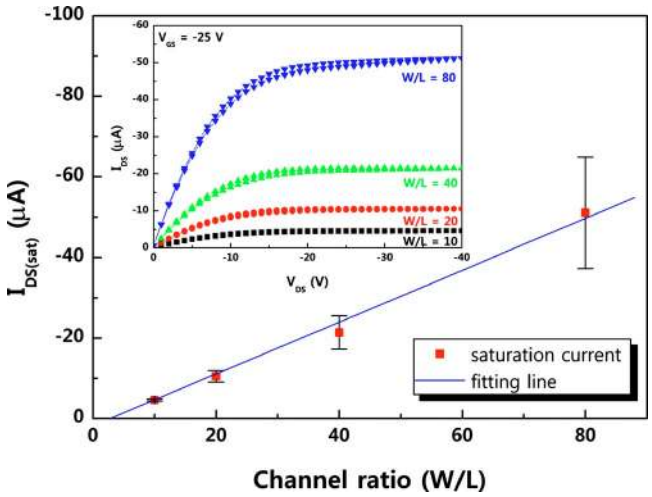

FIG. 12. (Color online) $I_{DS(sat)}$ vs channel width:length ratio (W/L) for pentacene OTFTs. The output characteristics are shown in the inset. V_{DS}= −25 V. PMMA thickness=152 nm.

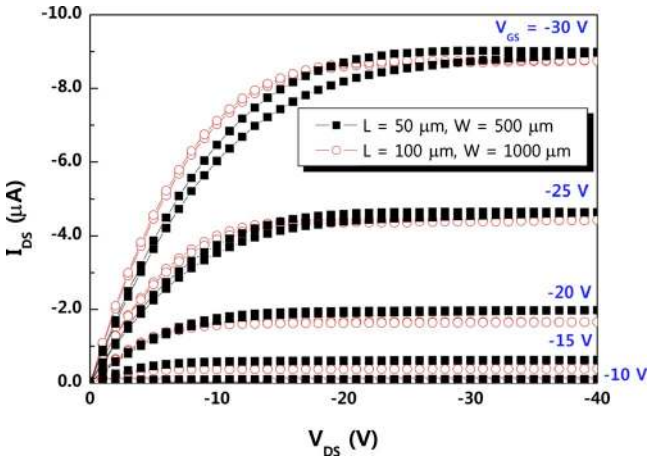

FIG. 13. (Color online) Output characteristics for OTFTs with the same channel width:length ratio but different channel lengths and widths. PMMA thickness=152 nm.

152 nm. The error bars reflect measurements on a number of different samples. The inset shows a typical set of output characteristics for these devices. Within experimental error, the saturated drain-source current varies linearly with W/L, as predicted by Eq. (2). The effects of keeping the same channel width to length ratio (W/L=10), but using different absolute values, are shown in Fig. 13: the results are for 50 μm channel length and 100 μm channel length structures. Both sets of data show similar output characteristics. However, the device with the longer channel shows improved saturation at lower values of V_{DS} and less hysteresis (evident as the gate-source voltage is increased). We attribute these effects to the ability to align the patterned pentacene during the OTFT manufacture.

Table I provides a summary of the electrical characteristics of all of the devices that were fabricated in this study. The output and transfer characteristics for an optimized OTFT are shown in Fig. 14; PMMA thickness=152 nm, L =50 μm, and W=2000 μm. For the output characteristics [Fig. 14(a)], linear behavior at low V_{DS} with good drain-source current saturation was observed. For gate voltages below −25 V, minimal hysteresis is evident when the direction of the drain voltage scan is reversed. This suggests a relatively "clean" (in an electronic sense) interface between the pentacene and the PMMA, which is also apparent from the minimal hysteresis in the C-V characteristics of the MIS structures (Fig. 7). Figure 14(b) shows the transfer characteristics of the device, measured at V_{DS}=−30 V. Plots are given in the form of both $\log(I_{DS})$ versus V_{GS} and $(I_{DS})^{1/2}$ versus V_{GS}. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for this particular device were 1.2×10^6, 0.33 cm^2 V^{-1} s^{-1}, −4 V, and 1.5 V/decade. These values compare very favorably with published data for pentacene/PMMA OTFTs.[7–9] For example, Huang *et al.*[10] gave μ=0.24 cm^2 V^{-1} s^{-1} and V_T=−6.3 V; Puigdollers *et*

TABLE I. Summary of pentacene/PMMA OTFT characteristics.

Thickness (nm)	Channel length (μm)	Channel width (μm)	Mobility (cm^2 V^{-1} s^{-1})	Subthreshold slope (V decade^{-1})	V_T (V)	I_{On}/I_{Off}
152	50	500	0.270	2.0	−4	6.9×10^6
	50	1000	0.343	1.2	−3	9.7×10^5
	50	2000	0.333	1.5	−4	1.2×10^6
	50	4000	0.388	2.9	−3	1.5×10^5
	100	1000	0.294	1.7	−6	6.3×10^6
	200	2000	0.259	1.6	−5	5.7×10^6
427	50	500	0.151	5.21	−5	4.1×10^4
	50	1000	0.113	7.4	−3	2.1×10^4
	50	2000	0.192	5.4	5	3.5×10^3
	50	4000	0.232	9.9	3	5.7×10^3
	100	1000	0.170	11	−7	3.5×10^3
	200	2000	0.148	3.7	−8	1.6×10^6
810	50	500	0.014	4.5	−14	2.1×10^4
	50	1000	0.019	3.4	−13	3.2×10^4
	50	2000	0.020	2.6	−10	8.6×10^4
	50	4000	0.017	2.9	−7	1.1×10^5
	100	1000	0.024	2.5	−10	2.8×10^4
	200	2000	0.024	2.4	−10	5.6×10^4

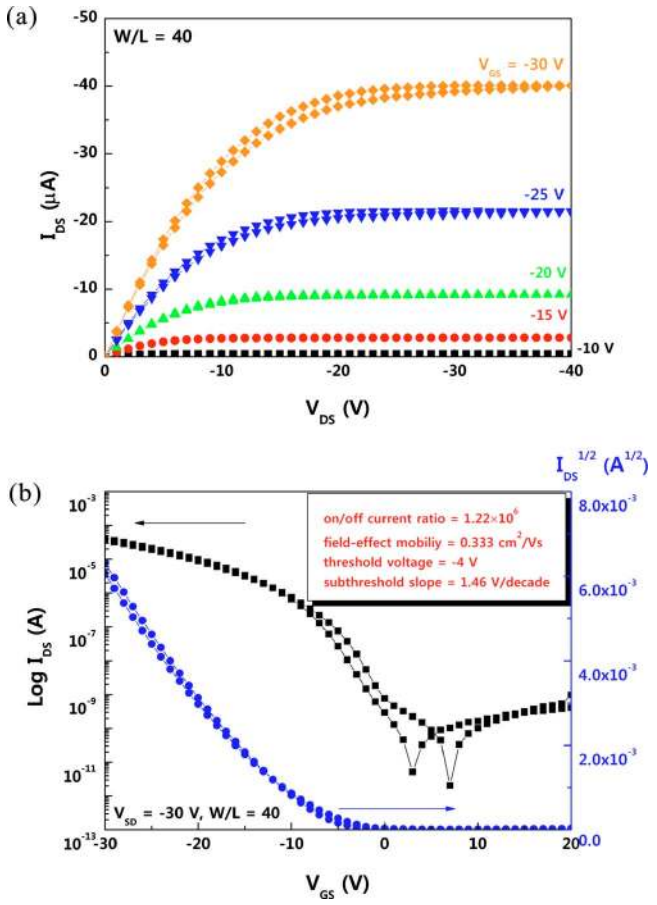

FIG. 14. (Color online) (a) Output and (b) transfer characteristics of a pentacene-based OTFT using PMMA as the gate dielectric. Channel length=50 μm; channel width=2000 μm.

al.[9] reported μ=0.01 cm^2 V^{-1} s^{-1} and $V_T \sim -15$; and Kang *et al.*[7] measured μ=0.045 cm^2 V^{-1} s^{-1} and V_T=−27.5 V. It is interesting to note that these three investigations used gate insulator thicknesses that are greater than the 152 nm for our optimized device, for example, 700 nm in the case of Puigdollers *et al.*[9] and 945 nm for Kang *et al.*[7] This is entirely consistent with the trend of the data shown in Table I, which reveal an improvement in the OTFT characteristics as the PMMA thickness is reduced. The 300 nm film thickness figure and the mobility value of 0.24 cm^2 V^{-1} s^{-1} obtained by Huang *et al.*[10] fit well with the trend of the data shown in the inset of Fig. 8.

IV. CONCLUSIONS

We have shown that the thickness of the PMMA dielectric layer in pentacene OTFTs has a strong influence on the field-effect mobility. In particular, the measured mobility was found to increase as the gate dielectric thickness decreased. With the thickness of the PMMA optimized to 150 nm, the OTFTs possessed a field-effect mobility >0.3 cm^2 V^{-1} s^{-1}, a threshold voltage of around −4 V, an on/off current ratio >10^6, and a subthreshold slope of 1.5 V/decade. The effect of patterning the pentacene layer during device fabrication was also investigated. This resulted in a significant reduction in the leakage currents. Finally, the influence of scaling on the OTFT characteristics was investigated with respect to the channel length and width. The results agree with simple thin film transistor theory. Although further work remains, such as understanding fully the dependence of field-effect mobility on the gate insulator thickness, the results show that PMMA is a very promising candidate for use as a dielectric layer in organic electronic devices.

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