Performance Advantage of Schottky Source/Drain in Ultra-Thin-Body Silicon-on-Insulator and Dual-Gate CMOS

Daniel Connelly (djconnel@ieee.org), Carl Faulkner, D. E. Grupp

Acorn Technologies, Palo Alto, CA

phone : (650)704-8976

Abstract

Here, for the first time, advanced simulation models are used to investigate the performance advantage of Schottky source/drain ultra-thin-silicon technologies at a 25 nm gate length target. Schottky and doped source/drain MOSFETs were optimized and compared using a novel benchmark. Mixed-mode simulations of optimized devices in a two-stage NAND chain show an approximate 45% speed advantage of Schottky source/drain for one set of parameter choices. Contact requirements for Schottky source/drain, and for doped source/drain relative to ITRS targets through 2016, are discussed.

Index Terms

CMOSFET circuits, MOS devices, Semiconductor device modeling, Semiconductor-metal interfaces, Schottky barriers, Silicon, Simulation

I. Introduction

CMOS technology continues its relentless drive toward 25 nm gate lengths. With length scaling comes reduced intrinsic channel resistance, increasingly emphasizing source/drain (S/D) extrinsics. Yet vertical scaling, in particular for single-gate fully-depleted silicon-on-insulator (FDSOI) and dual-gate[1] technologies, results in an increase in the sheet resistances of doped S/D regions. As dimensions shrink, the challenge of establishing and maintaining the required S/D doping gradients [2], including the inevitable atomistic stochas-

[1] The FinFET, for example [1], is a promising implementation.

tics [3], grows more daunting. One alternative to doping is Schottky (metal) S/D [4]. Metal S/D technology is challenging, but at $L = 25\,\mathrm{nm}$, so are all other options. It's thus important to understand the relative performance which can be achieved by doped and metal S/D's.

A previously published simulation study [5] compared these device types. However, the present work has several improvements. One is the use of the density gradient method [6], which accounts for quantum mechanical electrostatic effects which are important at these dimensions. Another is the use of the thermionic field emission model of Ieong *et al.* [7]; the approach used in the prior work neglects tunneling and thus can substantially underestimate current at metal-semiconductor contacts with large electric fields. Also, a more aggressive device design is considered here. The result is a much more realistic prediction of relative device performance, particularly considering the effect of changes in the metal S/D workfunction.

In [8], mixed-mode simulation is used to demonstrate the advantage of underlap in dual-gate metal S/D design. Here a broader view is taken, with an emphasis on a fair comparison of dual-gate and single-gated devices of each S/D type, using both discrete device benchmarking and mixed-mode circuit performance.

Other comparisons of Schottky and doped S/D ultra-thin-body MOSFET performance [9][10] have used devices with unoptimized source/drain placement. Furthermore, threshold-voltage roll-off was neglected, and circuit performance was not directly simulated.

II. Device Structure

NFET cross-sections are shown in Fig. 1. The S/D contacts were angled to reduce coupling capacitance while allowing a contact close to the channel. Contact was to the sidewall of metal S/D's and to the silicon top surface of doped S/D's. The gate was tunable-workfunction metal, where the workfunction was set to meet the leakage current constraint.

With FDSOI, the substrate was treated as a metallic contact to the bottom of the buried oxide.

[Fig. 1 about here.]

Doped S/D's were modeled using Gaussian profiles of arsenic (NFET) or boron (PFET) – one for FDSOI, and two for dual-gate. For each, concentration was constant along a reference line segment from the edge of the device to $\Delta x = x_{SD}$ from the edge of the gate, at $\Delta y = y_{SD}$ from the silicon surface(s) (top only for FDSOI, both to maintain symmetry for dual-gate). For each reference segment, the profile was attenuated as a Gaussian of $\sigma = \sigma_{SDy}$ above and below the segment, $\sigma = \sigma_{SDx}$ to the side. For dual-gate, the Gaussian amplitudes were reduced to maintain a net concentration of N_{SD} on each reference segment given the contribution from the other profile in the same S/D region. Atomistic dopant effects, significant in doped devices of this scale [3], were neglected.

Key NFET parameters are shown in Table I. PFETs were designed with the same parameters as NFETs, but with doping types swapped, and with metal S/D workfunctions near the silicon valence band rather than the conduction band.

[Table 1 about here.]

III. Modeling Details

A. Device Modeling

ISE/DESSIS version 8.0.5 [11] was used. Discrete device simulations used the density gradient model [12] with parameters from [13]. Metal S/D's were treated using the DESSIS implementation of the nonlocal thermionic field emission model of [7]. Light-carrier-dominated tunneling was assumed (NFET electron effective mass of 0.19, PFET hole effective mass of 0.16), with a Richardson factor of 2.1 for NFETs and 0.66 for PFETS [11] and a

tunneling submesh of 100 points[2] over 30 nm. Continuity equations and the density gradient equations were both solved for minority carriers only, as bipolar effects were found to be insignificant at the current levels of interest.

Low-field transport was treated via the drift-diffusion model of [14]. Assumptions implicit in this model are invalid at these gate lengths and silicon thicknesses. But the relative effect of the S/D is the focus here, and thus a highly accurate channel transport model is not required.[3]

High-field transport was handled with a Caughey-Thomas term [16] :

$$v = \mu \left|\nabla\phi_F\right| \left[1 + \left(\mu \left|\nabla\phi_F\right| / v_{sat}\right)^{\beta}\right]^{-1/\beta} , \tag{1}$$

where v is the magnitude of the mean carrier velocity, μ is the low-field mobility, $|\nabla\phi_F|$ is the magnitude of the quasi-Fermi potential gradient, v_{sat} is the saturation velocity, and β is an empirical parameter. Values of v_{sat} and β to accommodate Monte-Carlo simulation of ballistic transport in decananometer devices are described in [17]. For this work, given the lack of experimental data on high-field transport in silicon films in the $t_{\mathrm{Si}} \leq 5\,\mathrm{nm}$ range, more conventional values from [11] after [18] were used : for electrons $\beta = 1.11$ and $v_{sat} = 1.07 \times 10^7\,\mathrm{cm/sec}$, while for holes $\beta = 1.21$ and $v_{sat} = 0.84 \times 10^7\,\mathrm{cm/sec}$. If electron velocities were underestimated, then performance advantages predicted here were also underestimated, as the extrinsic resistance would be more significant.

Metal contacts were treated as constant potential surfaces whose workfunctions were specified relative to the vacuum potential. The assumed value of X_e, 4.072 eV at $T = 300\,\mathrm{K}$, must be considered when comparing workfunctions specified here to those published elsewhere.

[2] reduced to 40 points for mixed-mode simulations
[3] See [15] for another example of the use of drift-diffusion to compare 25 nm ultra-thin-body MOSFETs.

B. Meshing

Meshing was performed using ISE/MDRAW version 8.0.4, with approximately 2300 to 5000 mesh vertices per device for discrete device simulations, 880 to 1900 for circuit simulations.

C. Device Benchmarking

It is critical in device benchmarking to consider the effect of device variation; the "average" device characteristics alone are insufficient. In [19], variability in buried oxide thickness, silicon thickness, gate oxide thickness, and doping are all considered. Here the simpler approach of [20] was followed, with all device variation assumed to be in the gate length. Leakage current[4] was determined using the $L = L_{sub} \equiv L_{nom} - \sigma_L$ subnominal device, as shorter-than-average devices dominate the net circuit leakage.[5] The gate workfunction which yielded a leakage target of $20\,\mathrm{nA}/\mu\mathrm{m}$ at L_{sub} was used to simulate the $L = L_{sup} \equiv L_{nom} + 2\sigma_L$ supernominal device, under the assumption that the clock-limiting path among many candidates will likely have longer than average devices. After Equation 5.38 of [21], the supernominal current was evaluated at $V_G = 0.7\,V_{DD}$[6] for both $V_D = V_{Dlin} \equiv 50\,\mathrm{mV}$ (yielding I_{tlin}) and $V_D = V_{DD} \equiv 1\,\mathrm{V}$ (yielding I_{tsat}). These are summarized in Table II. A harmonic mean, weighting in proportion to drain voltages[7], was used as the benchmark :

[Table 2 about here.]

[4] I_D for $V_D = V_{DD} \equiv 1\,\mathrm{V}$, $V_G = 0$.

[5] The device with $L = L_{sub}$ has leakage current which approximates the average leakage current of all nominally equivalent devices of nominal length L_{nom}, assuming gate length is normally distributed and leakage current is near-exponential with gate length [20].

[6] The optimal V_{DD} fraction is specific to a given application; [21] claims it to be a "numerical fitting parameter" and "≈ 0.7". The use of I_D at $V_G = 0.7\,V_{DD}$ in Table II follows from Equation 5.38 of [21] if $I_D \propto V_G - V_T$.

[7] This crudely averages the channel resistance during switching. The optimal weighting of $1/I_{tlin}$ and $1/I_{tsat}$ is also application-specific, and thus the weighting should calibrated with circuit simulations.

$$I_t = \frac{V_{Dlin} + V_{DD}}{V_{Dlin}/I_{tlin} + V_{DD}/I_{tsat}} \quad (2)$$

This approach is more complex than just looking at I_{Dsat} of the nominal-length device. However, the advantages are :

1. It includes consideration of low-V_D performance, which is needed if the circuit is to gain the full benefit of the supply voltage range.
2. It properly rewards a flatter V_T *vs.* L behavior near $L = L_{nom}$. A single-length approach does not.
3. It recognizes that devices do not see full $V_G = V_{DD}$ during the key portion of switching transients.[8]

D. Device Design

Parameters to be optimized were x_{SD} for the doped S/D, and L_x for the metal S/D. L_x was limited to at least 3 nm to avoid S/D shorts to the gate. In doped S/D devices with $x_{SD} > 3$ nm, L_x was set to x_{SD} to keep the contact in the heavily doped region.

Silicon thickness t_{Si} was constrained to be 4 nm for the FDSOI devices, based on several considerations. One is that for $t_{Si} \leq 3$ nm, structural electron confinement severely reduces mobility [22]. Another is that the threshold voltage sensitivity to silicon thickness becomes significant as t_{Si} drops below 5 nm [23], excessively increasing intradevice and interdevice threshold variation if t_{Si} is taken too much lower. For dual-gate, $t_{Si} = 5$ nm was the primary choice to accommodate a more challenging fabrication, but $t_{Si} = 4$ nm was also simulated. Recently published work [24][25] shows PFET mobility may be sufficiently reduced by thickness-variation scattering to make thicker films preferable. Dual-gate is thus even more attractive relative to FDSOI than presented here, due to dual-gate's ability to

[8] See Fig. 5.28 of [21].

maintain gate control to higher t_{Si} values.

[Fig. 2 about here.]

Tuned gate workfunctions of selected subnominal-length devices are shown in in Fig. 2. As the source and drain are moved closer, S/D-to-channel coupling becomes stronger, and the gate workfunction needs to be increased to maintain the off-state leakage condition. This coupling is stronger for a metal than a doped S/D, due to the lack of a depletion region in the metal. Thus the metal S/D should have a larger optimal S/D-to-gate offset.

The primary "uncontrolled" parameter was ρ_{SD} for the doped S/D, and $\Delta\Phi_{SD}$ for the metal S/D.[9] For each value, the parameter to be optimized was varied in 1 nm increments until the maximum of I_t was straddled. The optimal L_x or x_{SD} was then parabolically interpolated, and the associated device simulated to yield the optimized device benchmark.[10]

An example of this optimization, with a finer sampling of L_x values, for metal S/D is shown in Fig. 3. For FDSOI, optimization is a balance between reducing short channel effects with a greater S/D separation (longer extension), and maximizing drive with a reduced S/D separation (shorter extension). The optimal was still a considerable S/D-to-gate underlap. For dual-gate, the minimum $L_x = 3\,\mathrm{nm}$ was preferable to greater underlaps. A similar tradeoff is involved with x_{SD} for the doped S/D devices.

[Fig. 3 about here.]

[9] Φ_{SD} may differ from the value appropriate for planar junctions due to effects of quantum confinement at nanometer scales. Guo *et al.*[10] discuss the effect on the Si conduction band, but the metal bands, and the states responsible for Fermi level pinning [26], will also be affected.

[10] If, in the case of the metal S/D, the peak I_t was for $L_x < 3\,\mathrm{nm}$, $L_x = 3\,\mathrm{nm}$ was used instead.

IV. Results & Discussion

A. Discrete Device

Fig. 4 shows *I-V* curves for FDSOI MOSFETs. Doped FETs with ρ_{SD} either 10^{-3} or $3\,\Omega$-μm^2 are shown in (a) and (b). The significant drive degradation due to the contact resistance, especially at low V_D, is clear. Metal S/D results are shown in (c) and (d). The thermionic barrier grows as Φ_{SD} passes the affinity of the channel carrier (electron in NFET, hole in PFET), again causing a reduction in current which is more prominent at low V_D.

[Fig. 4 about here.]

Fig. 5 shows the results of the device optimization for both FDSOI and dual-gate NFETs, for both S/D types. Marked on the graphs are some references for the S/D parameters – for doped S/D (a and b), 2001 ITRS Roadmap for Semiconductors [27] targets for 2010 and 2016 are shown, while for metal S/D (c and d), X_e is indicated. The optimized S/D offsets in (a) are quite close to those derived from mixed-mode transient circuit calculations, presented in [8].[11]

[Fig. 5 about here.]

Lessons from Fig. 5 include :

1. From (a), lower ρ_{SD} implies a slightly lower optimal x_{SD}, as the extension resistance becomes a greater fraction of the extrinsic S/D resistance, and thus increasing S/D-to-gate overlap has more effect on the drive current capacity.
2. From (b), $\rho_{SD} > 0.1\,\Omega$-μm^2 significantly degrades performance of doped S/D devices. ITRS projections for ρ_{SD} through 2016 fall well short of achieving their full potential.
3. From (c), lower Φ_{SD} implies a greater optimal L_x, as the electron concentration in the

[11] In [8] a different Schottky S/D structure is used which allows arbitrary S/D-to-gate underlap and overlap, so the values in Fig. 5(c) cannot be compared to those published there.

vicinity of the metal is increased, decreasing the "effective" source-drain separation at a given L_x.

4. From (d), for $\Phi_{SD} > X_e$, the thermionic barrier substantially reduces metal S/D performance.

It is evident that managing the extrinsic S/D resistance is critical for both doped and metal S/D. The doped S/D, in the ideal limit, comes within approximately 5% of the limiting metal S/D I_t. The primary issue, therefore, is how closely each approach can be taken to its ideal limit.

ITRS 2001 targets go from $6.4\,\Omega$-μm^2 in 2010 to $2.4\,\Omega$-μm^2 in 2016. A value of $3\,\Omega$-μm^2 can thus be considered characteristic of what might be achieved in the next decade. For the metal S/D devices, $\Phi_{SD} = 4.05\,\text{eV}$ was used, within k_BT of the 300 K value $X_e = 4.072\,\text{eV}$.

These values yielded the discrete device benchmark comparison in Table III. The metal S/D had an approximate 33% improvement in I_t of NFETs. PFET metal S/D workfunctions were reflected about the silicon mid-gap, $\Phi_{SD} = 5.22\,\text{eV}$ versus $\Phi_{SD} = 4.05\,\text{eV}$ for the NFETs. The PFET metal S/D benchmark advantage was approximately 23%.

[Table 3 about here.]

B. Circuit

A two-stage NAND chain with fan-out of two (see Fig. 6) was simulated using the DESSIS mixed mode capability to assess integrated behavior in a sample application. All devices had $L = L_{sup}$, in order to predict the performance of the clock-limiting path, for which it is assumed there are many candidates. The gate-loaded limit was considered, so interconnect loads were omitted, and device widths were normalized. The output load was a dummy gate – a metal-SiO_2-n^+ ($10^{20}/\text{cm}^3$) capacitor of the same L, t_{ox}, and Φ_G. All devices were assigned a gate workfunction which yielded $I_D = 20\,\text{nA}/\mu\text{m}$ for $V_G = 0$ and $V_D = 1\,\text{V}$

at $L = L_{sub}$, as determined in the discrete device simulations described in IV-A.

[Fig. 6 about here.]

To accommodate the increased device count, mesh spacings were roughly doubled relative to the discrete device simulations, and the thermionic field emission submesh was reduced from 100 to 40 points. For numerical stability, the density gradient model was not used.[12] The reduced mesh density was observed to have negligible effect on device I-V characteristics.

Simulations were done for the devices from Table III. Input V_{in} was a 1 ps transition from 0 to 1 V at $t = 0$, followed at $t = 50$ ps by a 1 ps transition back to 0 V. Sample rising-edge transient responses are shown in Fig. 7. The output V_{out} was considered to have switched at 80% V_{DD} for the rising transition and 20% V_{DD} for the falling transition.[13] Delay was calculated relative to the previous crossing of 50% V_{DD} by V_{in}.

Results, seen in Fig. 8, show the metal S/D to be approximately 45% faster than doped S/D for the same device type. This is a somewhat larger improvement than was predicted using the benchmark for discrete device optimization, I_t, which was uncalibrated and which neglects the effect of capacitance differences.

[Fig. 7 about here.]

[Fig. 8 about here.]

V. Conclusion

Schottky S/D's can offer significantly improved performance over doped S/D's in $L_{nom} =$ 25 nm single-gate FDSOI and dual-gate CMOS. In each case, a large role is played by the

[12] This omission has negligible effect on the transient response of these devices. Small shifts in the inversion charge centroid tend to shift capacitance and current in proportion, resulting in compensating effects on device-loaded circuit speed. For the same reason, vertical mesh refinement is somewhat less important in the device-loaded transient response than it is in a current-voltage curve. The density gradient method is important for setting Φ_G based on a leakage current constraint, however.

[13] These values were chosen instead of 50% to reward robust switching characteristics; thermionic source/drain barriers can yield an undesired “tail” to the transitions.

metal/semiconductor interface. For the full potential of the Schottky S/D to be realized, the thermionic barrier from the metal to the silicon conduction band needs to be essentially eliminated and the S/D-to-gate separation needs to be optimized. Doped S/D technology must, in addition to overcoming the substantial challenge of achieving, controlling, and maintaining doping profiles with near-atomic-scale abruptness, reduce S/D specific contact resistivity well beyond the ITRS Roadmap schedule to be competitive with near-zero-barrier metal S/D devices.

VI. Acknowledgments

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List of Figures

1 Schematic half cross-sections of NFETs : (a) and (b) : Single-gate FDSOI; (c) and (d) : Dual-gate; (a) and (c) : doped S/D; (b) and (d) : metal S/D. Key dimensions are shown in either main figure or insets. Only the "top" half of dual-gate devices are shown; the "bottom" is a reflection about the reflection plane. 16

2 Tuned gate workfunction for various NFETs. Metal S/D FETs have similar "short-channel" characteristics as doped S/D counterparts if an offset is applied to the S-to-D separation, with metal S/D further apart. This is due to carrier depletion in the doped S/D, which is to approximately $x_{SD} + 1\,\mathrm{nm}$ with subthreshold V_{GS} and low V_{DS}. Doped S/D offset x_{SD} is measured to the edge of the doping peak, rather than to the metallurgical junction. The use of the latter would increase the difference with the metal S/D. 17

3 Device optimization is a tradeoff between managing short channel effects via greater source-drain separation and reducing resistance via a closer S/D placement. As extension length is increased, the V_T *vs.* L curve flattens (b right), which retains more performance at $L = L_{sup}$ for Φ_G set based on leakage at $L = L_{sub}$ (a). Setting Φ_G based on leakage at $L = L_{sup}$, neglecting V_T roll-off, yields a preference for short extensions (b left). For single-gate FDSOI, the V_T roll-off is substantial, and the optimum I_t is near $L_x = 3.9\,\mathrm{nm}$. Dual-gate MOSFET gate control is stronger, and thus with these devices the resistance advantage of a smaller L_x can be exploited. In (b), V_T is the V_G at $I_D = 100\,\mathrm{nA}/\mu\mathrm{m}$, $V_D = 1\,\mathrm{V}$. 18

4 I_D-V_G curves for $L = L_{sup}$ single-gate FDSOI devices with optimized x_{SD} (doped S/D) or L_x (metal S/D), and Φ_G set to yield $I_D = 20\,\mathrm{nA}/\mu\mathrm{m}$ for $L = L_{sub}$ at $V_D = 1\,\mathrm{V}$, $V_G = 0$. The drive current loss with increasing ρ_{SD} (a and b) and S/D barrier (c and d) is evident. 19

5 Benchmark results for devices with optimized x_{SD} (doped S/D) or L_x (metal S/D) for a range of metal/silicon interface parameters. A minimum value is set at $L_x = 3\,\mathrm{nm}$. 20

6 Schematic of 2-input NAND Test Circuit. FET widths (W) are in arbitrary units. The FETs and the capacitor all have $L = L_{sup}$. 21

7 Rising edge responses for 2-input NAND test circuit with doped or metal S/D CMOS. Single-gate (FD) and double-gate (DG) metal S/D circuits are each faster than either of the doped S/D versions. 22

8 Delays extracted from NAND-chain transient response of single-gate FDSOI ($t_{Si} = 4\,\mathrm{nm}$) and dual-gate ($t_{Si} = 5\,\mathrm{nm}$) CMOS show an approximate 45% advantage to metal S/D. Net delay is the sum of rising and falling edge delays. DSD: Doped S/D; MSD: Metal S/D; MN,DP: Metal S/D on NFETs and doped S/D on PFETs. Devices same as Table III. 23

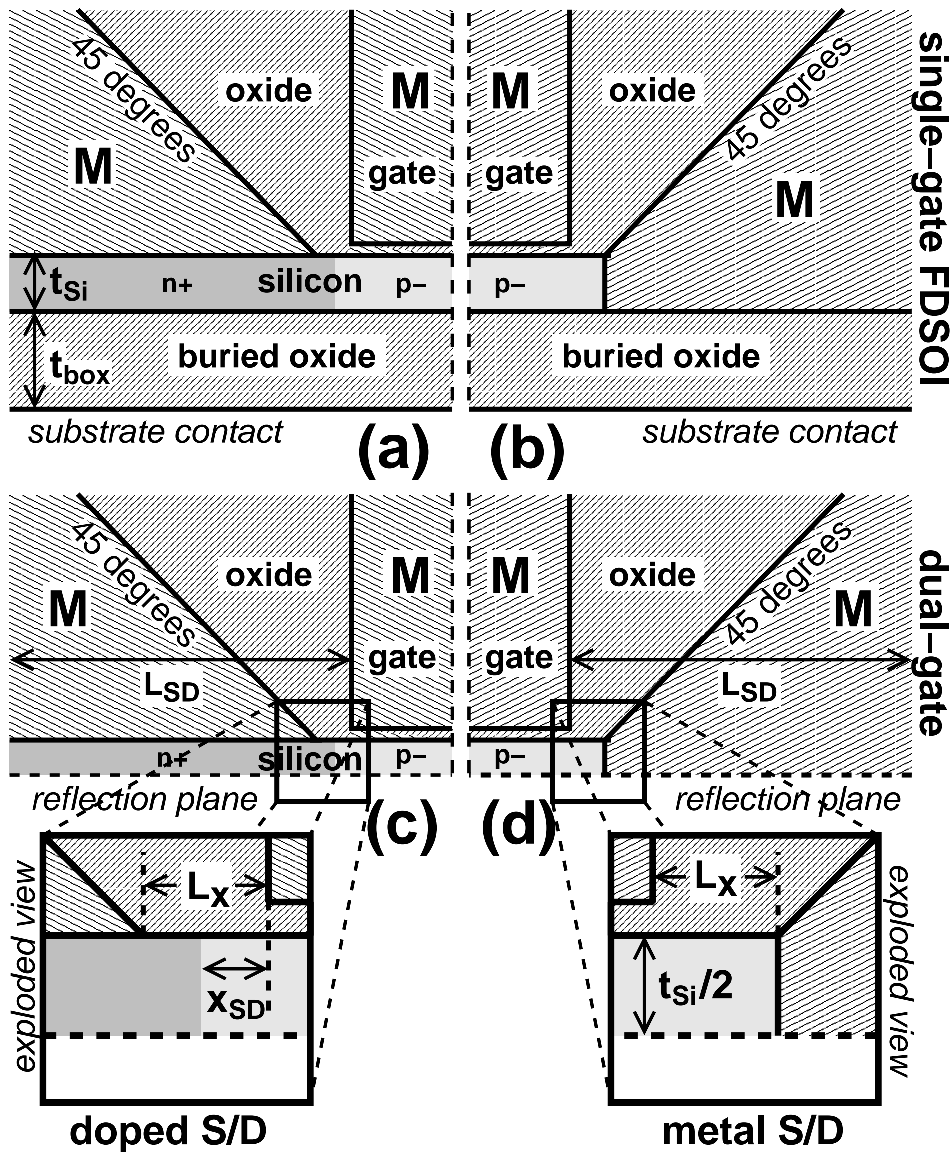

Fig. 1. Schematic half cross-sections of NFETs : (a) and (b) : Single-gate FDSOI; (c) and (d) : Dual-gate; (a) and (c) : doped S/D; (b) and (d) : metal S/D. Key dimensions are shown in either main figure or insets. Only the “top” half of dual-gate devices are shown; the “bottom” is a reflection about the reflection plane.

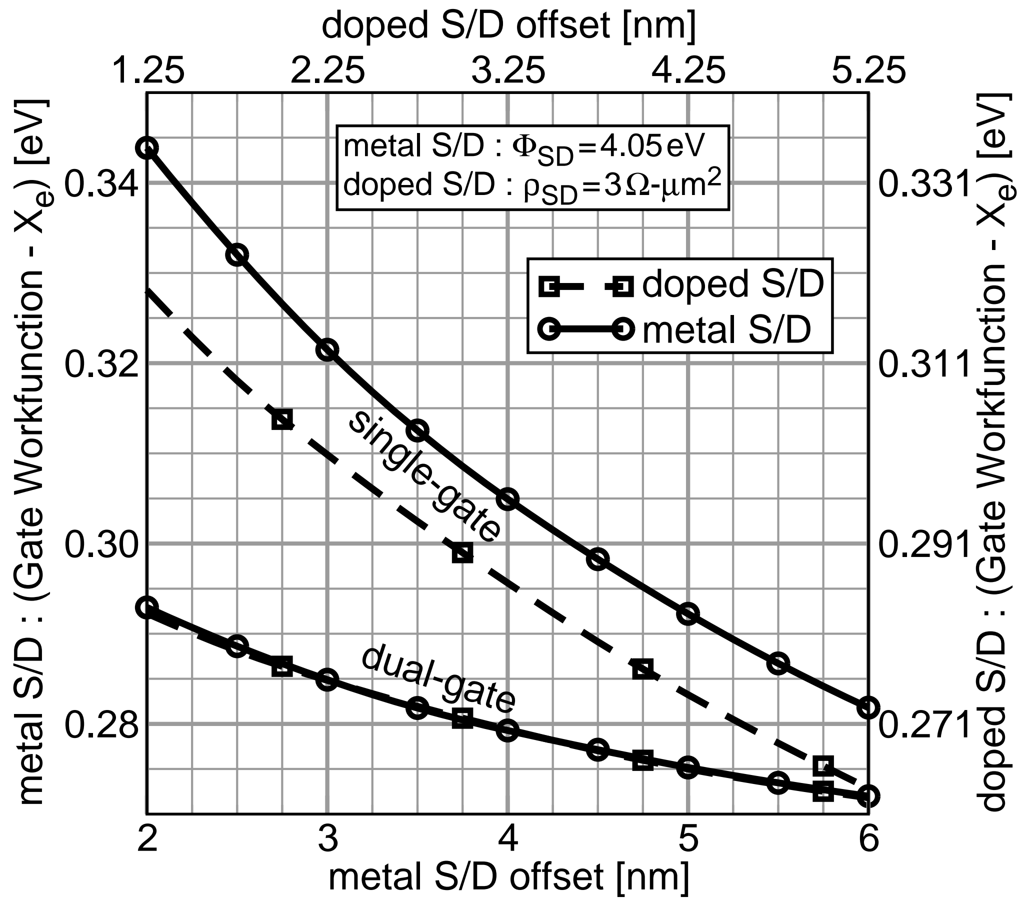

Fig. 2. Tuned gate workfunction for various NFETs. Metal S/D FETs have similar "short-channel" characteristics as doped S/D counterparts if an offset is applied to the S-to-D separation, with metal S/D further apart. This is due to carrier depletion in the doped S/D, which is to approximately $x_{SD} + 1\,\mathrm{nm}$ with subthreshold V_{GS} and low V_{DS}. Doped S/D offset x_{SD} is measured to the edge of the doping peak, rather than to the metallurgical junction. The use of the latter would increase the difference with the metal S/D.

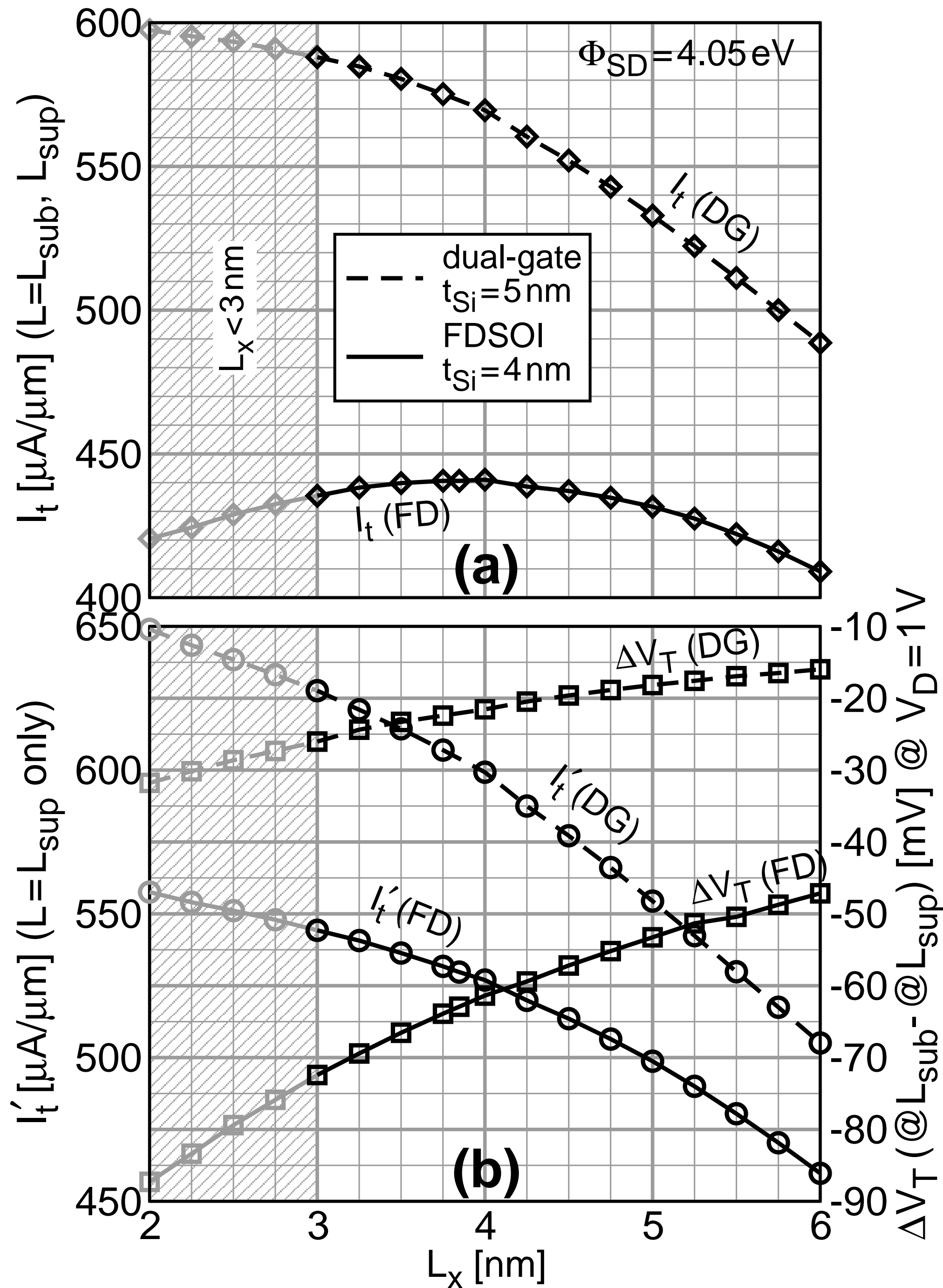

Fig. 3. Device optimization is a tradeoff between managing short channel effects via greater source-drain separation and reducing resistance via a closer S/D placement. As extension length is increased, the V_T *vs.* L curve flattens (b right), which retains more performance at $L = L_{sup}$ for Φ_G set based on leakage at $L = L_{sub}$ (a). Setting Φ_G based on leakage at $L = L_{sup}$, neglecting V_T roll-off, yields a preference for short extensions (b left). For single-gate FDSOI, the V_T roll-off is substantial, and the optimum I_t is near $L_x = 3.9\,\text{nm}$. Dual-gate MOSFET gate control is stronger, and thus with these devices the resistance advantage of a smaller L_x can be exploited. In (b), V_T is the V_G at $I_D = 100\,\text{nA}/\mu\text{m}$, $V_D = 1\,\text{V}$.

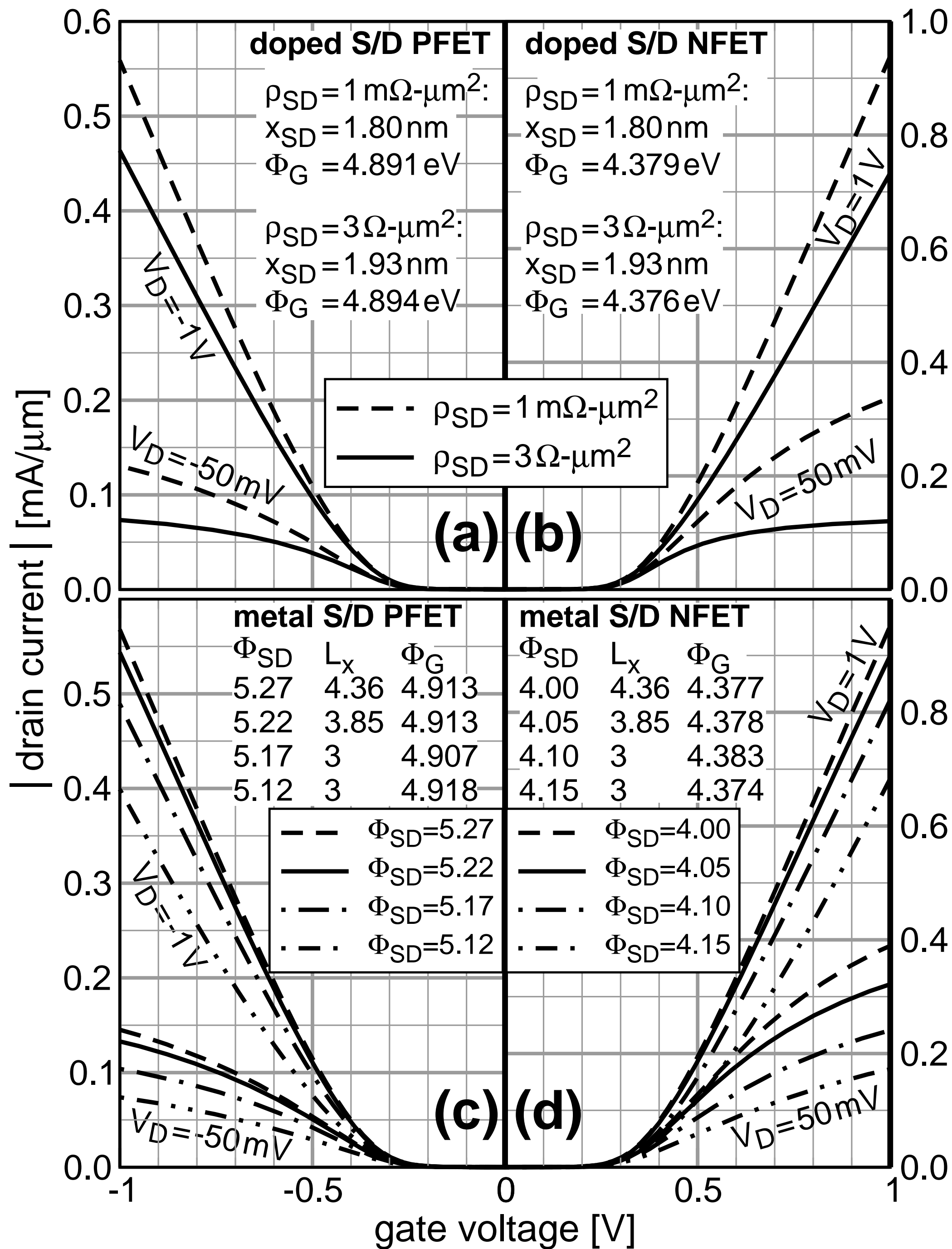

Fig. 4. I_D-V_G curves for $L = L_{sup}$ single-gate FDSOI devices with optimized x_{SD} (doped S/D) or L_x (metal S/D), and Φ_G set to yield $I_D = 20\,\text{nA}/\mu\text{m}$ for $L = L_{sub}$ at $V_D = 1\,\text{V}$, $V_G = 0$. The drive current loss with increasing ρ_{SD} (a and b) and S/D barrier (c and d) is evident.

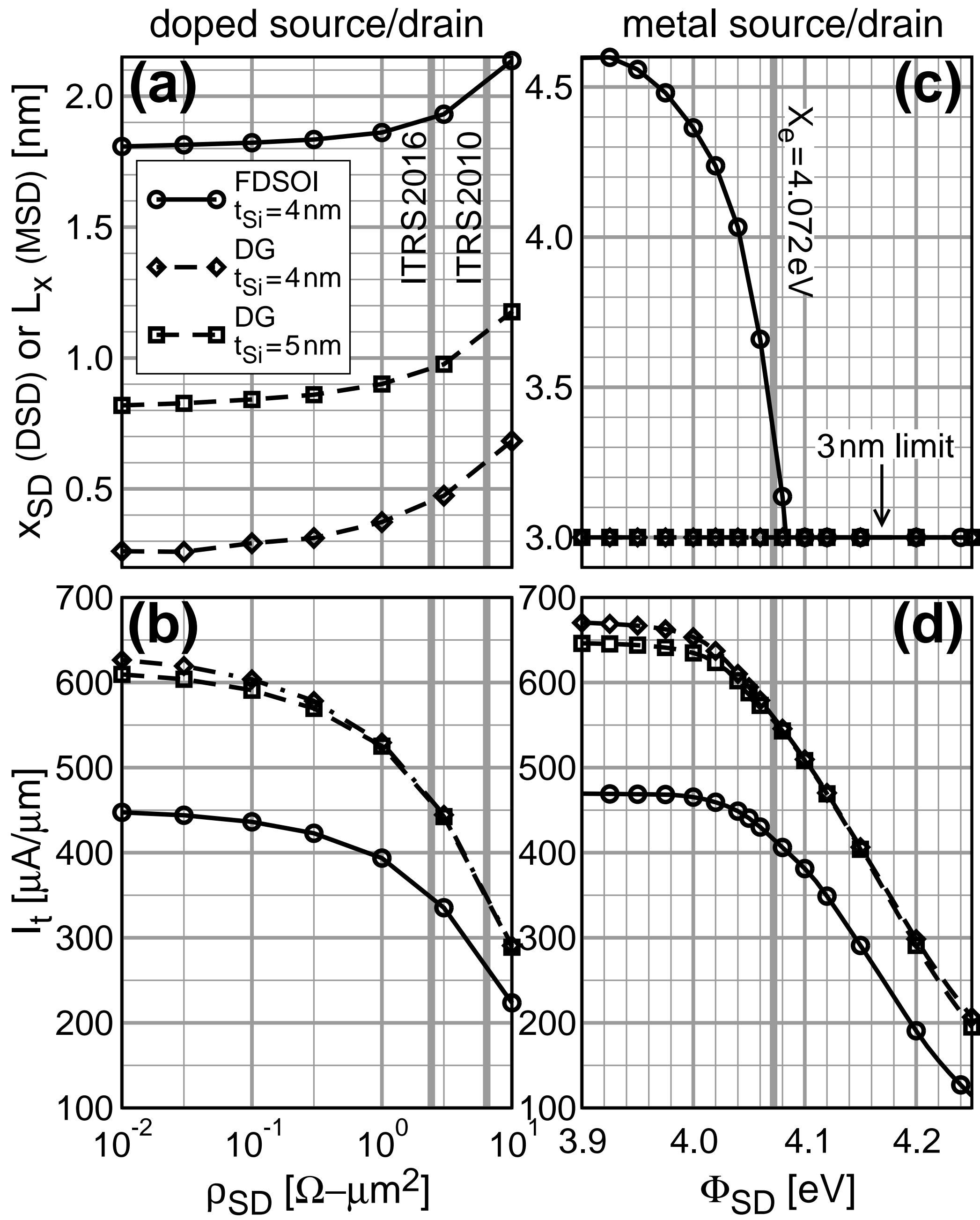

Fig. 5. Benchmark results for devices with optimized x_{SD} (doped S/D) or L_x (metal S/D) for a range of metal/silicon interface parameters. A minimum value is set at $L_x = 3\,\text{nm}$.

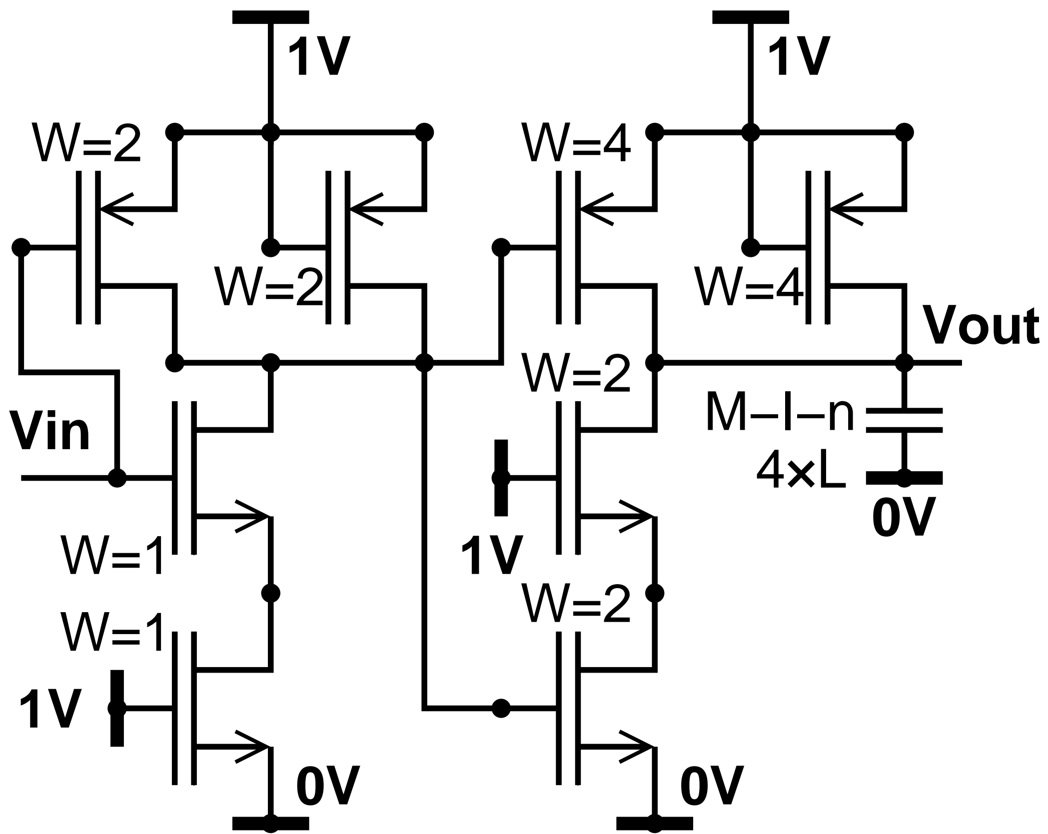

Fig. 6. Schematic of 2-input NAND Test Circuit. FET widths (W) are in arbitrary units. The FETs and the capacitor all have $L = L_{sup}$.

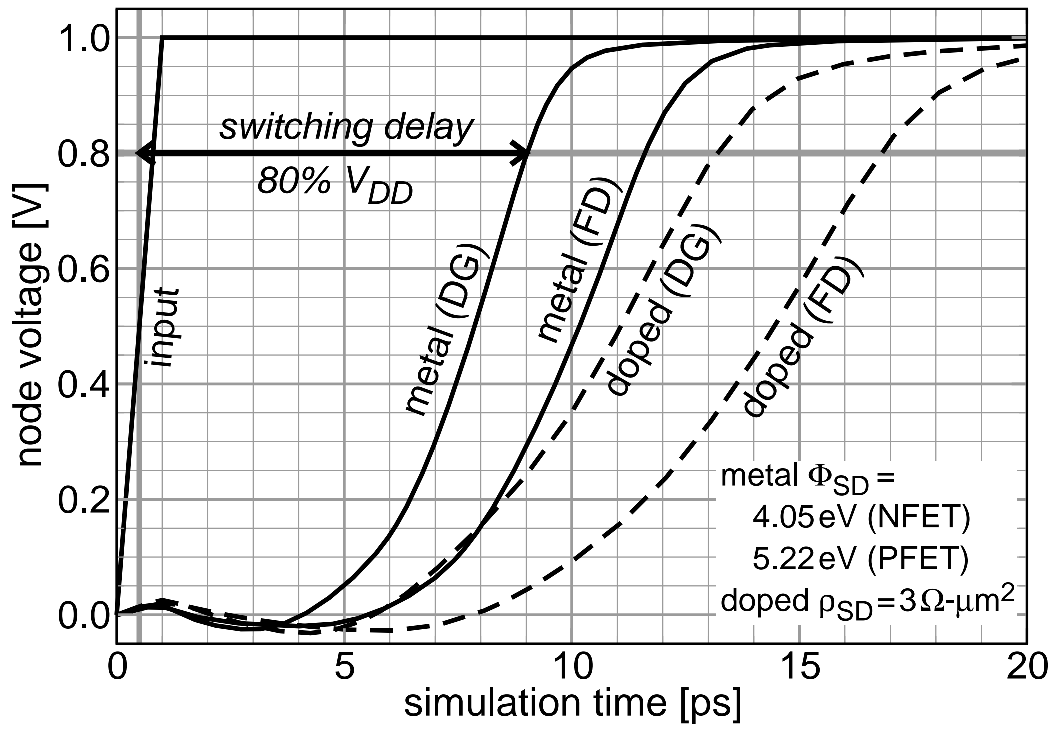

Fig. 7. Rising edge responses for 2-input NAND test circuit with doped or metal S/D CMOS. Single-gate (FD) and double-gate (DG) metal S/D circuits are each faster than either of the doped S/D versions.

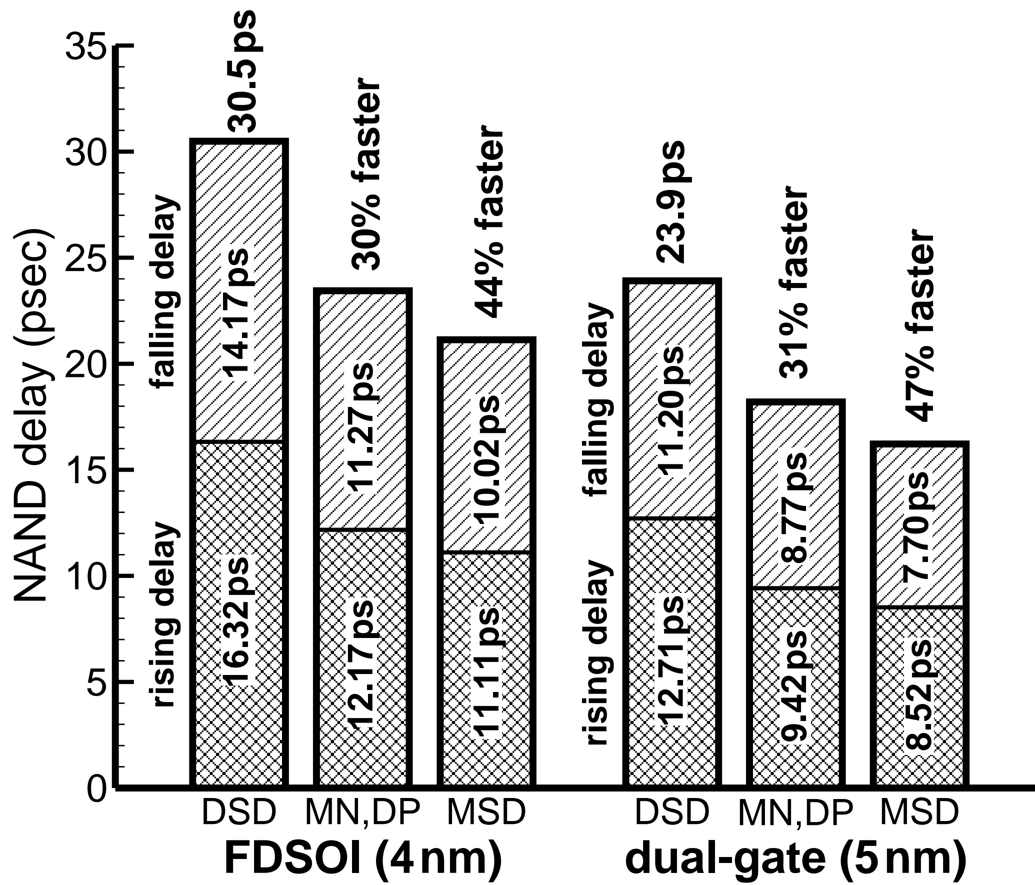

Fig. 8. Delays extracted from NAND-chain transient response of single-gate FDSOI ($t_{Si} = 4\,\text{nm}$) and dual-gate ($t_{Si} = 5\,\text{nm}$) CMOS show an approximate 45% advantage to metal S/D. Net delay is the sum of rising and falling edge delays. DSD: Doped S/D; MSD: Metal S/D; MN,DP: Metal S/D on NFETs and doped S/D on PFETs. Devices same as Table III.

List of Tables

I NFET parameters; PFET parameters analogous 25
II Device Benchmark Components 26
III Discrete device I_t comparison 27

p	*value(s)*	*description*
L_{nom}	25 nm	gate length of nominal device
L_{SD}	25 nm	length of S/D contact
L_{sub}	21 nm	subnominal gate length L
L_{sup}	33 nm	supernominal gate length L
L_x	3 to 6 nm	gate edge to S/D contact
N_{Si}	$10^{15}/\text{cm}^3$	acceptor concentration in Si
N_{SD}	$10^{20}/\text{cm}^3$	DSD peak donor conc. @ y_{SD}
Φ_G	*tuned*	workfunction of gate
Φ_{SD}	$X_e + \Delta\Phi_{SD}$	MSD effective workfunction
$\Delta\Phi_{SD}$	*variable*	MSD effective "barrier"
Φ_{sub}	4.6 eV	workfunction of FD substrate
ρ_{SD}	*variable*	specific contact resistivity to DSD
σ_L	4 nm	standard deviation of gate length
σ_{SDx}	1.6 nm	DSD lateral Gaussian param.
σ_{SDy}	2 nm	DSD depth Gaussian param.
t_{box}	10 nm	thickness of buried oxide of FD
t_{gate}	20 nm	thickness of gate
t_{ox}	1 nm	gate oxide thickness
t_{Si}	4 or 5 nm	full thickness of silicon
x_{SD}	-2 to 6 nm	offset of DSD peak from gate edge
y_{SD}	1 nm	depth of DSD Gaussian profile(s)

DSD : Doped S/D; *MSD* : Metal S/D; *FD* : Single-gated SOI

TABLE I

NFET parameters; PFET parameters analogous

<table>
<tr><th>p</th><th>L</th><th>Φ_G</th><th>V_D [V]</th><th>V_G [V]</th><th>$value$</th></tr>
<tr><td>I_{tlin}</td><td rowspan="3">L_{sup}</td><td rowspan="2">$tuned$ $@L_{sub}$</td><td>0.05</td><td rowspan="2">0.70</td><td rowspan="2">I_D</td></tr>
<tr><td>I_{tsat}</td><td>1.00</td></tr>
<tr><td>I_t</td><td colspan="4">see (2)</td></tr>
</table>

TABLE II
DEVICE BENCHMARK COMPONENTS

type:	FDSOI		dual-gate			
t_{Si}:	4 nm		4 nm		5 nm	
N/P:	N	P	N	P	N	P
DSD:	335	205	444	291	442	289
MSD:	441	251	595	358	588	357
ratio:	1.31	1.22	1.34	1.23	1.33	1.24

I_t ("DSD" and "MSD") in μA/μm
doped S/D: $\rho_{SD} = 3\,\Omega$-μm^2
metal S/D: $\Phi_{SD} = 4.05$ eV (NFET), $\Phi_{SD} = 5.22$ eV (PFET)

TABLE III
Discrete device I_t comparison