Performance Analysis and Hardware-In-the-Loop (HIL) Validation of Single Switch High Voltage Gain DC-DC Converters for MPP Tracking in Solar PV System

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ABSTRACT This article presents a high-gain DC-to-DC converter with a single switch, called the cubic converter, which provides very high voltage gain compared to the existing topologies such as the quadratic converter and conventional boost converter. The operation of the proposed converter at a lower duty ratio ensures lesser conduction losses. Various mathematical approaches are employed to confirm the higher voltage gain and improved efficiency of the converter. The proposed cubic boost converter (CBC) is compared with the quadratic boost converter (QBC) and other converters discussed in the literature. A generalized nth-order boost converter is also derived. To test the effectiveness of the QBC and CBC circuits, the Hardware-In-the-Loop (HIL) validation is performed using Typhoon HIL 402 real-time emulator machine. Moreover, the proposed topology is tested and compared with other topologies for maximum power point tracking (MPPT) of a solar photovoltaic (PV) array to show its effectiveness in a real-world scenario. A detailed comparison between conventional boost, QBC and CBC is presented for dynamic partial shading conditions in real-time mode using Typhoon HIL 402 real-time emulator machine.

INDEX TERMS DC-dc converter, high voltage gain, renewable energy, boost converter.

LIST OF ACRONYMNS

ABC: Artificial Bee Colony
CBC: Cubic Boost Converter
DC: Direct Current
HFT: High Frequency Transformer
HIL: Hardware-In-the-Loop
HVDC: High Voltage Direct Current
MPP: Maximum Power Point
MPPT: Maximum Power Point Tracking
PV: Photovoltaic
PSO: Particle Swarm Optimization
QBC: Quadratic Boost Converter
SC: Switched Capacitor
V-D: Voltage vs Duty ratio

I. INTRODUCTION

Power electronic converters play an important role in the field of renewable energy because they provide an interface between renewable energy sources and the electrical power system. Their optimal utilization can improve the power transfer from renewable energy sources in terms of achieving the desired output at higher efficiency and reduced manufacturing cost [1]–[5]. Power electronic converters have a

wide applicability in electrical systems such as in the maximum power point tracking of a solar photovoltaic (PV) array, charging and discharging of batteries, high-voltage DC transmission, electric drive trains, street lightning, satellites, AMOLED, and electric vehicles [6].

The voltage provided by a solar PV array is comparatively low and depends on the environmental factors [7]. In order to achieve high output voltage values out of PV systems they are configured in a series parallel combination, which results in lowering down of efficiency and large size of the system [8], [9]. For such voltage-boosting applications, a high-gain boost converter is employed that can increase voltage at the output to much higher values with respect to its input by adjusting the duty cycle of the converter. The general architecture of a DC grid system employed with a DC-DC boost converter is shown in figure 1. Consequently, numerous topologies of these types of converters have been proposed in the literature in order to obtain the desired output voltage [3], [4], [6] and [9]–[14]. These topologies are divided into various categories such as isolated/non-isolated, unidirectional/bidirectional, voltage-fed/current-fed, hard-switched/soft-switched and minimum-phase/non-minimum-phase.
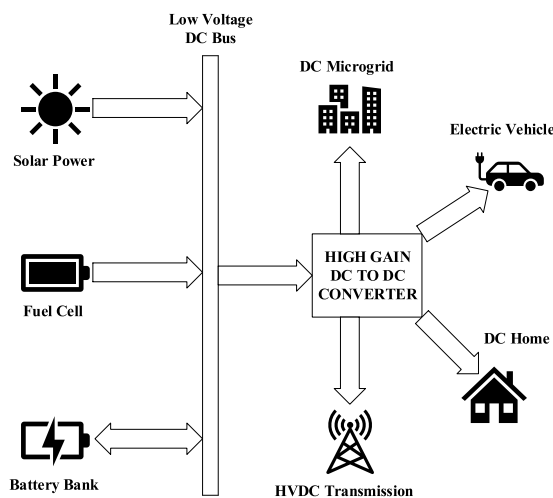

FIGURE 1. DC-energy system.

In an isolated converter topology, a high-frequency transformer (HFT) is employed to boost the input voltage by adjusting its turns ratio [10]. However, these converters have high ripple content in the input current and high voltage stress at the secondary side [11]. Additionally, leakage energy, bulky transformer and the multistage power conversion process are the main drawbacks of the isolated converters [12]. Consequently, non-isolated converters are being used for improvising performance of the system. Various topologies of this type have been proposed in the literature [2]–[4], [13], [14] and [16]–[19]. These converters are widely used since they are simple, less expensive, efficient and broadly applicable [6]. One such example is the conventional DC-DC boost converter, which is a less complicated

and less expensive topology that is being widely used in practical applications and in almost all the literature describing maximum power point tracking (MPPT). However, this topology cannot provide a sufficiently high voltage gain for some applications [15], [16]. Theoretically, in this arrangement the voltage gain can reach infinitely higher values at its highest duty ratio but practically the output voltage is limited due to the leakage resistance in the inductor-charging loop [16], [18]. Moreover, a very high duty ratio is required by this type of converter to produce high voltages ratios, and can reach very high values of about 0.8, 0.9 thereby resulting in high losses, lower efficiency and higher voltage and current stress on the device [18], [19]. For this reason, the conventional boost converter is not used for applications requiring a duty ratio more than a certain limit.

One way to eliminate this issue is to make use of small reactive components by increasing the converter's switching frequency up to the extent where the ripples are acceptable [15]. Various researchers have shown that making use of small reactive elements reduces the leakage resistance [16], [18], [20]–[22]. Nevertheless, for very high or very low values of duty ratio, the switching frequency is limited due to the finite switching time in actual power semiconductors [15].

Considering these issues, the coupled inductor as an element was introduced that was able to improve the transformation ratio. But these devices produced leakage inductance that caused high voltage spikes across the switching devices [23]. In [24], a single-stage boost converter topology is introduced that is based on switched capacitor (SC) circuits. Its operation on the basis of parallel-charging-series-discharging principle was helpful in voltage amplification. It had the capability of working as a boost converter and with significantly reduced current ripples at the input and the much lower voltage stress on the semiconductors [15]. However, it achieved a voltage gain only twice that of a conventional boost converter which was not sufficient for most of the large voltage applications thereby causing the high duty ratio problem [15].

Cascaded converters [25]–[27] were designed to eliminate high duty ratio problems. They were constructed by joining two boost converters in series. These converters, although expensive, were able to provide very high voltage gains at the output at lower duty ratio values when compared with the conventional ones [25], [26]. The voltage stress in these types of converters was low and hence can be operated at higher frequencies in their first stage thereby benefiting from high power density [6]. In contrast, its second stage can be operated at lower frequencies to reduce switching losses [6]. An improved version of this configuration was the quadratic boost converter in which the number of switches was reduced to one in order to reduce the complexity [6]. The cascaded boost converter, although able to produce high voltages at lower duty ratio values, suffered from lesser efficiency due to the power being processed multiple times and extra effort and complicated control are needed to stabilize the system [28], [29].

The duty ratio problem can be eliminated by using transformers that step-up the voltages without any switching [15]. The literature contains many such transformer-based topologies that eliminate duty ratio issues [30]–[35]. In these literatures, the topologies based on coupled inductor were proposed. The output voltage of the converter was increased to very higher values without causing any duty ratio related issues. However, in transformers the losses increase with the increase in frequency [15]. Apart from high voltage gains at lower duty ratio values efficiency also play an important role in the overall improvement of the system's performance. A system producing sufficiently higher voltages but at the cost of lower efficiencies will not be reliable unless efficiency has no significance for such type of a system. The quadratic converter produced higher gains at higher efficiencies when compared with the conventional, however at higher loads its efficiency was significantly reduced.

In this article a new converter, called the cubic converter, is proposed in order to reduce the issues with the existing topologies. The proposed topology is compared with the quadratic boost converter in terms of output gain values with and without the effect of internal resistance of inductors using a voltage versus duty ratio (V-D) graph. Moreover, a hardware-in-loop comparison was also performed between the topologies under ideal conditions (neglecting internal resistance). The proposed converter outperforms the existing quadratic converter in terms of:

- Producing much higher voltage gains at the same duty ratio value (mathematical modelling of both the converters is provided for verification of results).
- Producing higher efficiencies at increased loads.

Additionally, to validate further the performance of the proposed topology and to show its usefulness in the practical world it was used for maximum power point tracking (MPPT) of a Solar PV array. The proposed converter was compared with the quadratic and the conventional boost converters. The proposed topology successfully outperformed both the topologies in terms of tracking the same maximum power point (MPP) but at a reduced duty ratio value thereby reducing conduction losses and increasing the efficiency.

The following sections are structured as follows: Section II describes the quadratic boost converter and its operation; section III describes the cubic boost converter and its operation; section IV is the comparative analysis between quadratic and the cubic converter in terms of high-voltage gain and efficiency; and section V provides solar MPPT using the cubic converter, managerial implications and conclusions are presented in section VI and VII respectively.

II. PERFORMANCE ANALYSIS OF THE QUADRATIC BOOST CONVERTER WITH REAL-WORLD PARAMETERS

To explain the steady-state operation of the quadratic boost converter, all components are assumed to be ideal. The converter's output voltage is controlled by a single switch S, which means the converter will have two modes of operation.

During the first mode of operation, the switch 'S' is in the ON condition as shown in figure 2 (b) and during the second mode of operation, the switch is in the OFF condition as shown in figure 2 (c).
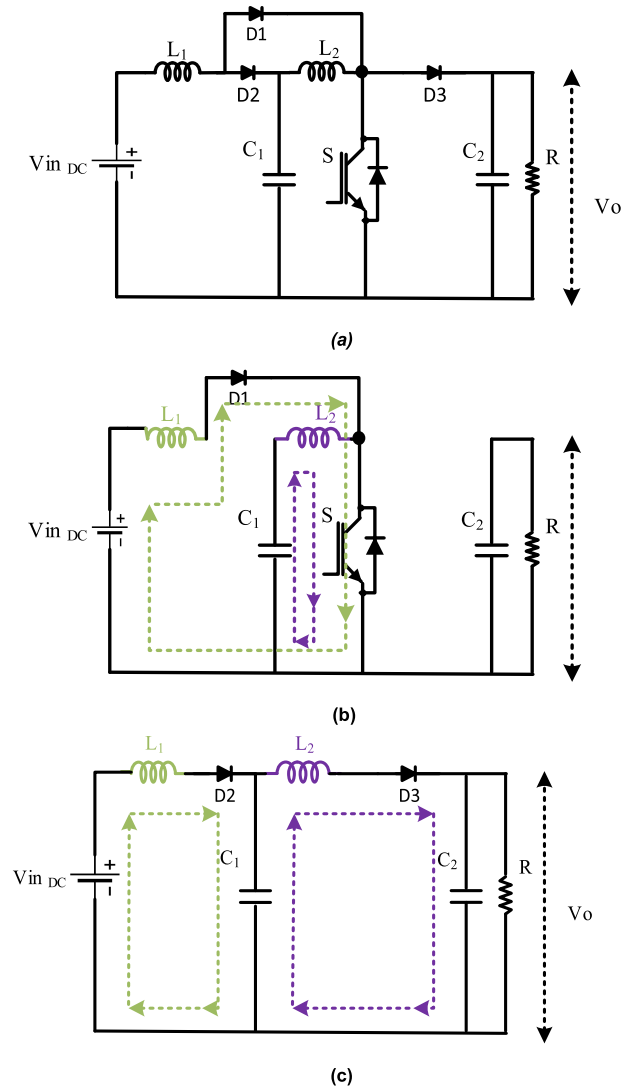

(a)

(b)

(c)

FIGURE 2. Circuit diagram of (a) the quadratic boost converter, (b) first mode of operation and (c) second mode of operation.

A. MODE-1 (0 to DT)

During the first mode of operation, switch S is in the ON condition and diode D1 is conducting, while the diodes D2 and D3 are reversed-biased. The switch S is conducting for an interval of DT where D is the duty ratio and T is the time period of the switching signal. The voltage across the inductor L_1 and L_2 during this mode of operation can be obtained by applying KVL as shown in figure 2 (b). As given in (1) and (2) the voltage across the inductors 1 and 2 are *Vin* and V_{C1} respectively.

$$VL_1 = Vin \qquad (1)$$

$$VL_2 = V_{C1} \qquad (2)$$

B. MODE-2 (DT to T)

During this mode of operation, the switch is in the OFF condition and the diodes D2 and D3 are conducting while diode D1 is reverse-biased. The voltage equations for inductors L_1 and L_2 can be obtained by using figure 2 (c) as given below.

$$VL_1 = Vin - V_{C1} \tag{3}$$

$$VL_2 = V_{C1} - V_{C2} \tag{4}$$

$$VL_2 = V_{C1} - Vo \tag{5}$$

Equations (3), (4) and (5) shows the voltages across the inductors L_1 and L_2 respectively for second mode of operation.

Now applying Volt-Sec balance across inductor L_1 using equation (6) we get:

$$\int_0^T VL_1(t) \, dt = 0$$
$$Vin \times DT + (Vin - V_{C1}) \times (1 - D) \, T = 0 \tag{6}$$

$$V_{C1} = \frac{Vin}{(1-D)} \tag{7}$$

where the equation represents the voltage across the capacitance C_1.

Now applying Volt-Sec balance across Inductor L_2 using (8) we get:

$$\int_0^T VL_2(t) \, dt = 0$$
$$V_{C1} \times DT + (V_{C1} - Vo) \times (1 - D) \, T = 0 \tag{8}$$

$$Vo = \frac{V_{C1}}{1-D} \tag{9}$$

where (9) represents the output voltage.

Now, putting the value of V_{C1} in terms of input DC voltage from (7) we get (10) as follows:

$$Vo = \frac{Vin}{(1-D)^2} \tag{10}$$

C. DESIGNING OF INDUCTOR

When the switch is ON the expression for the voltage across the inductor L_1 equal to the input voltage is given in (11). The expression for the change in current is given in (12). Therefore, the expression for the minimum current across the inductor L_1 is given in (13).

$$L_1 \frac{dI_{L1}}{dt} = Vin$$
$$\frac{dI_{L1}}{dt} = \frac{Vin}{L_1} \tag{11}$$

$$\Delta I_{L1} = \frac{VinDT}{L_1} \tag{12}$$

$$(I_{L1})_{Min} = I_{L1} - \frac{\Delta I_{L1}}{2} \tag{13}$$

The average current flowing through the output diode is the same as that of the output current, therefore:

$$I_{D3} = Io = \frac{Vo}{R} \tag{14}$$

Diode D3 and D2 are conducting only when the switch is OFF, therefore:

$$I_{D3} = (1 - D) \times I_{L2} \tag{15}$$

$$I_{L2} = \frac{Vo}{R(1-D)}$$

$$I_{D2} = I_{L2} = (1 - D) \times I_{L1} \tag{16}$$

$$I_{L1} = \frac{Vo}{R(1-D)^2} \tag{17}$$

After combining equations (12), (13) and (17) we get:

$$(I_{L1})_{Min} = \frac{Vin}{R(1-D)^4} - \frac{VinDT}{2L_1} \tag{18}$$

For continuous mode conduction, the minimum inductor current should be greater than zero that is

$$\frac{Vin}{R(1-D)^4} - \frac{VinDT}{2L_1} \geq 0 \tag{19}$$

$$\frac{Vin}{R(1-D)^4} \geq \frac{VinDT}{2L_1} \tag{20}$$

$$L_1 \geq \frac{R(1-D)^4 D}{2f_s} \tag{21}$$

Similarly, the voltage across the inductor L_2 is equal to the capacitor voltage V_{C1}, and therefore the minimum inductance of inductor 2 for the continuous mode conductions can be calculated using equation (22)

$$L_2 \geq \frac{R(1-D)^2 D}{2f_s} \tag{22}$$

The value of the inductor depends on the duty ratio, load resistance, and the switching frequency.

D. DESIGNING OF CAPACITORS

The charge stored by a capacitor can be written as given in equations (23)

$$Q = CV_C \tag{23}$$

$$\Delta Q = C\Delta V_C \tag{24}$$

$$I_C \Delta T = C\Delta V_C \tag{25}$$

When the switch is ON:

$$I_{C1} = I_{L2} = \frac{Vo}{R(1-D)} \tag{26}$$

Substituting the value of I_{C1} and V_{C1} in equation (26), we obtain (27) and (28):

$$\frac{VoDT}{R(1-D)} = C_1 \Delta V_{C1} \tag{27}$$

$$C_1 \Delta V_{C1} = \frac{VoDT}{R(1-D)} \tag{28}$$

Now replacing the value of *Vo* in terms of input voltage we get C_1 as in equation (29):

$$C_1 = \frac{VinD}{R(1-D)^3 \Delta V_{C1} f_s} \tag{29}$$

Similarly,

$$I_{C2} = I_0 = \frac{Vo}{R} \tag{30}$$

Substituting the value of I_{C2} and V_{C2} in equation (30), we get:

$$C_2 \Delta V_{C2} = \frac{VoDT}{R} \tag{31}$$

Now replacing the value of *Vo* in terms of input voltage we get C_2 as in equation (32):

$$C_2 = \frac{VinD}{R(1-D)^2 \Delta V_{C2} f_s} \tag{32}$$

E. POWER LOSSES IN THE CIRCUIT

The power loss in the converter circuit depends on various parameters such as the internal resistances of the components present in the converter, the forward voltage drop of the diode, and the switching frequency.

The power loss in the inductor is mainly due to its DC resistance. An equivalent power loss model of the inductor is represented in figure 3(a). The power losses in each inductor are as follows:

$$P_L = (I_{L_{rms}})^2 r_L \tag{33}$$

$$P_{L_1} = \frac{Vo^2 r_{L1}}{R^2(1-D)^4} \tag{34}$$

$$P_{L_2} = \frac{Vo^2 r_{L2}}{R^2(1-D)^2} \tag{35}$$

$$P_{L_{total}} = \frac{Vo^2 r_{L1}}{R^2(1-D)^4} + \frac{Vo^2 r_{L2}}{R^2(1-D)^2} \tag{36}$$

The losses in the capacitor are due to the presence of the series resistance as represented by the figure 3 (b), the losses due to each capacitor can be calculated as follows:

$$P_C = (I_{C_{rms}})^2 r_C \tag{37}$$

$$P_{C_1} = \frac{Vo^2 D r_{C1}}{R^2 (1-D)^3} \tag{38}$$

$$P_{C_2} = \frac{Vo^2 D r_{C2}}{R^2 (1-D)} \tag{39}$$

$$P_{C_{total}} = \frac{Vo^2 D r_{C1}}{R^2 (1-D)^3} + \frac{Vo^2 D r_{C2}}{R^2 (1-D)} \tag{40}$$

The main power losses in the diode during its conduction are due to the ON resistance of the diode as well as due to the forward voltage drop of the diode as given in Fig. 3 (c). The losses in the circuit due to the diode can be calculated as follows:

$$P_d = V_d I_{d_{ON}} \times conduction\ time + (I_{d_{rms}})^2 r_d \tag{41}$$

$$P_{d_1} = \frac{V_d Vo}{R(1-D)^2} \times D + \frac{Vo^2 D r_d}{R^2(1-D)^4} \tag{42}$$

$$P_{d_2} = \frac{V_d Vo}{R(1-D)} + \frac{Vo^2 r_d}{R^2(1-D)^3} \tag{43}$$

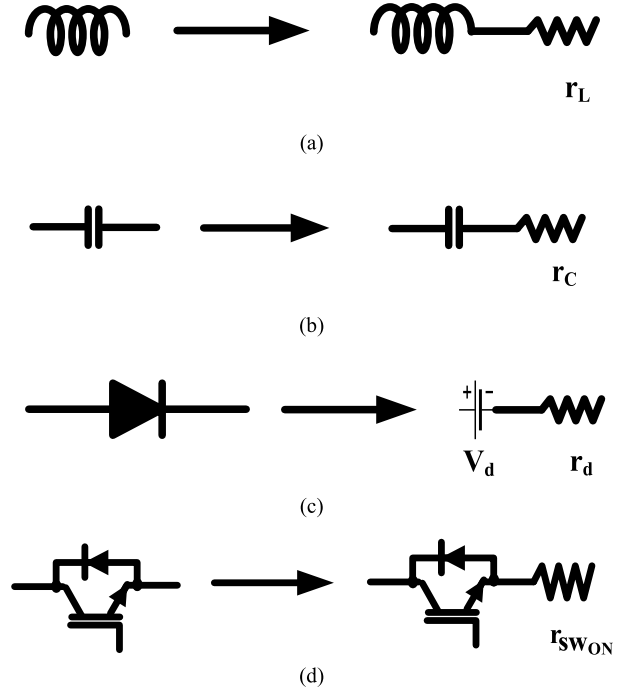$$P_{d_3} = \frac{V_d Vo}{R} + \frac{Vo^2 r_d}{R^2(1-D)} \tag{44}$$

FIGURE 3. Circuit diagram for loss calculation. (a) Inductor equivalent circuit. (b) Capacitor equivalent circuit. (c) Diode equivalent circuit. (d) Switch equivalent circuit.

$$P_{d_{total}} = \frac{V_d VoD}{R(1-D)^2} + \frac{V_d Vo}{R(1-D)} + \frac{V_d Vo}{R} + \frac{Vo^2 D r_d}{R^2(1-D)^4}$$
$$+ \frac{Vo^2 r_d}{R^2(1-D)^3} + \frac{Vo^2 r_d}{R^2(1-D)} \tag{45}$$

There are two types of power losses in the case of a switch, one is the conduction loss which depends upon the ON resistance of the switch. The other is the switching loss which depends on the switching frequency, so the total loss in the case of the switch as shown in Fig. 3 (d) can be calculated as follows:

$$P_{sw} = P_{sw_{Cond}} + P_{sw_{ON}} + P_{sw_{OFF}} \tag{46}$$

$$P_{sw_{Cond}} = I_{swrms}^2 r_{swON} \tag{47}$$

$$P_{sw_{Cond}} = \frac{Vo^2(2-D)^2 D}{R^2(1-D)^4} r_{swON} \tag{48}$$

$$P_{sw_{ON}} = 0.5 I_{sw_{ON}} V_{DD} \times \frac{t_{ri}+t_{fv}}{2} \times f_s \tag{49}$$

$$P_{sw_{ON}} = \frac{0.5 Vo^2(2-D)}{R(1-D)^2} \times \frac{t_{ri}+t_{fv}}{2} \times f_s \tag{50}$$

$$P_{sw_{OFF}} = \frac{0.5 Vo^2(2-D)}{R(1-D)^2} \times \frac{t_{fi}+t_{rv}}{2} \times f_s \tag{51}$$

where:
$\frac{t_{ri}+t_{fv}}{2}$ is the turn ON time.
$\frac{t_{fi}+t_{rv}}{2}$ is the turn OFF time.
f_s is the switching frequency.

F. NON-IDEAL VOLTAGE CALCULATION

The actual value of the output voltage depends upon the power losses in the circuit. Therefore, the actual output voltage can be determined by using the law of conservation of energy that is:

$$Input\ Power = Output\ Power + Losses \qquad (52)$$

$$Input\ Power = I_{L1}Vin \qquad (53)$$

$$Input\ Power = \frac{VoVin}{R(1-D)^2} \qquad (54)$$

$$Output\ Power = \frac{Vo^2}{R} \qquad (55)$$

After combining all the losses and inserting them into equation (52) we get the actual voltage as presented in equation (56), as shown at the bottom of the next page. The actual voltage depends on various factors but the main factor is the output load current. When the output current increases the overall loss in the circuit also increases, which decreases the voltage drop in the circuit that leads to a decrease in the actual output voltage. For a fixed output resistance, the load current increases with the increase in the duty ratio as the output voltage increases, therefore at higher values of the duty ratio the efficiency of the circuit decreases. After a particular duty ratio, the converter voltage starts to decrease with an increase in duty ratio: this is because at higher duty the losses in the circuits become very high.

G. HARDWARE-IN-THE-LOOP VALIDATION

For hardware-in-loop validation, the Typhoon Hardware-In-the-Loop (HIL) 402 Emulator was used. The results for the quadratic boost converter are provided in figure 4. It is seen in figure 4(a) that the voltage across capacitors C_1 and C_2 is 24 volts and 70 volts respectively. In figure 4(b) the current across the inductor L_1 is 10 amperes and the maximum and minimum value of current across the inductor L_2 is 2.2 amperes and 1.2 amperes respectively. In figure 4(c) the output voltage is boosted to 70 volts for an input voltage of 12 volts and a duty ratio of 0.6.

III. PERFORMANCE ANALYSIS OF THE PROPOSED CUBIC BOOST CONVERTER WITH REAL PARAMETERS

The output voltage control in a cubic boost converter given in figure 5(a) is a single switch operation similar to that of a quadratic converter. Hence, it has only two modes of operation which are described as follows.
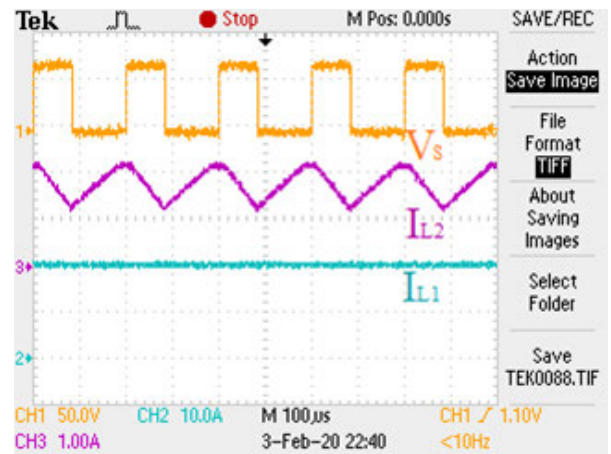
A. MODE-1 (0 to DT)

During the first mode of operation, switch S is in ON-condition diode D1 and D3 are conducting, D2, D4 and D5 diodes are reverse biased. The voltage across the inductor L_1, L_2, and L_3 during this mode of operation can be obtained by applying KVL as shown in figure 5(b).
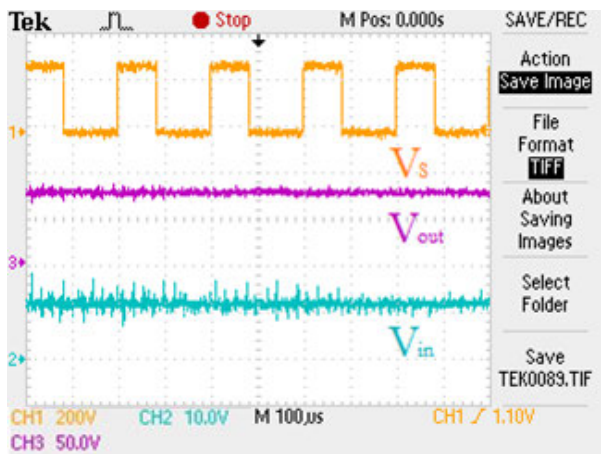
$$VL_1 = Vin \qquad (57)$$
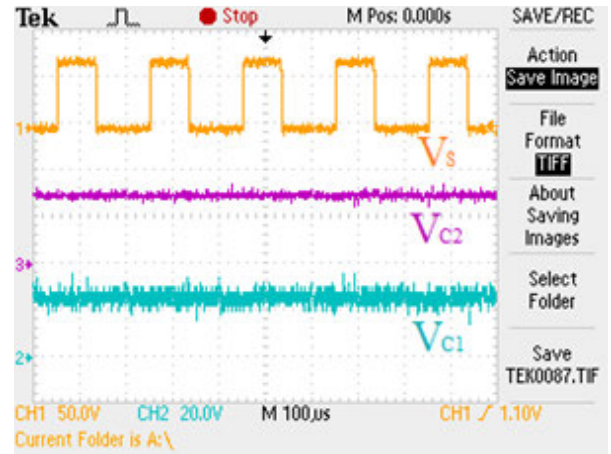
(a)

(b)

(c)

FIGURE 4. Hardware in Loop validation results for the quadratic boost converter for a duty ratio of 0.6. (a) the voltage across capacitors C_1 and C_2. (b) current across the inductor L_1 and L_2 (c) the input and output voltage.

$$VL_2 = V_{C1} \qquad (58)$$
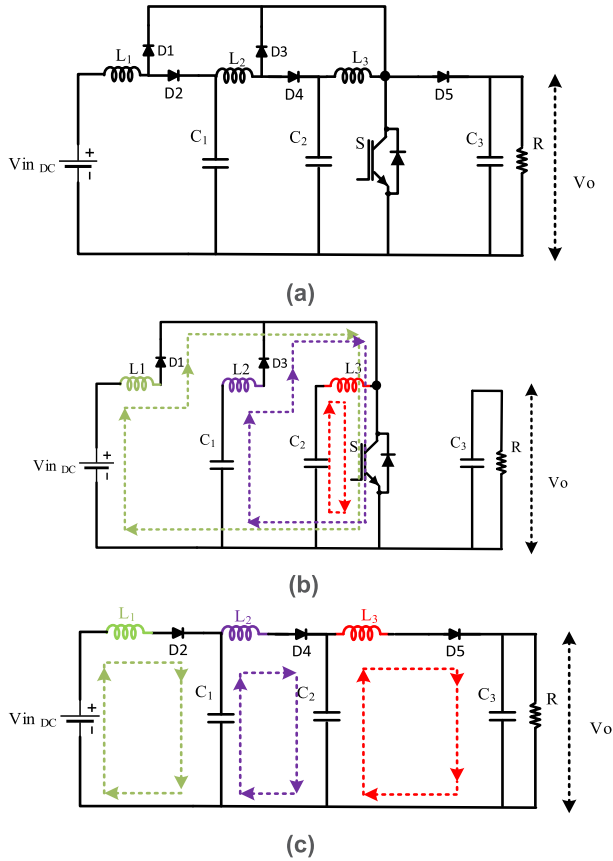
$$VL_3 = V_{C2} \qquad (59)$$

FIGURE 5. Circuit diagram of (a) the cubic boost converter, (b) first mode of operation and (c) second mode of operation.

B. MODE-2 (DT to T)

When switch S1 is in the OFF-condition diode D1 and D3 are reverse biased, D2, D4 and D5 diodes are conducting.

$$VL_1 = Vin - V_{C1} \qquad (60)$$

$$VL_2 = V_{C1} - V_{C2} \qquad (61)$$

$$VL_3 = V_{C2} - Vo \qquad (62)$$

Applying Volt-Sec balance across inductor L_1 in figure 5(c):

$$\int_0^T VL_1(t) \, dt = 0 \qquad (63)$$

$$Vin \times DT + (Vin - V_{C1}) \times (1-D) \, T = 0 \qquad (64)$$

$$Vin \times D + (Vin - V_{C1}) \times (1-D) = 0$$

$$Vin \times D + Vin - V_{C1} - Vin \times D + V_{C1} \times D = 0$$

$$V_{C1} - V_{C1} \times D = Vin$$

$$V_{C1}(1-D) = Vin$$

$$V_{C1} = \frac{Vin}{(1-D)} \qquad (65)$$

Now applying Volt-Sec balance across Inductor L_2:

$$\int_0^T VL_2(t) \, dt = 0 \qquad (66)$$

$$V_{C1} \times DT + (V_{C1} - V_{C2}) \times (1-D) \, T = 0$$

$$V_{C1} \times D + (V_{C1} - V_{C2}) \times (1-D) = 0$$

$$V_{C1} \times D + V_{C1} - V_{C2} - V_{C1} \times D + V_{C2} \times D = 0$$

$$V_{C2} - V_{C2} \times D = V_{C1}$$

$$V_{C2}(1-D) = V_{C1}$$

$$V_{C2} = \frac{V_{C1}}{1-D} \qquad (67)$$

Substituting the value of V_{C1} in terms of input DC voltage, we obtain:

$$V_{C2} = \frac{Vin}{(1-D)^2} \qquad (68)$$

Applying Volt-Sec balance across Inductor L_3:

$$\int_0^T VL_3(t) \, dt = 0$$

$$V_{C2} \times DT + (V_{C2} - Vo) \times (1-D) \, T = 0$$

$$V_{C2} \times D + (V_{C2} - Vo) \times (1-D) = 0$$

$$V_{C2} \times D + V_{C2} - Vo - V_{C2} \times D + Vo \times D = 0 \qquad (69)$$

$$Vo - Vo \times D = V_{C2}$$

$$Vo(1-D) = V_{C1}$$

$$Vo = \frac{V_{C2}}{1-D} \qquad (70)$$

Now putting the value of V_{C2} in terms of input DC voltage, we obtain:

$$Vo = \frac{Vin}{(1-D)^3} \qquad (71)$$

C. DESIGN OF INDUCTORS

When the switch is ON the voltage across the inductor L_1 is equal to the input voltage:

$$L_1 \frac{dI_{L1}}{dt} = Vin \qquad (72)$$

$$\frac{dI_{L1}}{dt} = \frac{Vin}{L_1}$$

$$\frac{\Delta I_{L1}}{DT} = \frac{Vin}{L_1}$$

Vo
$$= \frac{VinR(1-D)^2 - RVd(1-D)^2 \left\{ D + (1-D) + (1-D)^2 \right\}}{R(1-D)^4 + r_d \left\{ D + (1-D) + (1-D)^3 \right\} + r_{L1} + r_{L2}(1-D)^2 + r_{C1}D(1-D) + r_{C2}D(1-D)^2 + r_{swoN}(2-D)^3 + 0.5(1-D)^2(2-D)\left(\frac{t_{fi}+t_{rv}}{2} + \frac{t_{ri}+t_{fv}}{2} \right)f_s R} \qquad (56)$$

$$\Delta I_{L1} = \frac{VinDT}{L_1} \quad (73)$$

$$(I_{L1})_{Min} = I_{L1} - \frac{\Delta I_{L1}}{2} \quad (74)$$

The average current flowing through the output diode is the same as that of the output current, therefore:

$$I_{D5} = Io = \frac{Vo}{R} \quad (75)$$

Diode D2, D4 and D5 are conducting only when the switch is OFF, therefore:

$$I_{D5} = (1-D) \times I_{L3} \quad (76)$$

$$I_{L3} = \frac{Vo}{R(1-D)}$$

$$I_{D4} = (1-D) \times I_{L2} \quad (77)$$

$$I_{D4} = I_{L3} = (1-D) \times I_{L2} \quad (78)$$

$$(1-D) \times I_{L2} = \frac{Vo}{R(1-D)} \quad (79)$$

$$I_{L2} = \frac{Vo}{R(1-D)^2} \quad (80)$$

$$I_{D2} = (1-D) \times I_{L1} \quad (81)$$

$$I_{D2} = I_{L2} = (1-D) \times I_{L1}$$

$$(1-D) \times I_{L1} = \frac{Vo}{R(1-D)^2} \quad (82)$$

$$I_{L1} = \frac{Vo}{R(1-D)^3} \quad (83)$$

Now, rewriting the above equation in terms of input voltage by replacing the Vo from equation (71) and combining equation (74) and equation (83) we get:

$$(I_{L1})_{Min} = \frac{Vin}{R(1-D)^6} - \frac{VinDT}{2L_1} \quad (84)$$

For continuous mode conduction, the minimum inductor current should be greater than zero:

$$\frac{Vin}{R(1-D)^6} - \frac{VinDT}{2L_1} \geq 0$$

$$\frac{Vin}{R(1-D)^6} \geq \frac{VinDT}{2L_1}$$

$$L_1 \geq \frac{R(1-D)^6 D}{2f_s} \quad (85)$$

The voltage across the inductor L_2 is equal to the capacitor voltage V_{C1}:

$$L_2 \frac{dI_{L2}}{dt} = V_{C1}$$

$$\frac{dI_{L2}}{dt} = \frac{V_{C1}}{L_2}$$

$$\frac{\Delta I_{L2}}{DT} = \frac{V_{C1}}{L_2} \quad (86)$$

$$\Delta I_{L2} = \frac{V_{C1}DT}{L_2} \quad (87)$$

$$(I_{L2})_{Min} = I_{L2} - \frac{\Delta I_{L2}}{2} \quad (88)$$

Now putting the value of I_{L2} from equation (80) into equation (88):

$$(I_{L2})_{Min} = \frac{Vo}{R(1-D)^2} - \frac{\Delta I_{L2}}{2} \quad (89)$$

Now replacing Vo from equation (71) and ΔI_{L2} from equation (87):

$$(I_{L2})_{Min} = \frac{Vin}{R(1-D)^5} - \frac{V_{C1}DT}{2L_2} \quad (90)$$

Now replacing V_{C1} from equation (67):

$$(I_{L2})_{Min} = \frac{Vin}{R(1-D)^5} - \frac{VinDT}{2L_2(1-D)} \quad (91)$$

For continuous mode conduction, the minimum inductor current should be greater than zero:

$$\frac{Vin}{R(1-D)^5} - \frac{VinDT}{2L_2(1-D)} \geq 0 \quad (92)$$

$$\frac{Vin}{R(1-D)^5} \geq \frac{VinDT}{2L_2(1-D)}$$

$$L_2 \geq \frac{R(1-D)^4 D}{2f_s} \quad (93)$$

The voltage across the inductor L_3 is equal to the capacitor voltage V_{C2}:

$$L_3 \frac{dI_{L3}}{dt} = V_{C2}$$

$$\frac{dI_{L3}}{dt} = \frac{V_{C2}}{L_3}$$

$$\frac{\Delta I_{L3}}{DT} = \frac{V_{C2}}{L_3} \quad (94)$$

$$\Delta I_{L3} = \frac{V_{C2}DT}{L_3} \quad (95)$$

$$(I_{L3})_{Min} = I_{L3} - \frac{\Delta I_{L3}}{2} \quad (96)$$

Now putting the value of I_{L3} from equation (76) into equation (96) we get:

$$(I_{L3})_{Min} = \frac{Vo}{R(1-D)} - \frac{\Delta I_{L3}}{2} \quad (97)$$

Now replacing Vo from equation (71) and ΔI_{L3} from equation (95):

$$(I_{L3})_{Min} = \frac{Vin}{R(1-D)^4} - \frac{V_{C2}DT}{2L_3} \quad (98)$$

Now replacing V_{C2} from equation (68):

$$(I_{L3})_{Min} = \frac{Vin}{R(1-D)^4} - \frac{VinDT}{2L_3(1-D)^2} \quad (99)$$

For continuous mode conduction, the minimum inductor current should be greater than zero:

$$\frac{Vin}{R(1-D)^4} - \frac{VinDT}{2L_3(1-D)^2} \geq 0 \quad (100)$$

$$\frac{Vin}{R(1-D)^4} \geq \frac{VinDT}{2L_3(1-D)^2}$$

$$L_3 \geq \frac{R(1-D)^2 D}{2f_s} \tag{101}$$

As with the quadratic boost converter, the value of the inductor depends on the duty ratio, load resistance, and the switching frequency.

D. DESIGN OF CAPACITORS

When the switch is ON:

$$I_{C1} = I_{L2} = \frac{Vo}{R(1-D)^2} \tag{102}$$

Substituting the value of I_{C1} and V_{C1} in equation (25):

$$\frac{VoDT}{R(1-D)^2} = C_1 \Delta V_{C1} \tag{103}$$

$$C_1 \Delta V_{C1} = \frac{VoDT}{R(1-D)^2} \tag{104}$$

Now putting the value of *Vo* in terms of input voltage:

$$C_1 = \frac{VinD}{R(1-D)^5 \Delta V_{C1} f_s} \tag{105}$$

Similarly,

$$I_{C2} = I_0 = \frac{Vo}{R(1-D)} \tag{106}$$

Substituting the value of I_{C2} and V_{C2} in equation (25):

$$I_{C2} = I_0 = \frac{Vo}{R(1-D)} \tag{107}$$

$$C_2 \Delta V_{C2} = \frac{VoDT}{R(1-D)} \tag{108}$$

Now replacing the value of *Vo* in terms of input voltage:

$$C_2 = \frac{VinD}{R(1-D)^4 \Delta V_{C2} f_s} \tag{109}$$

Similarly:

$$I_{C3} = I_0 = \frac{Vo}{R} \tag{110}$$

Substituting the value of I_{C3} and V_O in equation (47):

$$C_3 \Delta V_{C3} = \frac{VoDT}{R} \tag{111}$$

Replacing the value of *Vo* in terms of input voltage:

$$C_3 = \frac{VinD}{R(1-D)^3 \Delta V_{C3} f_s} \tag{112}$$

E. POWER LOSSES IN THE CIRCUIT.

The power loss calculation is performed as explained in section D of the quadratic boost converters. The expressions for various losses in the case of cubic boost converter are as follows:

Power loss in the inductors:

$$P_{L_1} = \frac{Vo^2 r_{L1}}{R^2(1-D)^6} \tag{113}$$

$$P_{L_2} = \frac{Vo^2 r_{L2}}{R^2(1-D)^4} \tag{114}$$

$$P_{L_3} = \frac{Vo^2 r_{L3}}{R^2(1-D)^2} \tag{115}$$

$$P_{L_{total}} = \frac{Vo^2 r_{L1}}{R^2(1-D)^6} + \frac{Vo^2 r_{L2}}{R^2(1-D)^4}$$
$$+ \frac{Vo^2 r_{L3}}{R^2(1-D)^2} \tag{116}$$

Power loss in the capacitors:

$$P_{C_1} = \frac{Vo^2 r_{C1}(D+D^3-D^2)}{R^2(1-D)^6} \tag{117}$$

$$\frac{Vo^2 D r_{C2}}{R^2(1-D)^3} \tag{118}$$

$$P_{C_3} = \frac{Vo^2 D r_{C3}}{R^2(1-D)} \tag{119}$$

$$P_{C_{total}} = \frac{Vo^2 r_{C1}(D+D^3-D^2)}{R^2(1-D)^6} + \frac{Vo^2 D r_{C2}}{R^2(1-D)^3}$$
$$+ \frac{Vo^2 D r_{C3}}{R^2(1-D)} \tag{120}$$

Power loss in the diodes:

$$P_{d_1} = \frac{V_d VoD}{R(1-D)^3} + \frac{Vo^2 D r_d}{R^2(1-D)^6} \tag{121}$$

$$P_{d_1} = \frac{V_d Vo}{R(1-D)^2} \times D + \frac{Vo^2 D r_d}{R^2(1-D)^4} \tag{122}$$

$$P_{d_2} = \frac{V_d Vo}{R(1-D)^2} + \frac{Vo^2 r_d}{R^2(1-D)^3} \tag{123}$$

$$P_{d_3} = \frac{V_d VoD}{R(1-D)^2} + \frac{Vo^2 D r_d}{R^2(1-D)^4} \tag{124}$$

$$P_{d_4} = \frac{V_d Vo}{R(1-D)} + \frac{Vo^2 r_d}{R^2(1-D)^3} \tag{125}$$

$$P_{d_5} = \frac{V_d Vo}{R} + \frac{Vo^2 r_d}{R^2(1-D)} \tag{126}$$

$$P_{d_{total}} = \frac{V_d VoD}{R(1-D)^3} + \frac{V_d Vo}{R(1-D)^2}$$
$$+ \frac{V_d VoD}{R(1-D)^2} + \frac{V_d Vo}{R(1-D)} + \frac{V_d Vo}{R}$$
$$+ \frac{Vo^2 D r_d}{R^2(1-D)^6} + \frac{Vo^2 r_d}{R^2(1-D)^3} + \frac{Vo^2 D r_d}{R^2(1-D)^4}$$
$$+ \frac{Vo^2 r_d}{R^2(1-D)^3} + \frac{Vo^2 r_d}{R^2(1-D)} \tag{127}$$

Power loss in the switch:

$$P_{sw} = P_{sw_{Cond}} + P_{sw_{ON}} + P_{sw_{OFF}} \tag{128}$$

$$P_{sw_{Cond}} = \frac{Vo^2(3-3D+D^2)^2 D}{R^2(1-D)^6} r_{swcON} \tag{129}$$

$$P_{sw_{ON}} = \frac{0.5 Vo^2(3-3D+D^2)}{R(1-D)^3} \times \frac{t_{ri}+t_{fv}}{2} \times f_s \tag{130}$$

$$P_{sw_{OFF}} = \frac{0.5 Vo^2(3-3D+D^2)(t_{fi}+t_{rv})}{2R(1-D)^3} \times f_s \tag{131}$$

TABLE 1. Hardware in loop validation- parameters.

Parameters	Value
Inductors	$L_1 = 2 \times 10^{-4}\ H$
	$L_2 = 5 \times 10^{-4}\ H$
	$L_3 = 9 \times 10^{-4}\ H$
Capacitors	$C_1 = 9000 \times 10^{-6}\ F$
	$C_2 = 2000 \times 10^{-6}\ F$
	$C_3 = 1000 \times 10^{-6}\ F$

F. NON-IDEAL VOLTAGE CALCULATION

The actual value of the output voltage could be calculated as follows:

$$Input\ Power = I_{L1} Vin \tag{132}$$

$$Input\ Power = \frac{VoVin}{R(1-D)^3} \tag{133}$$

$$Output\ Power = \frac{Vo^2}{R} \tag{134}$$

After combining all the losses and putting it in equation (52) we get the actual voltage as presented in equation (135), as shown at the bottom of the next page. As the duty ratio increases the losses in the circuit increase but the cubic boost converter is capable of providing high gain at lower duty ratio which means that, for the same output voltage with a similar load, the cubic boost converter will provide better efficiency as compared to quadratic boost.

G. HARDWARE-IN-LOOP VALIDATION

The hardware-in-loop validation results for the proposed cubic boost converter are provided in figure 6.

Figure 6(a) shows the waveforms for current across the inductors. The current across inductor 1, 2 and 3 is 11, 4.4 and 2.2 amperes respectively. Figure 6(b) shows the waveforms for the voltage across the capacitors C_1 and C_2 and the switch. The voltage values are 28 and 70 volts respectively across capacitors C_1 and C_2.

Figure 6(c) shows the waveforms for the input and output voltage and the voltage across the switch while in conduction. The input and output voltages were found to be 12 volts and 170 volts respectively. Hence, for an input voltage of 12 volts, the output is 170 volts at a duty ratio of 0.6. Hence, the gain is approximately 14 times of the input value.

Table 2 shows the summary of output gains of both the converters. It is clearly seen from the comparison that the proposed converter has a much higher value of gain at the same duty ratio.

H. VOLTAGE STRESS CALCULATION

Table 3 gives the voltage stress across the switch and diodes used in conventional boost, quadratic boost and cubic boost converters.

TABLE 2. Summary of output gains.

Converter	Input Voltage (volts)	Output Voltage (volts)	Gain Factor
Cubic	12	170	14
Quadratic	12	70	6

TABLE 3. Voltage stress across The switch and diodes.

Conventional Boost Voltage Stress	Quadratic Boost Voltage Stress	Cubic Boost Voltage Stress
$V_{sw} = Vo$	$V_{sw} = Vo$	$V_{sw} = Vo$
$V_{D1} = Vo$	$V_{D3} = Vo$	$V_{D5} = Vo$
	$V_{D2} = Vo(1-D)$	$V_{D4} = Vo(1-D)$

If the output voltage for all three converters is the same, then the maximum voltage stress across the switch and the diode is the same in all three converters (conventional, quadratic, and cubic). The voltage stress across each diode and the switch is presented in table 4 for an output voltage of 48V and with an input voltage of 12V. The voltage stress across the diode and switch per unit output voltage is shown in figure 7.

TABLE 4. Voltage stress across the switch and diodes at a constant output voltage.

Conventional Boost Voltage Stress	Quadratic Boost Voltage Stress	Cubic Boost Voltage Stress
$V_{sw} = 48V$	$V_{sw} = 48V$	$V_{sw} = 48V$
$V_{D1} = 48$	$V_{D3} = 48V$	$V_{D5} = 48V$
	$V_{D2} = 24V$	$V_{D4} = 30.24V$
	$V_{D1} = 24V$	$V_{D3} = 17.76V$
		$V_{D2} = 19.05V$
		$V_{D1} = 29V$

I. DISCONTINUOUS CONDUCTION MODE ANALYSIS

The proposed converter has three inductors; if the current of any inductor becomes zero, the output voltage of the converter changes with the following behaviour:
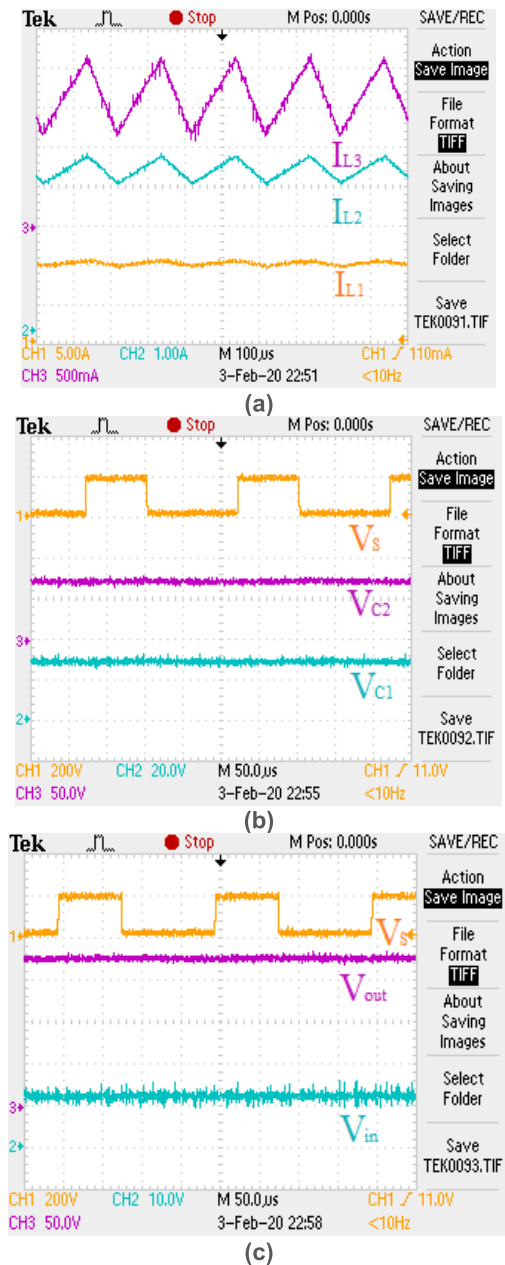
i. When L_1 or L_3 has a lower value of inductance that is:

$$L_1 < \frac{R(1-D)^6 D}{2f_s} orL_3 < \frac{R(1-D)^2 D}{2f_s} \tag{136}$$

The converter fails to operate, and the output voltage becomes unstable.

ii. When only L_2 has a lower value of inductance that is:

$$L_2 < \frac{R(1-D)^4 D}{2f_s} \tag{137}$$

FIGURE 6. Hardware in loop validation results for the cubic boost converter for duty ratio=0. 6. (a) current across the inductor L_1 and L_2 (b) the voltage across capacitors C_1 and C_2. (c) the input and output voltage.

The proposed converter operates in DCM and the output voltage can be calculated as follows

$$Vo = \frac{Vin(D_1+D_2)}{(1-D_1)^2 D_2} \quad (138)$$

where

D_1 is the rise time duty ratio of I_L
D_2 is the fall time duty ratio of I_L

The simulation results shown in figure 8, D2 is found to be 0.42 whereas D_1 is set at 0.4. Using these values, the output voltage is calculated and was found to be 65 volts, which is slightly greater than the value presented in the graph. This is because of the internal losses of the circuit.

J. EFFICIENCY CALCULATION

Thermal losses and the resultant heat generation is an important loss criterion in the design of power electronic converters. Switching losses and conduction losses are the two components that eventually result in degradation of the performance of the converter. Conduction loss is caused by the non-ideal behavior switch as a result of a voltage drop across the switch and the equivalent resistance in ON state. The losses in an IGBT and diode respectively are described by (139) and (140) respectively. The total is averaged over the fundamental period of 2π in (141).

$$P_{c_{sw}} = V_{sw}i(t) + R_s i^\beta(t) \quad (139)$$

$$P_{c_D} = V_D i(t) + R_D i^2(t) \quad (140)$$

$$P_c = \sum_{k=1}^{N_{sw}} \frac{1}{2\pi} \int_0^{2\pi} \left(V_{sw}i(t) + R_s i^\beta(t) \right) dt$$

$$+ \sum_{k=1}^{N_D} \frac{1}{2\pi} \int_0^{2\pi} \left(V_D i(t) + R_D i^2(t) \right) dt \quad (141)$$

where V_{sw} stands for the voltage drop of the power electronic switch during ON state and V_D stands for the corresponding voltage drop across the antiparallel diode.

Switching loss is due to non-ideal transitions through the ON and OFF states across a switch. Linear variation of current and voltage is an underlying assumption while calculating switching losses. Switching losses are described using (142).

$$P_s = \left[\sum_{k=1}^{Ns} \left(N_{ON_k} E_{ON_k} + N_{OFF_k} E_{OFF_k} \right) \right] \times f \quad (142)$$

N_{ON_k} and N_{OFF_k} respectively enumerate the transitions between ON and OFF states within one complete fundamental period and E_{ON_k} and E_{OFF_k} represent the energy losses in joules with f denoting the modulation frequency.

Total loss

$$P_{\text{loss}} = P_c + P_s \quad (143)$$

$$Vo = \frac{VinR(1-D)^3 - RVd(1-D)^3 \left\{ D + (1-D) + D(1-D) + (1-D)^2 + (1-D)^3 \right\}}{R(1-D)^6 + r_d \left\{ D + 2(1-D)^3 + D(1-D)^2 + D(1-D)^5 \right\} + r_{L1} + r_{L2}(1-D)^2 + r_{L3}(1-D)^4 + r_{C1}\left(D + D^3 - D^2\right) + r_{C2}D(1-D)^3 + r_{C3}D(1-D)^5 + r_{swoN}\,D\left(3 - 3D + D^2\right)^2 + 0.5(1-D)^3\left(3 - 3D + D^2\right)\left(\frac{t_{fi}+t_{rv}}{2} + \frac{t_{ri}+t_{fv}}{2}\right)f_s R}$$
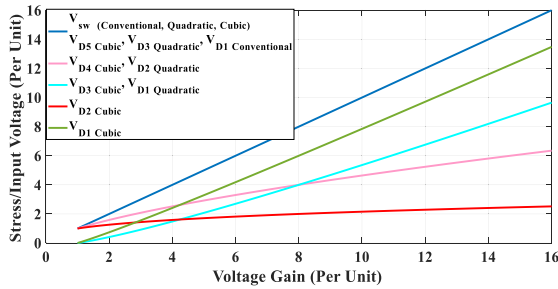
$$(135)$$

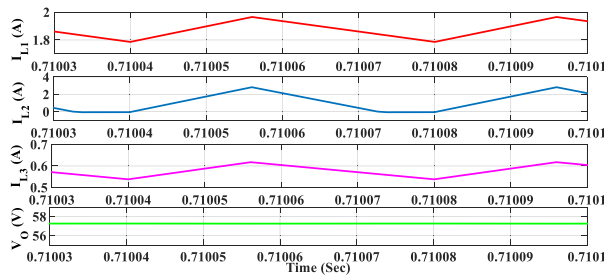**FIGURE 7.** Voltage stress for different devices.

FIGURE 8. Discontinuous Mode Analysis.

Efficiency is calculated as given in (144)

$$\eta = \frac{P_0}{P_0 + P_{loss}} \times 100\% \tag{144}$$

The proposed converter was analyzed for thermal modelling on PLECS software. C6D06065A Schottky Diode and IKW40N65ES5 IGBT were taken for thermal modelling of the topology.

Figure 9 and figure 10 represent the conduction loss characteristics for Diode and IGBT respectively while figure 11 shows the switching loss characteristics for the IGBT.

Figure 12 shows the efficiency curve as a function of output power. Peak efficiency was achieved at a value of 96.5% at the output power of 100W. Although efficiency decreases with increasing load, the decrease is not substantial and the lowest value 93% is observed at 2kW.

K. BOOST CONVERTER OF $\frac{1}{(1-D)^n}$ GAIN
The same approach as in the case of the quadratic boost and cubic boost converter can be used to develop a converter with a voltage gain of $1/(1-D)^n$, where n is the number of inductors or capacitors used.

The generalized equation for nth-order boost converter shown in figure 13 is as follows:

$$(Vo)_{Ideal} = \frac{Vin}{(1-D)^n} \tag{145}$$

IV. COMPARATIVE ANALYSIS
This section presents a comparison of the voltage gain and voltage stress across the switch of the various boost converters discussed in the literature, the QBC, and the

proposed CBC. The voltage drop across the inductor is also presented in this section.

A. COMPARISION WITH OTHER TOPOLOGIES
The comparison of the CBC with other high gain converters like QBC and other converters given in literature [11], [12], [36]–[42] is shown in figure 14 in terms of voltage gain and duty ratio and in terms of the number of different components required in table 5. The gain in the case of cubic boost is higher than other topologies as illustrated in figure 14.

TABLE 5. Comparison of various high gain converters.

Topology	Number of components				Gain	Voltage across switch
	L	C	D	S		
[11]	3	3	3	1	$\dfrac{D}{(1-D)^2}$	Vo
[12]	2	3	3	2	$\dfrac{2+D}{1-D}$	$\dfrac{Vo}{2+D}$
[36]	2	3	2	1	$\dfrac{1+D}{1-D}$	$\dfrac{Vo}{1+D}$
[37]	4	6	3	1	$\dfrac{3D}{1-D}$	$\dfrac{Vo}{2}$
[38]	1	3	3	1	$\dfrac{2}{1-D}$	$\dfrac{Vo}{2}$
[39]	1	4	4	1	$\dfrac{3-D}{1-D}$	$\dfrac{Vo}{3-D}$
[40]	2	3	3	2	$\dfrac{1}{D(1-D)}$	$Vo(1-D),$ VoD
[41]	2	3	2	1	$\dfrac{2D}{1-D}$	$\dfrac{Vo}{2D}$
[42]	3	3	5	1	$\dfrac{D^2}{(1-D)^2}$	$\dfrac{Vo}{D^2}$
QBC	2	2	3	1	$\dfrac{1}{(1-D)^2}$	Vo
CBC	3	3	5	1	$\dfrac{1}{(1-D)^3}$	Vo

S: Switch, D: Diode, L: Inductor, C: Capacitor, Voltage Gain= Vo/Vin

B. VOLTAGE DROP ACROSS INDUCTOR
There is a net voltage drop across each inductor which is due to the presence of internal resistance of the inductor. The average voltage drop across each inductor can be calculated as follows:

$$\Delta V_{L1} = \frac{I_{L1} \times r_{L1}}{Vo} \times 100\% \tag{146}$$

$$\Delta V_{L1} = \frac{\frac{Vo}{R(1-D)^3} \times r_{L1}}{Vo} \times 100\% \tag{147}$$
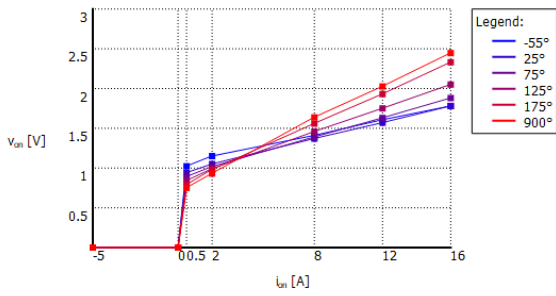
FIGURE 9. Diode Conduction loss model C6D06065A.
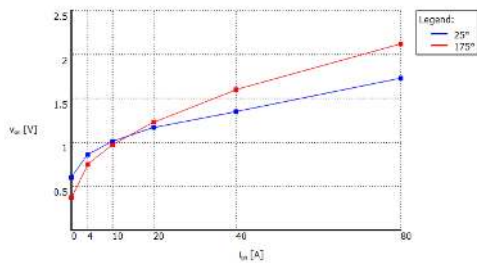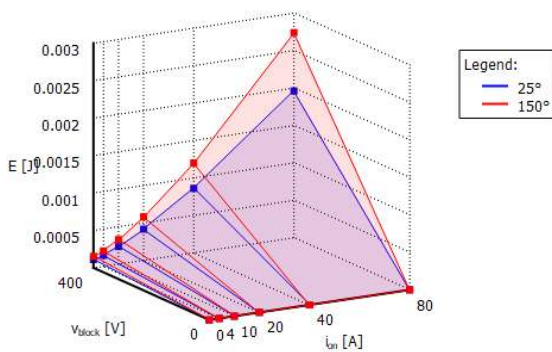

FIGURE 10. IGBT Switch conduction loss IKW40N65ES5.

FIGURE 11. IGBT Switch switching loss IKW40N65ES5.

$$\Delta V_{L1} = \frac{r_{L1}}{R(1-D)^3} \times 100\% \qquad (148)$$

Similarly : $\qquad\qquad\qquad\qquad\qquad (149)$

$$\Delta V_{L2} = \frac{r_{L2}}{R(1-D)^2} \times 100\% $$

$$\Delta V_{L3} = \frac{r_{L3}}{R(1-D)} \times 100\% \qquad (150)$$

The voltage drop across each inductor as a percentage of output voltage depends on the load resistance, internal resistance as well as on the duty ratio. The pie chart for the voltage drop across each inductor as a percentage of the output voltage is shown in figure 15 for different duty ratios.

The voltage drop across each inductor is similar at lower duty ratios but at higher values of duty ratio, the voltage drop across the inductor increases as we move towards the source. This happens because at a high value of duty ratio the input current becomes very high.
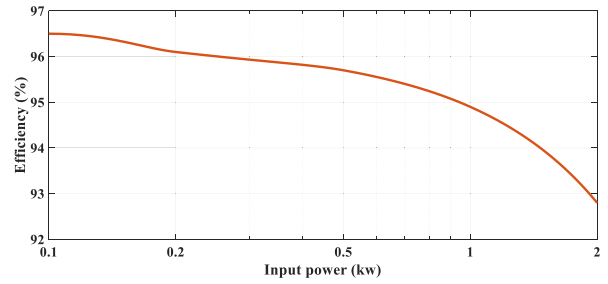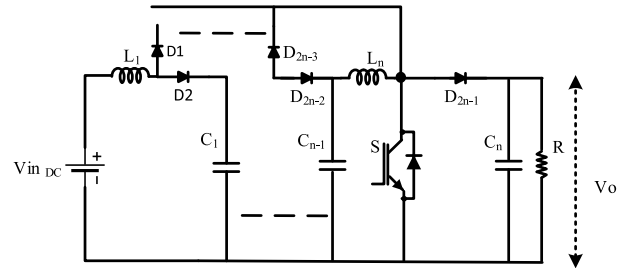

FIGURE 12. Efficiency curve.

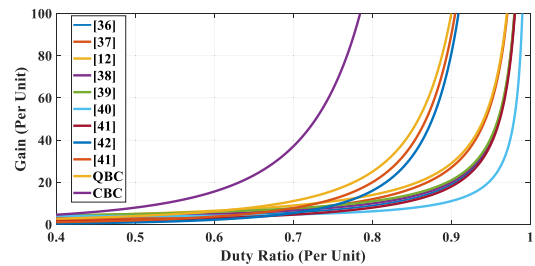**FIGURE 13.** Circuit diagram of nth boost.

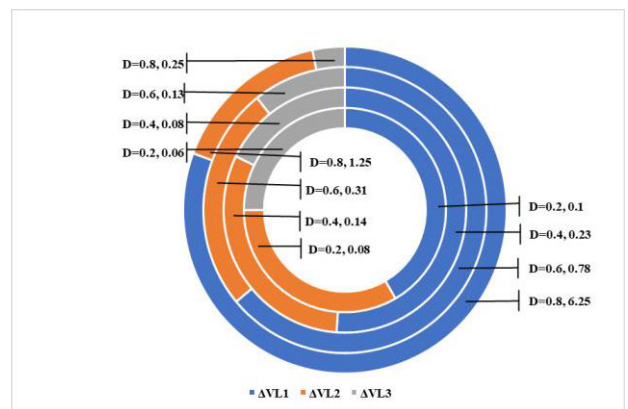**FIGURE 14.** Comparison of the various high gain converter.

FIGURE 15. Voltage drop across each inductor as a percentage of the output voltage at D=0.2, 0.4, 0.6 and 0.8.

V. SOLAR MPPT USING THE PROPOSED CUBIC CONVERTER

For further verification, the proposed converter's performance was tested on a real-world application. The voltage output of a solar PV array is generally very low and cannot

be used for high voltage applications. Moreover, connecting a conventional boost converter as an interface between a solar PV and the output load produces high voltages but at the cost of higher conduction losses due to higher duty ratio values. The quadratic boost converter was employed to mitigate higher losses by generating higher voltages at lower duty ratios. Even though the converter was successful, the smaller the duty ratio the more efficient the system will become. Hence, owing to its ability to produce higher gains at lower duty ratios, in this article the proposed cubic converter is employed for solar PV applications. A PV module of standard rating having an MPP of 21.8 watts was chosen. A total of four modules were connected in series thereby making an array of MPP of 87 watts. In order to show the effectiveness of the proposed converter, it was tested for different insolation conditions on the PV array. The comparison was done between the proposed converter and the quadratic and conventional boost converters. The results clearly show that the proposed algorithm successfully tracked the MPP at lower duty ratio values thereby reducing conduction losses and increasing the overall efficiency. The Jaya algorithm proposed for MPPT in [43] was chosen to track the MPP of the PV array under different insolation conditions.

A. THE JAYA ALGORITHM

The jaya algorithm is a nature-inspired algorithm. It is an efficient algorithm for solving optimization problems owing to its simplicity and causing less burden on processors. Moreover, unlike other metaheuristic algorithms, it does not have any algorithm specified parameters defined by the authors like inertial weight and acceleration in particle swarm optimization (PSO), scout bees in an artificial bee colony (ABC), etc., hence it is independent and does not require specific tuning for different optimization problems [43]. The term jaya means victory—the algorithm works by eliminating bad solutions thereby moving towards victory. The following equations are involved in the implementation of the jaya algorithm:

$$X_v^{iC1} = X_v^i + c_1^i * rand_1^i \left(X_{best}^i - \left| X_v^i \right| \right)$$
$$- c_2^i * rand_2^i \left(X_{worst}^i - \left| X_v^i \right| \right) \quad (151)$$

In this article time-varying coefficients are also incorporated in order to further improvise the performance of the jaya algorithm based on the study in [44]. The coefficients are defined as follows:

$$c_{1i} = c_{2i} = 1, c_{1f} = 0.5 \, and \, c_{2f} = 0 \quad (152)$$

$$c_1^i = c_{1i} - (c_{1i} - c_{1f}) \frac{i}{i_{max}} \quad (153)$$

$$c_2^i = c_{2f} - (c_{2f} - c_{2i}) \frac{i_{max} - i}{i_{max}} \quad (154)$$

where, X_v^i denotes the *vth* solution of a function at the *ith* iteration, c_1^i and c_2^i are acceleration coefficients at the

ith iteration respectively, and *rand* is a random number between zero and one.

B. MPPT USING THE JAYA ALGORITHM

In MPP tracking the duty ratio value of a boost converter is the most significant parameter. The duty ratio is considered analogous to the *vth* solution of a function at the *ith* iteration. In each iteration the duty ratio was updated using the updating equations of the jaya algorithm as given in figure 16. After every iteration the power corresponding to the new duty ratio was compared with the previous power value. The new power with its corresponding duty ratio was saved if it was higher than the previous value. After a few iterations, when the difference between the best and the worst values becomes insignificant, all the particles become approximately equal
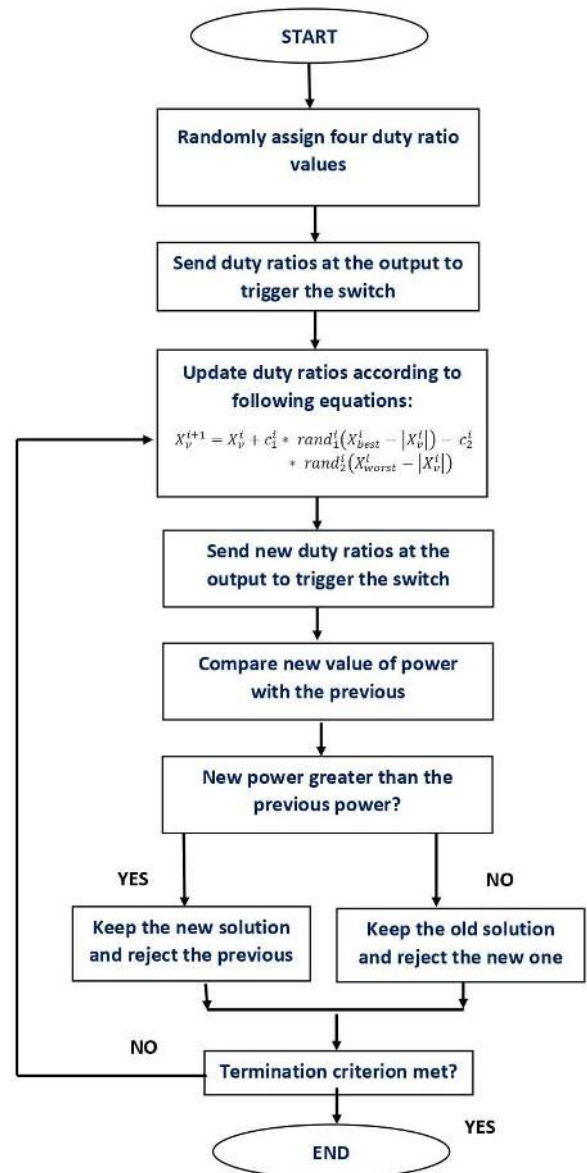

FIGURE 16. Flowchart for MPPT using Jaya algorithm.

to the global optima. Therefore, the difference between the present, best and the worst solutions becomes negligible and the best and worst values now have no effect on the present solution which is thereby constant in each iteration. Consequently, a constant duty ratio is sent at the output in each iteration and the algorithm converges to the optimal power. Moreover, in this study the algorithm was designed such that, as soon as the difference between powers corresponding to all the duty ratio values becomes less than 5%, the algorithm only sends the global best duty ratio at the output thereby ensuring guaranteed convergence as done in [45]. The iteration continues until the difference between all the power values is more than 5%.

C. HARDWARE-IN-THE-LOOP VALIDATION OF THE PROPOSED TOPOLOGY FOR MPPT USING TYPHON HIL 402

The results are divided into two sections. In the first section the results were taken for the static insolation conditions After that the real time dynamic insolation conditions were defined in order to further verify the performance of the proposed topology. The curves blue and red in colour corresponds to power and duty ratio respectively.

#### 1) STATIC INSOLATION CONDITIONS

The results were taken for two different partially shaded conditions in order to show the performance of the proposed converter for different cases of partial shading.

a: SHADING CASE A

The insolation values on all the four modules were kept at 1000, 900, 800 and 850 W/m^2 respectively. The maximum power peak in this case was at the right most position. Figure 17 (a) shows the performance of the conventional boost converter. MPP was successfully tracked using this topology with the maximum power of 74.4 watts. The duty ratio value was found to be 0.57. The time taken for convergence to the maxima was 1.95 seconds. Figure 17 (b) shows the performance of the quadratic boost converter. The MPP was successfully tracked and the power at the output was found to be 74.5 watts. The duty ratio value was found to be 0.37. The time taken for convergence was 1.95 seconds. Figure 17 (c) shows the performance of the proposed cubic boost converter. The MPP was successfully tracked with the maximum power at the output to be 74.35 watts. The duty ratio was found to be 0.28. The time taken for convergence to the maximum was 2.2 seconds.
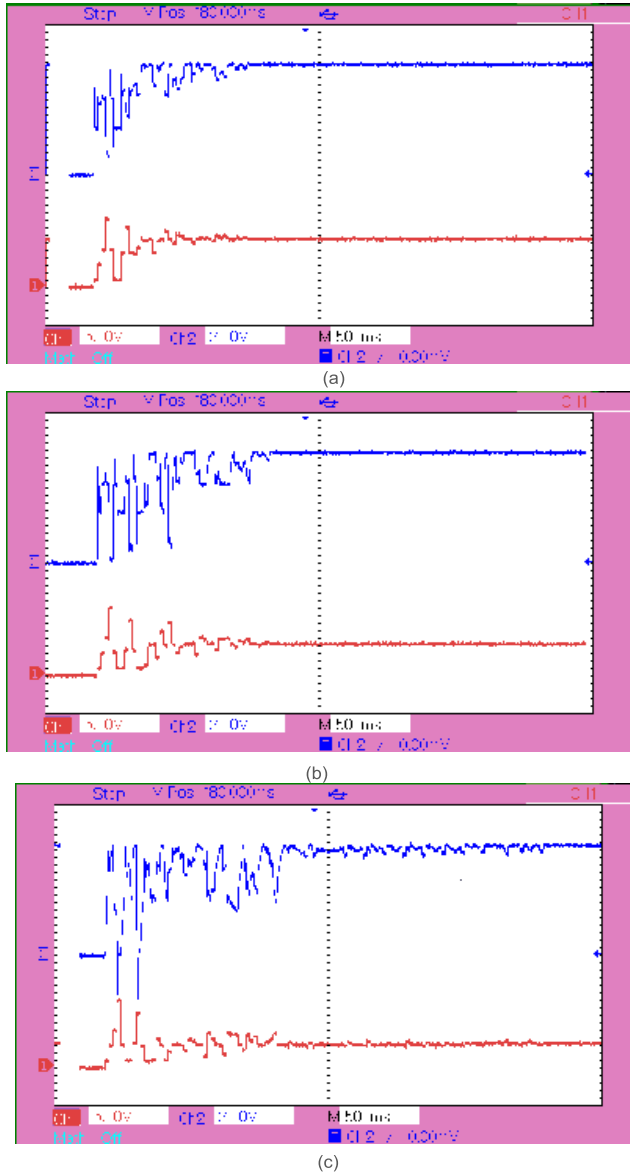
b: SHADING CASE B

The insolation values in this case were kept at 1000, 950, 850 and 500 W/m^2 on four modules respectively. The optimal peak was formed at the middle position. Figure 18 (a) shows the performance of the conventional boost converter. The MPP value was found to be 59 watts with a duty ratio of 0.64. The time taken for convergence was 1.95 seconds. Figure 18 (b) shows the performance of the quadratic boost
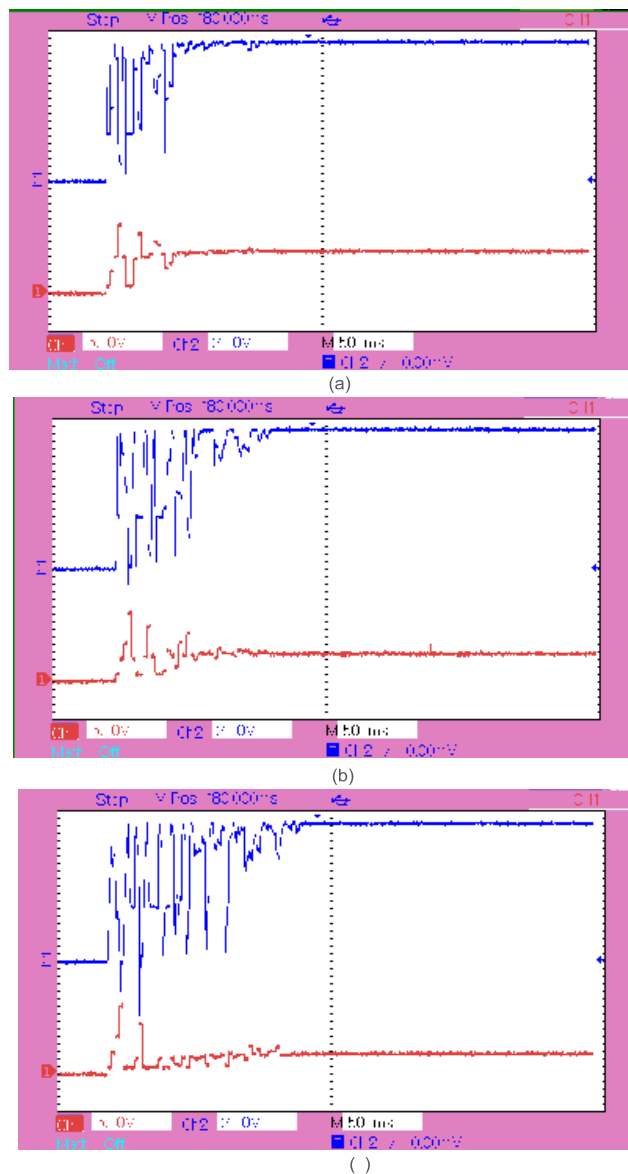
FIGURE 17. Power output and duty ratio for MPPT for partial shading case A of (a) Conventional converter (b) Quadratic converter (c) Cubic converter.

converter. The MPP value was found to be 58.41 watts at a duty ratio of 0.42. The time taken for convergence was 2.2 seconds. Figure 18 (c) shows the performance of the proposed cubic boost converter. The MPP value was found to be 58.96 watts at a duty ratio of 0.33. The time taken for convergence was 5.7 seconds. It is observed from the results that the duty ratio of the proposed converter is smaller than other two converters. Therefore, the conduction losses will be reduced. Although for this case the settling time was more, the fluctuations were very small and may not contribute to high power losses. Table 6 illustrates the summary of duty ratio, maximum power and convergence time for all the three converters for both partial shading cases.

FIGURE 18. Power output and duty ratio for MPPT for partial shading case B of (a) Conventional converter (b) Quadratic converter and (c) Cubic converter.

2) DYNAMIC INSOLATION CONDITIONS

In order to further prove the performance of the proposed converter the results are shown for a real-time scenario. In actual world scenario the insolation values keep changing with time, hence, in this case the insolation is changed after every 3 seconds on the PV array. Initially, three modules were partially shaded and the number of peaks formed were four. After 3 seconds only two modules were shaded and the number of peaks were three. Finally, after 6 seconds only one module was shaded and the number of peaks formed were two. The simulation was terminated after 9 seconds. The variation of insolation values is summarized in Table 7.

Figure 19 (a) shows the performance of conventional converter under dynamic insolation conditions. The duty ratios

TABLE 6. Performance summary of the three converters for both cases of partial shading.

| Shading Case A			
Converter	**Duty Ratio**	**Power (watts)**	**Convergence Time (seconds)**
Conventional	0.57	74.4	1.95
Quadratic	0.37	74.5	1.95
Cubic	0.28	74.35	2.2
Shading Case B			
Converter	**Duty Ratio**	**Power (watts)**	**Convergence Time (seconds)**
Conventional	0.64	59	1.95
Quadratic	0.42	58.41	2.2
Cubic	0.33	58.96	5.7

TABLE 7. Summary for shading patterns under dynamic insolation conditions.

| Instant	Insolation Pattern (W/m^2)
Initially	1000, 850, 800 and 700
After 3 seconds	1000, 1000, 900 and 750
After 6 seconds	1000, 1000, 1000 and 800

were changed for every insolation. The power for the three insolation conditions was found to be 66.68, 71.99 and 76.4 watts respectively. The time taken to converge was 1.35, 1.35 and 1.8 seconds respectively. The duty ratio corresponding to each insolation was found to be 0.5364, 0.545 and 0.566, respectively. Figure 19 (b) shows the performance of the quadratic boost converter. The power for the three insolation conditions were found to be 66.6, 71.72 and 75.35 watts respectively. The time taken to converge was 1.8, 2.5 and 1.95 seconds respectively. The duty ratio corresponding to each insolation was found to be: 0.338, 0.3468 and 0.35 respectively. Figure 19 (c) shows the performance of cubic boost converter. The power for the three insolation conditions were found to be 66.4, 71.86 and 76.33 watts. The time taken to converge was 2.45, 2.6 and 2.95 seconds respectively. The duty ratio corresponding to each insolation was found to be 0.26, 0.2707 and 0.281 respectively.

Hence, after comparing the proposed converter with other converters under different partially shaded conditions it was found that the proposed converter tracked the maximum power with the lowest duty ratio thereby reducing the conduction losses. The minimum duty ratio limit in this study was kept at 0.1. However, the author would suggest to keep it even smaller along with maintaining the safety. The performance summary of all the three converters is given in Table 8.
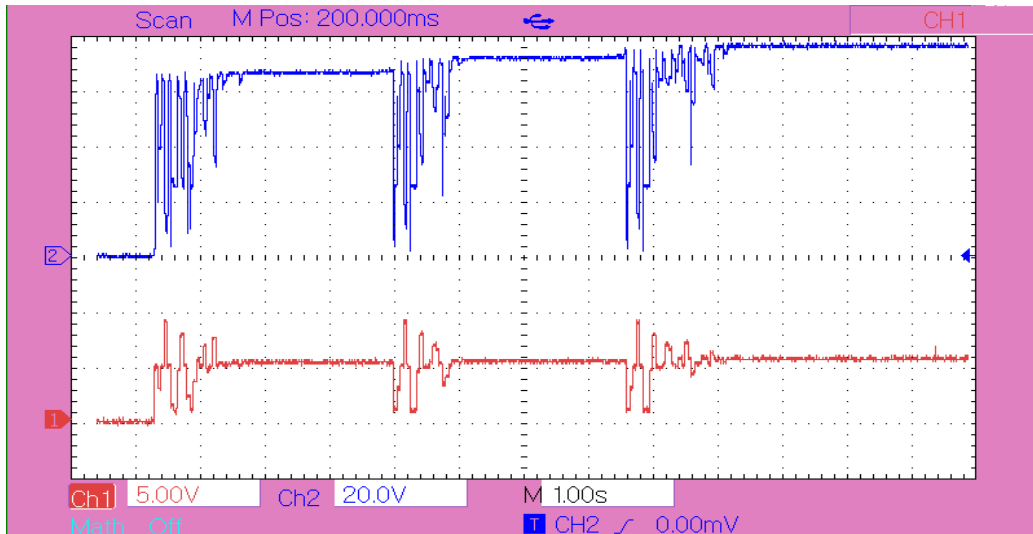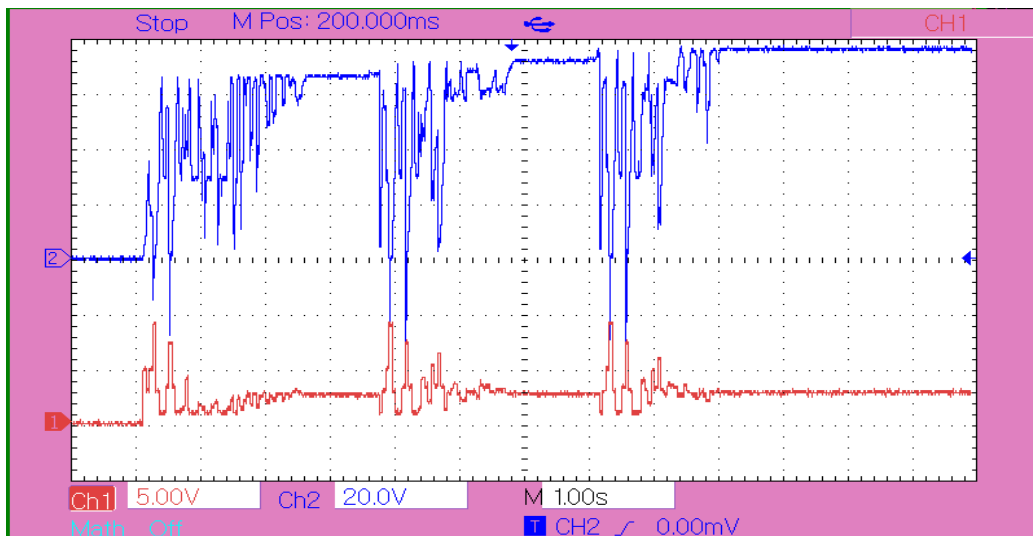
(a)
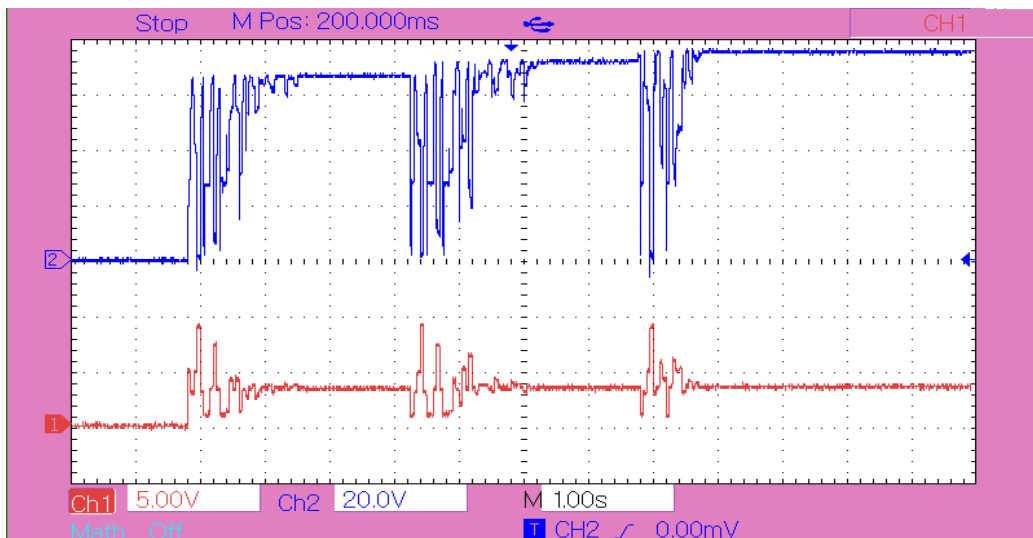
(b)

(c)

FIGURE 19. Power output and duty ratio for MPPT under dynamic insolation condition of (a) Conventional converter (b) Quadratic converter (c) Cubic converter.

TABLE 8. Performance summary of the three converters for dynamic partial shading conditions.

Dynamic Insolation Conditions				
Initially	Converter	Power (watt)	Duty Ratio	Convergence Time (sec.)
	Conventional	66.68	0.5364	1.35
	Quadratic	66.6	0.338	1.8
	Cubic	66.4	0.26	2.45
After 3 seconds	Conventional	71.99	0.545	1.35
	Quadratic	71.72	0.3468	2.5
	Cubic	71.86	0.2707	2.6
After 6 Seconds	Conventional	76.4	0.566	1.8
	Quadratic	75.35	0.35	1.95
	Cubic	76.33	0.281	2.95

VI. MANAGERIAL IMPLICATIONS

One of the most important factors in electricity generation devices is the efficiency that they provide. Higher efficiency implies lower losses thereby leading to reduced cost of the overall system. Moreover, it also provides long term benefits by reducing peak demands thereby eliminating the need for extra generation and transmission of energy which is a more expensive task. The proposed converter in this article provides the desirable benefits by significantly improving the voltage gain at smaller duty ratios thereby reducing conduction losses and increasing efficiency. Also, at higher output loads (high demands) the efficiency of the proposed topology was improved. The proposed topology was also employed for controlling power output of a solar PV array in order to show its effectiveness for industrial use. It was clear from the results that the proposed converter provides the same maximum power output but at a reduced switching when compared with the other existing converters. Hence, the conduction losses are reduced thereby increasing the overall efficiency of the system. The proposed system is therefore a good alternative for harvesting the maximum amount of power from a solar PV array and can replace the existing maximum power point tracking controllers available in the market.

VII. CONCLUSION

The cubic boost converter provides very high voltage gain but, because of the internal resistance of the circuit, the output voltage starts decreasing at lower values of duty ratio compared to the quadratic boost converter. Nonetheless, the maximum voltage gain is higher in the case of the cubic converter. The main advantage of the cubic boost converter over the quadratic boost converter is that it provides very high voltage gain at a lower duty ratio and has better efficiency at higher loads as compared to other similar converter topologies. Therefore, the cubic boost converter can be used for high voltage applications such as solar photovoltaic arrays, and high voltage DC transmission. Moreover, the cubic boost converter

is capable of providing a very high output power at lower efficiency, hence, can be used as a converter for an electric vehicle which sometimes needs overloading, and since the overloading is for a very small duration, the efficiency can be suppressed over cost.

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