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Performance Analysis of Shared Buffer Router Architecture for Low Power Applications

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***Abstract*—Network on chip (NoC) is an emerging technology in the field of multi core interconnection architecture. The routers plays an essential components of Network on chip and responsible for packet delivery by selecting shortest path between source and destination. State-of-the-art NoC designs used routing table to find the shortest path and supports four ports for packet transfer, which consume high power consumption and degrades the system performance. In this paper, the multi port multi core router architecture is proposed to reduce the power consumption and increasing the throughput of the system. The shared buffer is employed between the multi ports of the router architecture. The performance of the proposed router is analyzed in terms of power and current consumption with conventional methods. The proposed system uses Modelsim software for simulation purposes and Xilinx Project Navigator for synthesis purposes. The proposed architecture consumes 31 mW on CPLD XC2C64A processor.**

***Index Terms*—Shared buffer, router, multi core, power consumption**

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I. INTRODUCTION

Generally, routers consist of the following basic components: several network interfaces to the attached networks, processing module(s), buffering module(s), and an internal interconnection unit (or switch fabric). The basic functionalities in a router can be categorized as: route processing, packet forwarding, and router special services. The two key functionalities are route processing (i.e., path computation, routing table maintenance, and reachability propagation) and packet forwarding. Typically, packets are received at an inbound network interface, processed by the processing module and, possibly, stored in the buffering module. Then, they are forwarded through the internal interconnection unit to the outbound interface that transmits them on the next hop on the journey to their final destination. The aggregate packet rate of all attached network interfaces needs to be processed, buffered and relayed. Therefore, the processing and memory modules may be replicated either fully or partially on the network interfaces to allow for concurrent operations.

The routing problem is typically solved in two steps: Global routing and detailed routing. Global routing in VLSI (very large scale integration) design is one of the most challenging discrete optimization problems in computational theory and practice. In Global Routing, we generate a loose route for each network. In fact it assigns a list of routing regions to each network without specifying the actual geometrical layout of wires. In Detailed Routing, the exact geometric design within the dedicated routing regions of each network is found out.

The proposed algorithm ensures all routing demands to be satisfied at a reduced design cost. Traditionally, VLSI

routing is an important design step in the sense that the quality of routing solution has great impact on various design metrics such circuit timing, power consumption, chip reliability and manufacturability, etc. Moreover the instance sizes that occur in practice can be enormous.

Therefore, in this paper, in order to facilitate the development of a better router and routing flow, we propose a VLSI based router architecture with reduced chip size, less power consumption and low complexity without deteriorating the speed and performance. The related works in the design of router architecture is described in Section 2, the proposed multi port router architecture is described in Section 3, the Section 4 depicts the results and discussion and finally the Section 5 depicts the conclusion.

II. RELATED WORKS

In [1], the advantages of routing and interworking have been combined and Multi-Protocol Label Switching (MPLS) has been proposed in the Network layer and Data Link Layer. The authors proposed a constraint based routing algorithm for MPLS networks which makes use of both delay constraints and bandwidth. The path delay is calculated using the algorithm and the residual bandwidth of every link must be equal to or greater than the bandwidth constraint along the computed path if the path delay is less than or equal to the delay constraint. The shortest path is estimated to reduce path length based on avoiding critical links to reduce call blocking rate, path deletion of unsatisfied paths to simplify the algorithm.

Sowmya *et al.* [2] provided a onetime networking solution by means of merging the VLSI field with the networking field. Networking router today are with minimum pins and to enhance the network we go for the bridging loops which effect the latency and security concerns with protocol switching technique embedded in the router engine itself. This paper is based on the hardware coding which gave a great impact on the latency issue as the hardware itself will be designed according to the need. They provided a multipurpose networking router by means of Verilog code with which the same switching speed with more security is maintained. Their paper mainly focused on the implementation of hardware IP router which processes multiple incoming IP packets with different versions of protocols simultaneously with the purpose of increasing switching speed of a routing per packet for both the current trend protocols.

An algorithm based on net merging method was proposed for three-layer channel routing by Chen and Liu [3]. Individual routing methods are considered for the VHV (Vertical-Horizontal-Vertical) and HVH (Horizontal-Vertical-Horizontal) routing models. The extension of Left Edge Algorithm (LEA) is assigned for VHV model in which all the horizontal wire segments are assigned to the horizontal layer, all upward and downward vertical wire segments are assigned to each vertical layer, whereas merging techniques are used in HVH by merging the nets in the same zone (parallel merging) or between two different zones (serial merging).

A new technique called ‘Chameleon’ was proposed by Braunt *et al.* [4] for routing general multi-layer channels. Different ranges of technology constraints were handled by this method, i.e. line width and line-to-line spacing can be individually stated for each layer and controls the allowing of contact stacking. Their technique has been applied in a new multi-layer channel router.

In [5], a survey has been made on some important multi-layer routing algorithms. The authors analyzed the Efficient Routing algorithm and resolved horizontal constraints to minimize the net wirelength in a particular model of channel routing using MCC1 and MCC2 algorithms. Then, an algorithm for multi-channel routing was considered and compared with ‘Chameleon’, which is another multi-channel routing algorithm in the two-layer VH and three-layer HVH routing models. Particle swarm optimization (PSO) has been proposed in various works [6-8] for VLSI routing. These techniques find the minimum cost of Rectilinear Steiner Minimal Tree (RSMT), which is a NP-problem.

A heuristic approach to find the optimal routing path and buffer location simultaneously for minimal interconnect delay was presented in [8] and in [7], Prim's Algorithm was modified and implemented as a principle of finding the cost of the RSMT. Dong *et al.* [6] proposed a routing algorithm based on improved Discrete PSO in which a novel encoding for DPSO and update functions are performed to find the RSMT. The results of these methods [6-8] were compared with conventional methods and proved to give a better routing optimization.

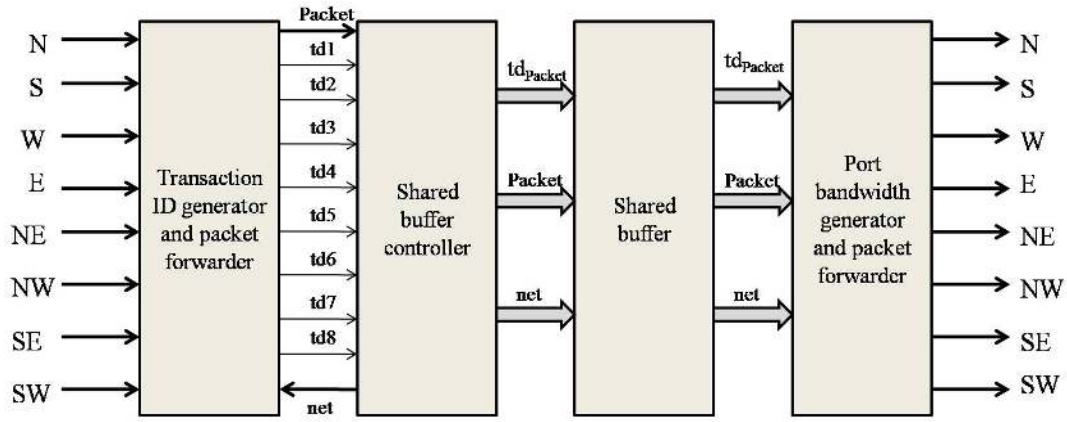

Fig. 1. Architecture of proposed router.

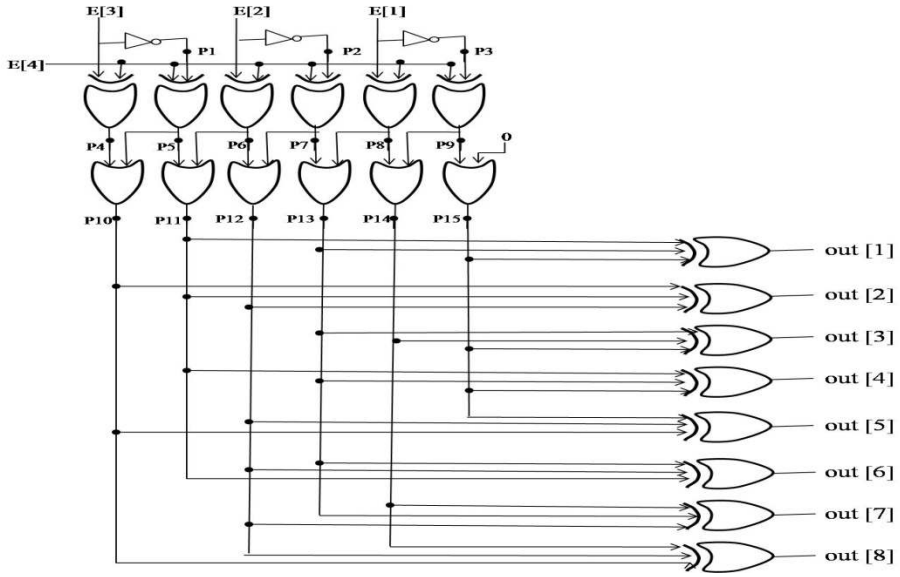

Fig. 2. Architecture of Transaction ID generating circuit.

Mattihalli *et al.* [9] adopted bridging loops to reduce the latency and security concerns. They proposed a multipurpose networking router by means of Verilog code and generate the code as a self-independent VLSI based router. Their method enabled the router to process multiple incoming IP packets simultaneously with different versions of protocols and produced an increased routing switching speed.

III. Proposed 8-port Router Design

The proposed router architecture design is shown in Fig. 1. It consists of Transaction ID generator, shared buffer with a controller, port bandwidth generator and packet forwarder. Each module is explained individually in the upcoming sections.

1. Transaction ID Generator

The Transaction ID generator provides a logical transaction and continuity among the packets by assigning unique IDs to each packet as identification in a transmitter or receiver. Appropriate generation of Transaction IDs for every individual transaction is necessary to avoid persistent losses in transactions due to duplications in IDs. The architecture of Transaction ID generator is shown in Fig. 2.

2. Shared Buffer and Controller

The shared buffer is used to choose the packets from the desired direction. Its decision depends on the value of ‘Net’ and the method of selection of packets is shown in

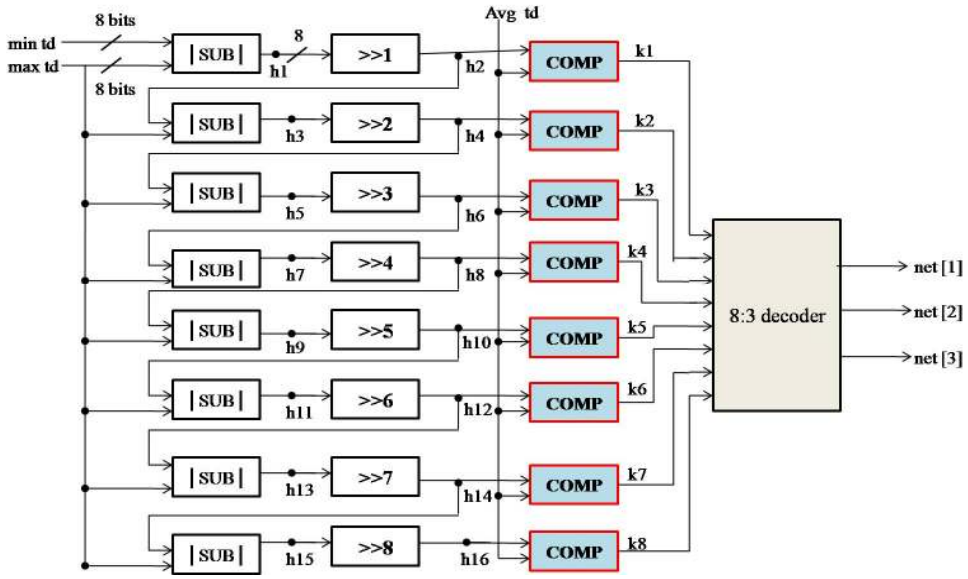

Fig. 3. Shared buffer controller.

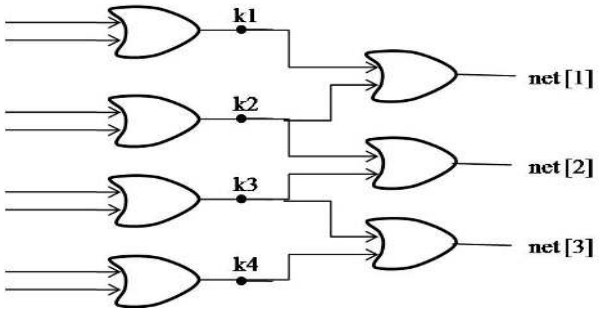

Fig. 4. Structure of 8×3 decoder unit.

Table 1. Packet selection

Net value	Shared buffer
000	Packets from North port
001	Packets from East port
010	Packets from South port
011	Packets from West port
100	Packets from North-east port
101	Packets from North-west port
110	Packets from South-east port
111	Packets from South-west port

Table 1. The design of shared buffer controller unit is shown in Fig. 3 and the decoder used in it is shown in Fig. 4.

3. Port Bandwidth Generator

Bandwidth generator allocates bandwidth for the process and minimizes the bandwidth usage under bandwidth-limited constraints also maintaining a stable Rate-Distortion performance. Overflow in bandwidth usage leads to encoding delays, thus causing a failure of real-time constraints and leading to frame dropping, i.e. loss in quality. Fig. 5 shows the port bandwidth generator circuit implemented with multiplexers, adders, subtractors and binary-to-integer converter at low hardware cost. If there is not enough bandwidth available, the weights are zero. The port weights for eight directions (North, South, West, East, North-east, North-west, South-east, and South-west) are given in Eqs. (1-8).

$$w_N = \begin{cases} b_N \times |y_d - y| + b_{max}, & y_d - y < 0 \\ 0, & b_N < b_p \\ b_N, & else \end{cases} \quad (1)$$

$$w_S = \begin{cases} b_S \times (y_d - y) + b_{max}, & y_d - y > 0 \\ 0, & b_S < b_p \\ b_S, & else \end{cases} \quad (2)$$

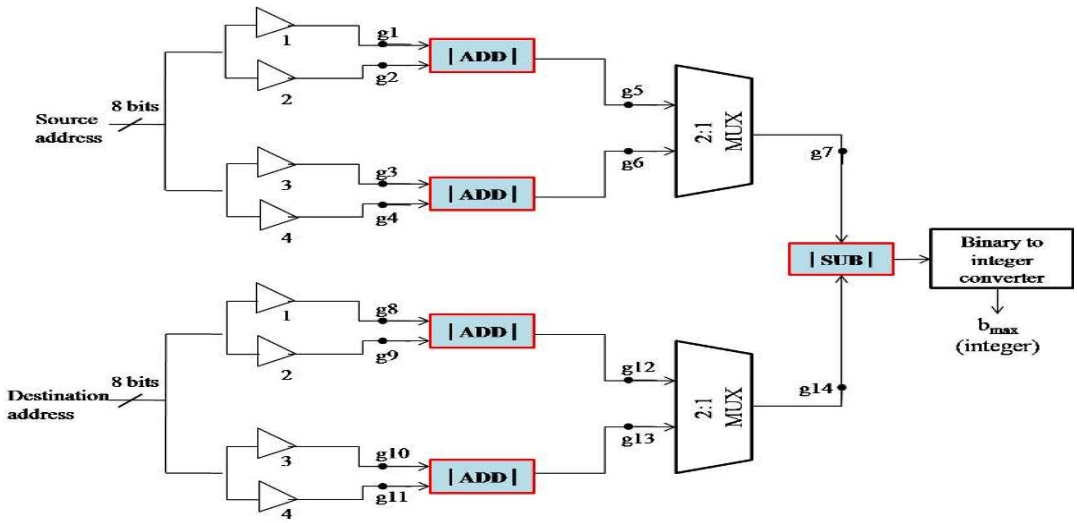

Fig. 5. Port bandwidth generator.

$$w_W = \begin{cases} b_W \times |x_d - x| + b_{max}, & x_d - x < 0 \\ 0, & b_w < b_p \\ b_W, & else \end{cases} \quad (3)$$

$$w_E = \begin{cases} b_E \times (x_d - x) + b_{max}, & x_d - x > 0 \\ 0, & b_E < b_p \\ b_E, & else \end{cases} \quad (4)$$

$$w_{NE} = \begin{cases} (b_N + b_E) \times (y_d - x_d) + b_{max}, & y_d - x_d < 0 \\ 0, & (b_N + b_E) < b_p \\ b_N + b_E, & else \end{cases} \quad (5)$$

$$w_{NW} = \begin{cases} (b_N + b_W) \times (y_d + x_d) + b_{max}, & y_d + x_d > 0 \\ 0, & (b_N + b_W) > b_p \\ b_N + b_W, & else \end{cases} \quad (6)$$

$$w_{SE} = \begin{cases} (b_S + b_E) \times (y_d - x_d) + b_{max}, & y_d - x_d < 0 \\ 0, & (b_S + b_E) < b_p \\ b_S + b_E, & else \end{cases} \quad (7)$$

$$w_{SW} = \begin{cases} (b_S + b_W) \times (y_d + x_d) + b_{max}, & y_d + x_d > 0 \\ 0, & (b_S + b_W) > b_p \\ b_S + b_W, & else \end{cases} \quad (8)$$

where b_N= North port bandwidth; b_S= South port bandwidth; b_E= East port bandwidth; b_W= West port bandwidth; b_{max}= Maximum available bandwidth; b_p=Minimum port bandwidth; W_N = North port weight; W_E = East port weight; W_S = South port weight; W_W = West port weight; W_{NE} = North East port weight; W_{NW} = North West port weight; W_{SE} = South East port weight; W_{SW} = South West port weight. x_d, y_d represents destination latitude and longitude, respectively. x, y represents router latitude and longitude, respectively.

The maximum port weight is determined by maximum of $\{w_N, w_S, w_W, w_E, W_{NE}, W_{NW}, W_{SE}, W_{SW}\}$. The packet will be transmitted through the output port, whose port weight is maximum.

IV. Results and Discussion

To evaluate the performance of the proposed scheme, we consider erroneous port which creates errors in other ports of the corresponding router itself. The proposed system architecture has minimal hardware utilities which provides low power consumption and reduces the routing latency in the router network on chip.

We have used Modelsim 6.1e as simulation software and Xilinx project navigator 12.1 as synthesis software to evaluate the proposed network on chip router. By analyzing the results from simulation, it shows that it produces the tolerable packet error rate and also the synthesis result shows that low hardware utilization such as 48 adders, 128 XOR gates and 0.031 mW of power consumption, respectively. The simulation results of packets being routed to different directions are depicted in Fig. 6.

Fig. 6(a) shows the packet transmission on NORTH port, Fig. 6(b) shows the packet transmission on EAST port, Fig. 6(c) shows the packet transmission on SOUTH port, Fig. 6(d) shows the packet transmission on WEST port, Fig. 6(e) shows the packet transmission on NORTH-EAST port, Fig. 6(f) shows the packet transmission on NORTH-WEST port, Fig. 6(g) shows the packet transmission on SOUTH-EAST port, Fig. 6(h)

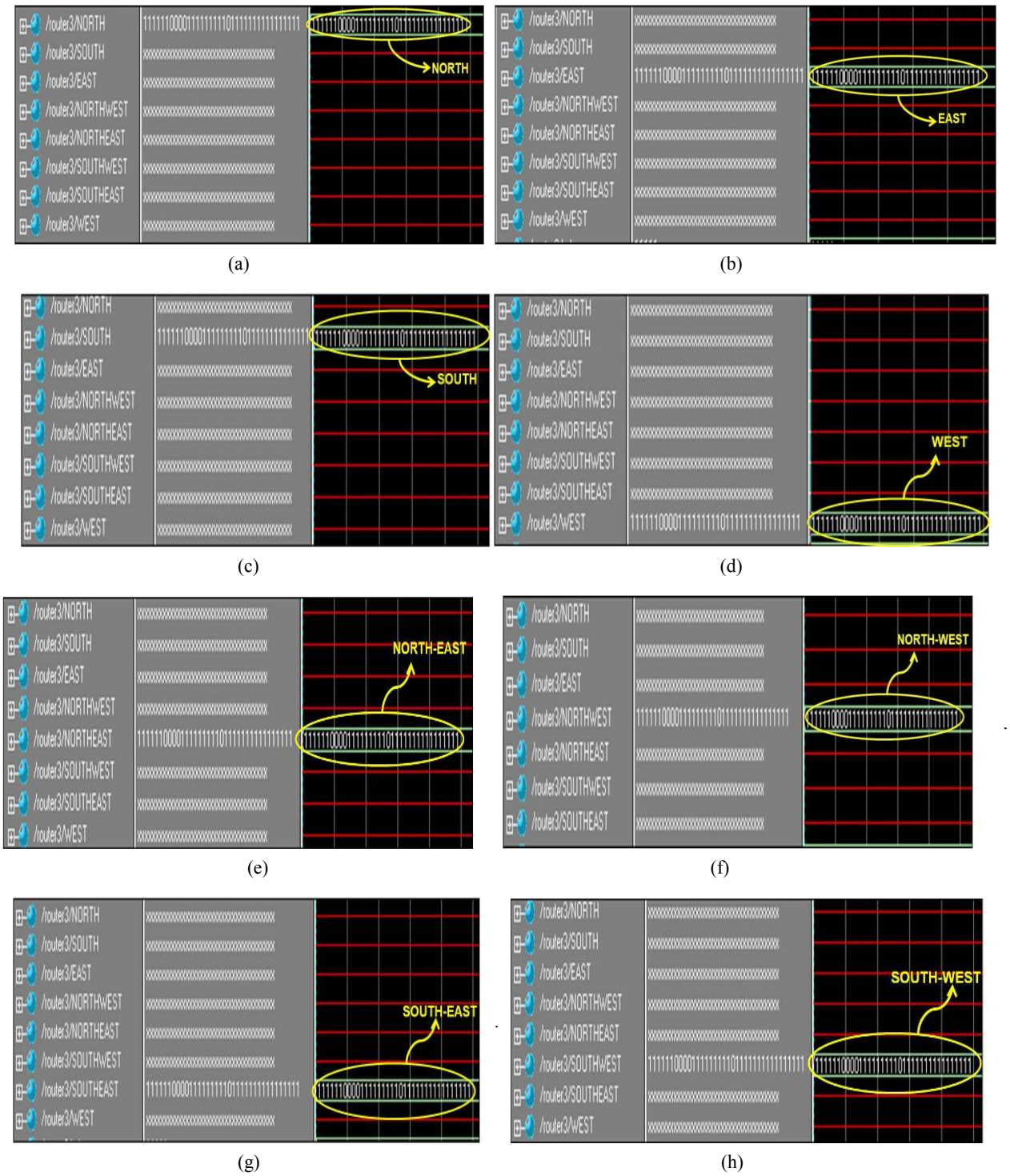

Fig. 6. Packets forwarded to (a) NORTH, (b) EAST, (c) SOUTH, (d) WEST (e) NORTHEAST, (f) NORTHWEST, (g) SOUTHEAST, (h) SOUTHWEST ports.

shows the packet transmission on SOUTH-WEST port.

The design of proposed router in its chip view is shown in Fig. 7(a) and Let us assume the packet is entering the router at WEST port; Register Transfer Logic (RTL) shows the cross sectional top view of the design and depicted in Fig. 7(b). Technology schematic shows the cross sectional front view of the design and shown in Fig. 7(c). The slices and Look-up-tables (LUT) are presented in RTL and technology view. The chip summary of various devices is summarized in Table 2.

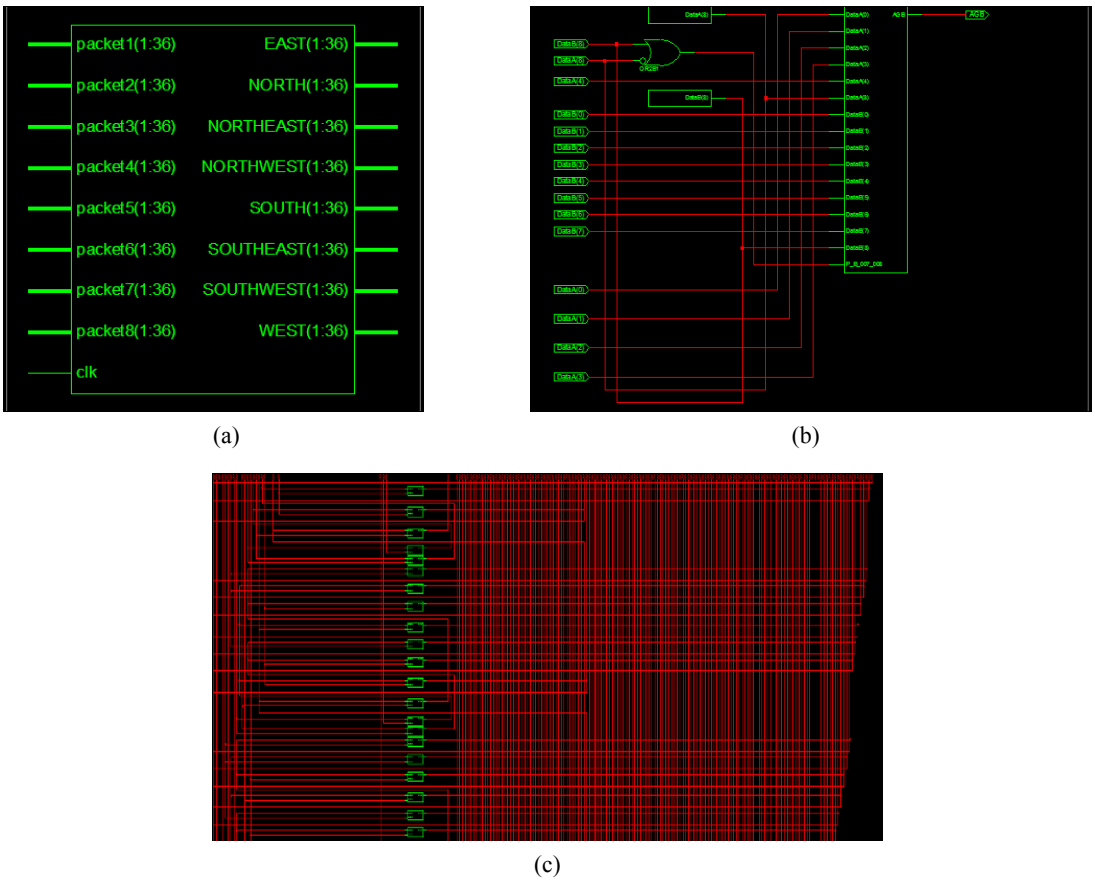

Fig. 7. (a) IC View, (b) RTL Schematic view, (c) Technology Schematic view.

Table 2. Chip summary

Device	Package	Speed Grade
XC2C64A,XC2C128	VQ100	-7
XC2C256	FT256	-7
XC2C384	FG324	-7
XCR3032XL	PC44	-5

Table 3. Performance analysis of power and current consumption

Device	Power Consumption (mW)	Current Consumption (mA)
XC2C64A	31	17
XC2C128	34	19
XC2C256	38	21
XC2C384	40	23
XCR3032XL	89	27

Table 3 represents the power consumption (mW) and current consumption (mA) of the proposed methodology (with respect to the condition of the Eqs. (1-8) using Xilinx project navigator synthesis tool, by implementing the proposed routing method on different CPLD processors. From Table 3, it is clearly shows that the linear relationship of power consumption with current consumption. The CPLD processor XCR3032XL consumes more current as 27 mA than the other processors.

Table 4. Performance evaluation of resource utilizations

Hardware Utilizations	Consumption results
Adders	48
XORs	128
Comparators	18
Memory Usage	128952KB

The hardware utilizations (Adders, XORs, Comparators and Memory Usage) are clearly shown in Table 4. It is clearly shows that the proposed method consumes less hardware. The proposed method is also compared with other existing routing algorithms in terms of power consumption and shown in Table 5.

Fig. 8 shows the graphical illustrations (X-axis represents the proposed and conventional methods , Y-axis represents the power consumption in mW) of the power consumption for proposed method with conventional methods Killian *et al*. [10], Banerjee *et al*.

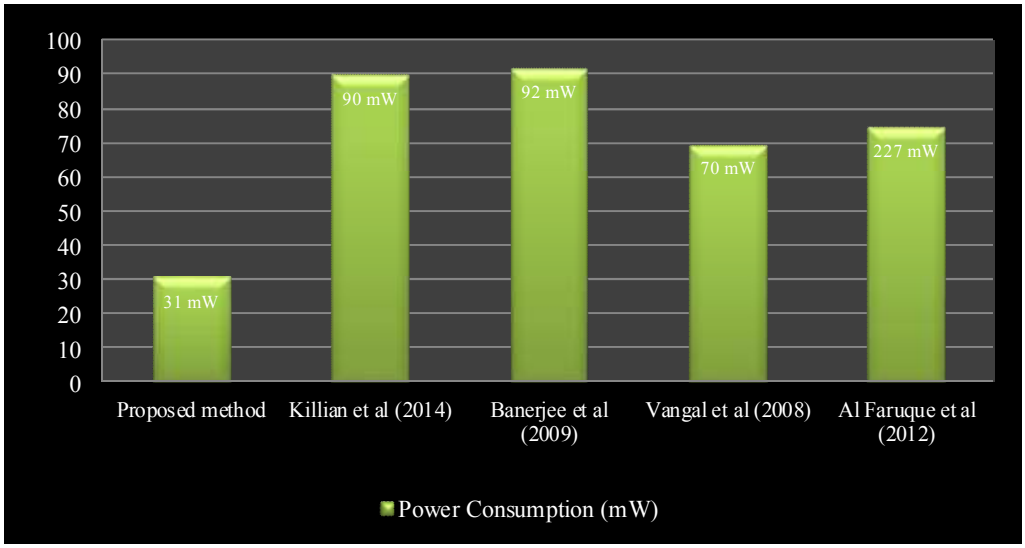

Fig. 8. Graphical illustration of comparison of power consumptions.

Table 5. Performance comparison of power consumption

Methodology	Year	Power Consumption (mW)
Proposed	2016	31
Killian *et al.* [10]	2014	90
Banerjee *et al.* [11]	2009	92
Vangal *et al.* [12]	2008	70
Al Faruque *et al.* [15]	2012	75

[11], Vangal *et al*. [12], Shacham *et al*. [13], Pham *et al*. [14] and Al Faruque *et al*. [15]. From Fig. 8, it is clearly shows that the proposed method consumes less power than the conventional methods stated in Table 5. The power consumption of the proposed methodology and conventional methodology ([10-15]) are measured using Xilinx Project Navigator 12.1(power prime) tool.

V. CONCLUSION

This paper has presented an efficient port bandwidth weight based routing architecture to route the packets from source to destination. The proposed router does not maintain any routing table to route the packets from source to destination. This paper depicts the multi port such as eight port architecture of router based on port bandwidth. The performance of the proposed router is analyzed in terms of power and current consumption with conventional methods.

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