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Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node

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***Abstract*—The performance and threshold voltage variability of fully depleted silicon-on-insulator (FD-SOI) MOSFETs are compared against those of conventional bulk MOSFETs via 3-D device simulation with atomistic doping profiles. Compact (analytical) modeling is then used to estimate six-transistor SRAM cell performance metrics (i.e., read and write margins, and read current) at the 22 nm CMOS technology node. The dependences of these metrics on cell ratio, pull-up ratio, and operating voltage are analyzed for FD-SOI versus bulk SRAM cells. Iso-area and iso-yield comparisons are then made to determine the yield and cell-area benefits of FD-SOI technology, respectively. Finally, the minimum operating voltages ($V_{\min}$) required for FD-SOI and bulk SRAM cells to meet the six-sigma yield requirement are compared.**

***Index Terms*—CMOS, MOSFET, silicon-on-insulator (SOI), SRAM, variability.**

I. Introduction

INCREASING variation in transistor performance with gate-length (L_{GATE}) scaling is a major challenge for continued bulk CMOS technology advancement [1]. The primary causes for random variations in transistor threshold voltage (V_{TH}) are gate line-edge roughness (LER) and random dopant fluctuations (RDFs) [2]. A lightly doped (fully depleted, FD) silicon-on-insulator (SOI) MOSFET structure with a very thin ($\sim$10 nm thick) buried oxide (BOX) layer and a heavily doped substrate ("ground plane") has been shown to be effective for reducing the impact of parameter variations and RDF due to its excellent electrostatic integrity and the elimination of channel doping [3]. Recently, functional SRAM cells were demonstrated using such FD-SOI devices, for the 32 nm technology node and beyond [4]. Furthermore, thin-BOX FD-SOI MOSFET technology has been projected to provide for improved SRAM yield as compared to SOI FinFET technology at the 22 nm technology node [5]. In this paper, which follows [6], the potential advantages of thin-BOX FD-SOI technology versus bulk CMOS technology with regard to six-transistor (6-T) SRAM cell performance and yield are assessed in detail for the 22 nm technology node.

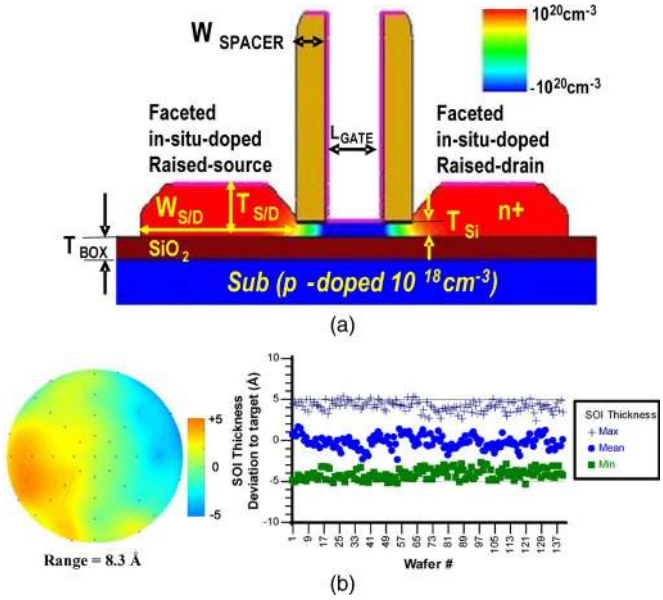

Fig. 1. (a) Cross-sectional view of the simulated thin-BOX FD-SOI MOSFET structure. The gate electrode is a thin metal layer with a specified work function. (b) Experimental data (courtesy of Soitec) for SOI layer thickness (T_{Si}) variation across a wafer (left) and from wafer to wafer (right). The peak-to-peak variation is less than 1 nm.

II. Thin-BOX FD-SOI Technology

A. MOSFET Design Optimization

The thin-BOX FD-SOI CMOSFET designs were optimized via 3-D process and device simulations with advanced physical models including the density–gradient and drift–diffusion transport models [7] and the phenomenological van Dort quantum correction model to account for energy quantization in the channel region. Physical and operating parameters (e.g., gate length, gate oxide thickness, and supply voltage) were taken from the International Technology Roadmap for Semiconductors for low-operating-power (LOP) technology at the 22-nm node [8]. The width of the gate-sidewall spacers (W_{spacer}) is constrained by the gate-to-contact spacing design rule for the 6-T SRAM cell and was selected to be 15 nm based on [10] and in consideration of the design optimization guidelines in [9]. Fig. 1(a) shows a cross-sectional view of the simulated

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TABLE I
OPTIMIZED THIN-BOX FD-SOI AND BULK (UNIFORM CHANNEL DOPING $\sim 10^{18}$ cm^{-3}) MOSFET DESIGN PARAMETERS FOR $V_{\rm DD} = 0.9$ V

	FD-SOI		Bulk	
Parameter	N-type	P-type	N-type	P-type
L_{GATE}	25nm	25nm	25nm	25nm
W_{SPACER}	15nm	15nm	15nm	15nm
T_{OX}	1nm	1nm	1nm	1nm
T_{BOX}	10nm	10nm	NA	NA
T_{Si}	6nm	6nm	NA	NA
$X_{J,EXT}$	NA	NA	10nm	10nm
$X_{J,S/D}$	NA	NA	22nm	22nm
Φ_M	4.45eV	4.85eV	4.05eV	5.20eV
$T_{S/D}$	22.6nm	22.6nm	NA	NA
$W_{S/D}$	72nm	72nm	72nm	72nm

n-channel MOSFET structure. An implantation-free process is used as follows in order to avoid dopant-atom straggle and defects in the thin body region to minimize RDF-induced variations [10]: faceted raised-source/drain regions are formed by a low-temperature zero-silicon-loss epitaxial growth process with *in situ* doping (10^{20} cm^{-3}) to reduce series resistance with minimal increase in gate-sidewall capacitance; then the lightly doped source/drain extension regions are formed by diffusion of dopant atoms from the raised-source/drain regions. The electrical channel length ($L_{\rm eff}$, defined as the distance between the lateral positions where the source and drain doping concentrations fall to 2×10^{19} cm^{-3} [11]) is tuned by adjusting the duration of the dopant-diffusion anneal step to achieve the maximum drive current for a gate voltage swing and drain bias equal to the supply voltage $V_{\rm DD}$ (0.9 V). The gate work function values were then selected to adjust the nominal $V_{\rm TH}$ values in order to meet the OFF-state leakage current ($I_{\rm OFF}$) specification, i.e., 3 nA/μm. The optimized device parameters for the FD-SOI devices are summarized in Table I.

For comparison, bulk CMOSFETs meeting the same $I_{\rm OFF}$ specification also were designed (Table I). Fig. 2 compares the transfer characteristics ($I_{\rm DS}$ versus $V_{\rm GS}$) for the optimized n-channel FD-SOI and bulk MOSFET structures. The FD-SOI device exhibits a steeper subthreshold slope due to negligible depletion capacitance and higher drive current due to higher carrier mobility. A summary comparison of device performance parameters is given in Table II. Both the FD-SOI and bulk MOSFET structures meet the general specification for drain-induced barrier lowering (DIBL) to be no greater than 100 mV/V. (DIBL for the bulk devices is comparable to that of the FD-SOI device because of the very shallow source/drain extension depths.)

An analytical I–V model for the short-channel MOSFET [see (1)] was fit to the simulated current-versus-voltage characteristics and then used to compute SRAM metrics such as read static noise margin (SNM) [12], [14], write current (I_w) [13], [14], and read current, following the methodology described in [22]. Five simulated I–V targets corresponding to the operating biases most critical for modeling SRAM metrics, i.e., $(V_{\rm GS}, V_{\rm DS}) = (1.0\ {\rm V}, 0.1\ {\rm V})$, (1.0 V, 1.0 V), (0.5 V, 1.0 V), (1.0 V, 0.5 V), and (0.0 V, 1.0 V), in addition to

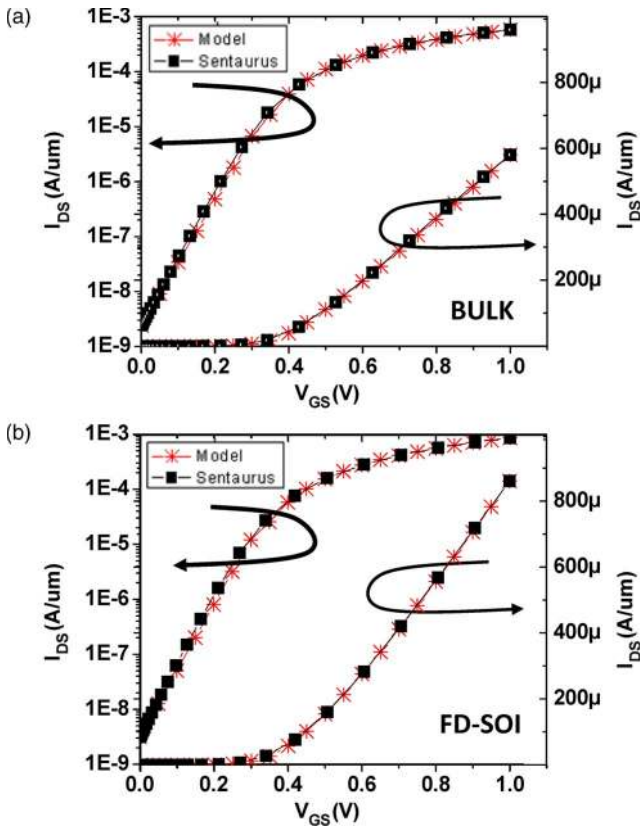


Fig. 2. Transfer characteristics. (a) Bulk MOSFET. (b) FD-SOI MOSFET. The analytical I–V model is fit (to within 5%) to the simulated characteristics, using the current values at 6 points: $(V_{\rm GS}, V_{\rm DS}) = \{(1.0, 1.0), (1.0, 0.5), (1.0, 0.1), (0.5, 1.0), (0.5, 0.1), (0.0, 1.0)\}$.

TABLE II
COMPARISON OF DEVICE PERFORMANCE PARAMETERS FOR $V_{DD} = 0.9$ V

V_{DD}= 0.9V	FD-SOI		Bulk	
	N-type	P-type	N-type	P-type
I_{ON} [μA/μm]	704	417	483	301
I_{OFF} [nA/μm]	3	3	3	3
SS [mV/dec]	75	83	81	89
$V_{T,LIN}$ [mV]	164	-186	182	-207
$V_{T,SAT}$ [mV]	118	-124	134	-142
DIBL [mV/V]	54.1	72.9	56.5	76.5
L_{eff} [nm]	35.6	30.7	46.1	40.5

linear ($V_{\rm DS} = 0.1$ V) and saturation ($V_{\rm DS} = 1.0$ V) threshold voltage values, were used to fit the analytical I–V model for each case of $+10\%$ or -10% variation in channel length (L), channel width (W), gate oxide thickness ($T_{\rm ox}$) or $V_{\rm TH}$. Linear interpolation or extrapolation was then used to obtain the analytical I–V curves for arbitrary variations in L, W, $T_{\rm ox}$, and $V_{\rm TH}$, which were then used to compute the SRAM metrics. L, W, and $T_{\rm ox}$ are assumed to have Gaussian distribution (with 3-sigma corresponding to $\pm 10\%$), while the standard deviation in $V_{\rm TH}$ due to random variations was determined as described in Section II-B.

B. Impact of Random Variations

The impacts of gate LER and RDF were evaluated via 3-D device and process simulations with atomistic doping profiles [7]. A scanning electron microscopy image of photoresist lines processed for the 22-nm node was sampled 100 times to provide the realistic gate electrode profiles for 3-D device simulations. Thirty kinetic Monte Carlo simulations—which account for reactions between defects and impurities as predicted by molecular dynamics—were performed for each of these gate electrode profile cases. The source/drain extensions in the bulk structure are formed by dopant ion implantation; the resultant defects result in larger $I_{\rm dsat}$ variation for the bulk structure. In contrast, the source/drain extensions in the FD-SOI structure are formed by dopant diffusion; because implant damage is avoided, less $I_{\rm dsat}$ variation (and smaller $\sigma(V_{\rm TH})$) is seen for the FD-SOI structure. The device simulation results are shown in Fig. 3. The impact of gate work function variations (WFVs) can be significant for nanometer-scale MOSFETs. Based on [15], $\sigma(V_{\rm TH})$ due to WFV is estimated to be 12.4 mV for the pull-down transistors in the 22-nm-node SRAM cell. Under the assumption that WFV is statistically independent of gate LER and RDF [16], the total $V_{\rm TH}$ variation is calculated as follows:

$$\sigma(V_{\rm TH})|_{\rm Total,\,random} \approx \sqrt{\sigma(V_{\rm TH})^2|_{\rm LER} + \sigma(V_{\rm TH})^2|_{\rm RDF} + \sigma(V_{\rm TH})^2|_{\rm WFV}}.$$

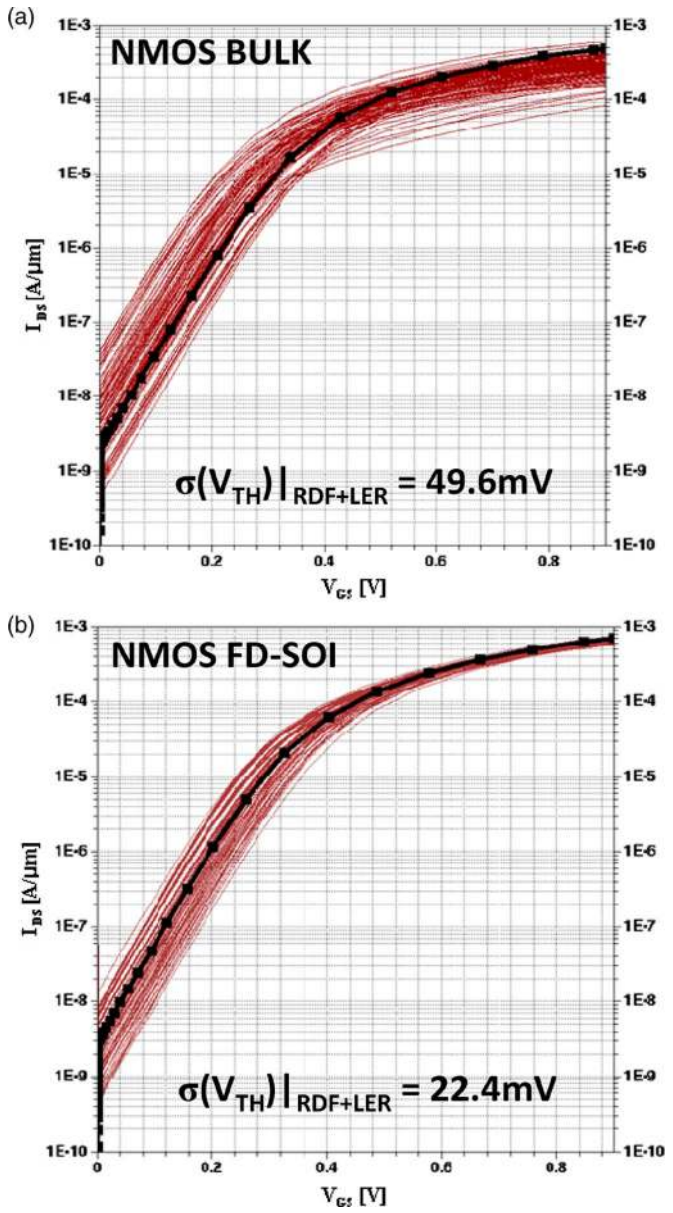


Fig. 3. Simulated transfer characteristics of the pull-down transistor for 500 cases of gate-LER and atomistic doping. (a) Bulk MOSFET (b) FD-SOI MOSFET. $V_{\rm DD} = 0.9$ V. The simulated transfer characteristics for continuum doping are also shown (with thicker lines) for reference.

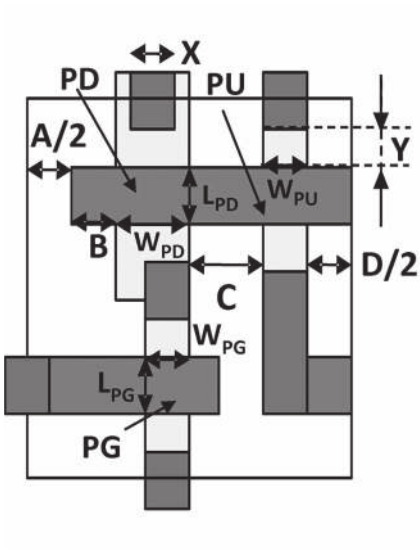
Due to reduced $V_{\rm TH}$ roll-off and light channel doping, the FD-SOI structure provides for a $V_{\rm TH}$ variation smaller than that of the bulk structure: $\sigma(V_{\rm TH})|_{\rm SOI} = 26$ mV versus $\sigma(V_{\rm TH})|_{\rm BULK} = 50$ mV. It also shows less lowering of the average value of $V_{\rm TH}$ due to atomistic doping effects.

III. SIX-TRANSISTOR SRAM CELL PERFORMANCE COMPARISON

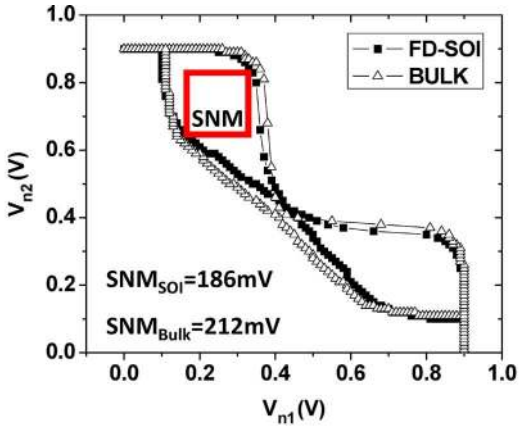
A. Nominal Cell Design

Based on recent publications [17]–[21], the dimensions for 22-nm-node 6-T SRAM cells were selected for this study. The cell layout parameters are summarized in Table III. Fig. 4(a) and (b) shows the butterfly plots and write-N curves, respectively, obtained using the analytical I–V model.

TABLE III
FD-SOI 6-T SRAM CELL DIMENSIONS. A HALF-BIT CELL IMAGE IS SHOWN ON THE LEFT SIDE



Design rules		Symbol	Size [nm]
Cell Height	PG CH length	L_{PG}	25
	PD CH length	L_{PD}	25
	CONT size	X	30
	Gate-to-CONT	Y	20
	Total	190	
Cell Width	POLY-to-POLY	A	30
	POLY-to-DIF ext	B	20
	PD Width	W_{PD}	55
	N/P isolation	C	50
	PU width	W_{PU}	32
	DIF-DIF (min)	D	50
	PG width	W_{PG}	35
	Total	394	
A SRAM cell area		0.07486 μm²	



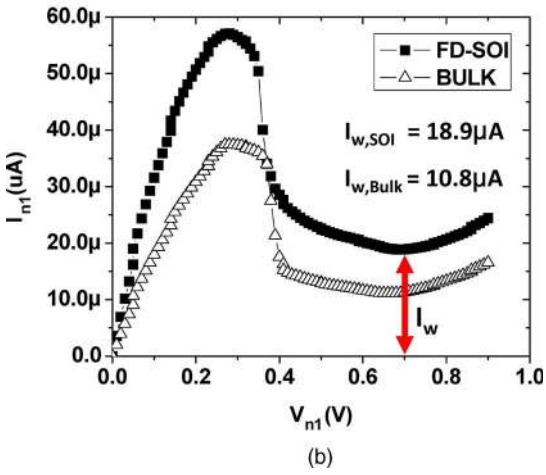


Fig. 4. Comparisons of (a) SNM and (b) write current (I_w), for $V_{DD} = 0.9$ V. The write-ability of the FD-SOI SRAM cell is larger by 71%, but the SNM is lower by 10%.

Although the FD-SOI cell has a slightly lower SNM due to its lower switching voltage, it has higher write-ability (∼70% higher I_w) and read current (∼60% higher $I_{\rm read}$). Thus, the FD-SOI cell offers a better tradeoff between read stability and write-ability, as compared to the bulk cell.

B. Dependency of SRAM Performance Metrics on Cell Ratio, Pull-Up Ratio, and V_{DD}

For a fixed cell area, there is room to adjust the width of the pass-gate transistors ($W_{\rm PG}$) in order to optimize the tradeoff between the various SRAM performance metrics (i.e., SNM, I_w, and $I_{\rm read}$). This is because the SNM increases with increasing cell (β) ratio ($= W_{\rm PD}/W_{\rm PG}$), which decreases with increasing $W_{\rm PG}$; I_w increases with decreasing pull-up (α) ratio ($= W_{\rm PU}/W_{\rm PG}$), which decreases with increasing $W_{\rm PG}$; and $I_{\rm read}$ increases directly with $W_{\rm PG}$. Fig. 5(a)–(c) shows the dependences of SNM, I_w, and $I_{\rm read}$ on cell ratio, pull-up ratio, and $W_{\rm PG}$, respectively. The improved tradeoff between read stability and write-ability offered by the FD-SOI cell can be evaluated graphically using these figures. For example, the FD-SOI can achieve comparable SNM (∼212 mV) as the bulk cell if $W_{\rm PG}$ is decreased to 27.2 nm (so that cell ratio $= W_{\rm PD}/W_{\rm PG} = 55$ nm/27.2 nm $= 2.02$, and pull-up ratio $= W_{\rm PU}/W_{\rm PG} = 32$ nm/27.2 nm $= 1.18$), in which case I_w (∼12.4 μA) is still 15% higher than that for the bulk cell (∼10.8 μA), and $I_{\rm read}$ (∼15.5 μA) is still 34% higher than that for the bulk cell (11.6 μA). Fig. 6 compares the dependences of SNM, I_w, and $I_{\rm read}$ on $V_{\rm DD}$ for this case (in which $W_{\rm PG}$ is reduced to 27.2 nm for the FD-SOI cell). The FD-SOI benefit of improved write-ability (I_w) and speed ($I_{\rm read}$) for comparable read stability (SNM) is retained as $V_{\rm DD}$ is reduced.

IV. YIELD-AWARE SRAM CELL DESIGN

In Section III, the FD-SOI cell was shown to offer improved tradeoff between the nominal values of SNM and I_w for a fixed cell area. In this section, the corresponding improvement in cell yield is evaluated using the concept of cell sigma, defined as the minimum amount of variation for read/write failure [22]. Assuming that the metric (SNM or I_w) has a Gaussian distribution, this is simply the mean divided by the standard deviation. If a metric "f" is subject to small independent parameter variations "x_i" in a range such that "f" can be approximated as a linear

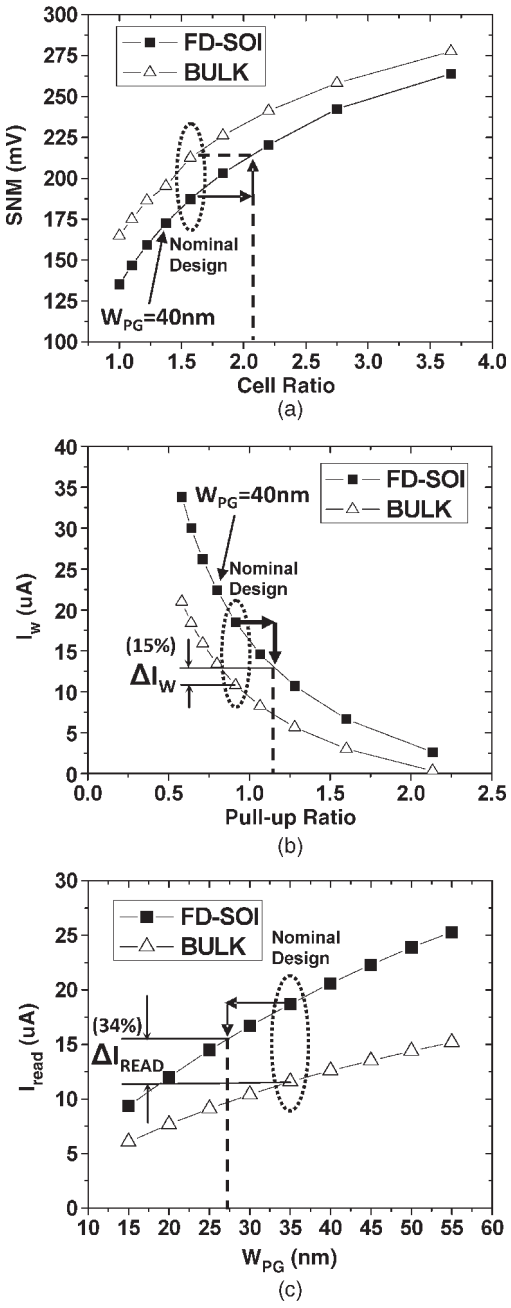


Fig. 5. Comparison of cell performance metrics for FD-SOI versus bulk 6-T SRAM cells: (a) SNM; (b) I_w; and (c) $I_{\rm read}$. (The curves are each obtained by adjusting the value of $W_{\rm PG}$.)

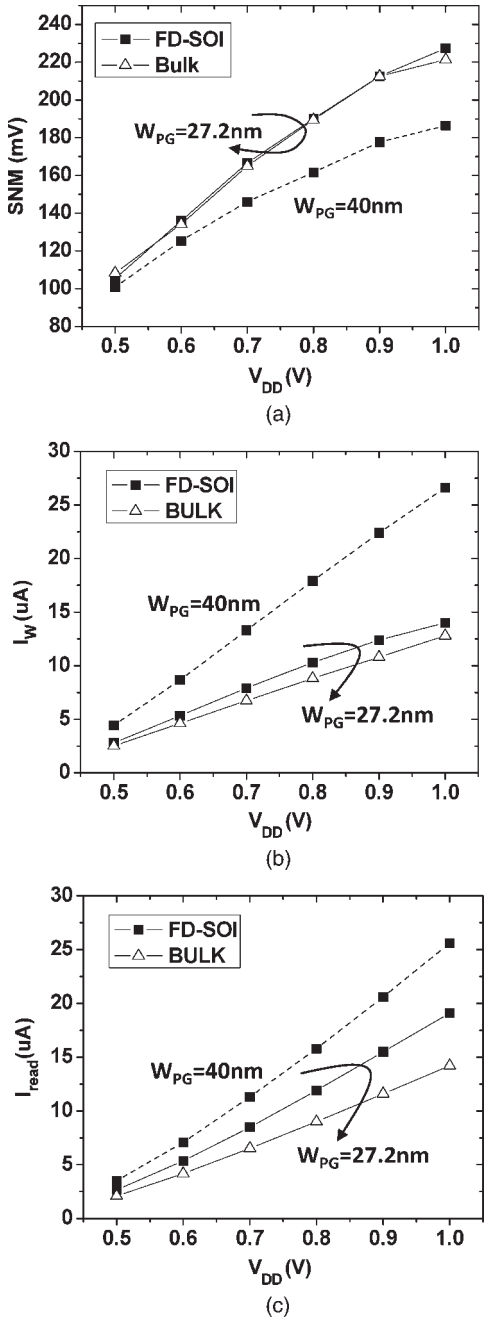


Fig. 6. Impact of $V_{\rm DD}$ scaling on 6-T SRAM cell performance metrics.

function of "x_i," then the distribution of the metric is Gaussian, according to the Central Limit Theorem. The cell sigma is given by

$$\text{cell sigma} = \frac{f(0)}{\sqrt{\sum_i \left(\frac{\partial f}{\partial x_i}\right)^2 \sigma_{x_i}^2}}.$$

It should be noted that SNM and I_w each exhibit a linear response to small variations in x_i. Although their sensitivities can become nonlinear for large variations (beyond several σ_{x_i}), the most probable combination of variations in L, W, $T_{\rm ox}$ and $V_{\rm TH}$ does not exceed $\sim 4\sigma$ variation in a single parameter. Thus, this method of estimating SRAM yield is reasonably accurate [22].

As explained above, random variations due to gate LER and RDF, as well as global (Gaussian) variations due to process-induced variations ($\pm 10\%$) in gate length, channel width, gate oxide thickness, and body thickness [Fig. 1(b)] are considered.

A. Iso-Area Comparison

In the future, six-sigma (6σ) yield or larger will be required for large SRAM arrays to be functional. Fig. 7 shows the trade-off between I_w yield and SNM yield for FD-SOI and bulk cells, for $V_{\rm DD} = 0.9$ V. ($W_{\rm PG}$ is varied along the curves.) In order for a cell design to meet the 6σ yield requirement, both SNM and I_w must be able to tolerate at least 6σ variation. The FD-SOI

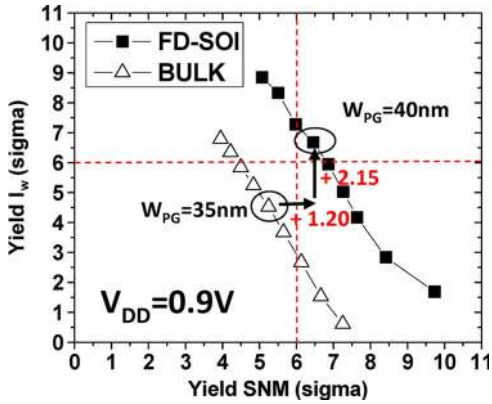


Fig. 7. Yield of I_w versus yield of SNM. The optimal design points for bulk and FD-SOI cells are indicated (corresponding to $W_{\rm PG} = 35$ nm for the optimal bulk cell and $W_{\rm PG} = 40$ nm for the optimal FD-SOI cell).

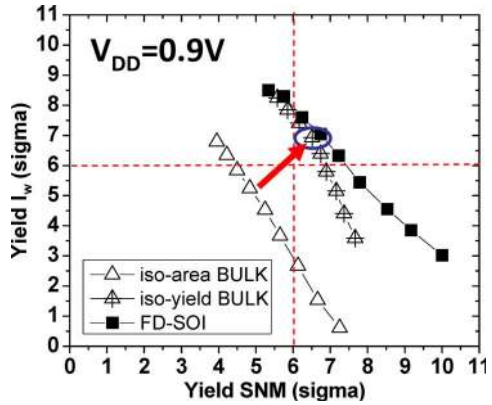


Fig. 8. By upsizing the bulk cell, yield that is comparable to that of the FD-SOI cell can be achieved. However, the tradeoff between yield of I_w and yield of SNM is more severe for the bulk cell due to lower drive current and larger random $V_{\rm TH}$ variation.

cell can satisfy the 6σ yield requirement and achieves maximum cell sigma with $W_{\rm PG} = 40$ nm. Approximately 10 nm variation in $W_{\rm PG}$ can be tolerated at this design point. In contrast, the bulk cell cannot satisfy the 6σ yield requirement. The optimal bulk cell design corresponds to $W_{\rm PG} = 35$ nm and has $\sim 1.2\sigma$ worse SNM yield and $\sim 2.2\sigma$ worse I_w yield than the FD-SOI cell.

B. Iso-Yield Comparison

In order for the bulk cell to achieve $> 6\sigma$ yield, comparable to that of the optimized FD-SOI cell (with $W_{\rm PG} = 40$ nm), the pull-down and pull-up transistor widths must be increased to $W_{\rm PD} = 95$ nm and $W_{\rm PU} = 50$ nm, respectively, so that the cell area is increased by $\sim$30% (from ~ 0.075 μm^2 to ~ 0.1 μm^2). In other words, the area savings offered by the FD-SOI cell is $\sim$25%. The resultant I_w yield versus SNM yield curve is plotted in Fig. 8, along with the curves from Fig. 7. The spotlighted design point corresponds to $W_{\rm PG} = 65$ nm.

C. Minimum Operating Voltage ($V_{\rm min}$)

By plotting I_w yield versus SNM yield for various values of $V_{\rm DD}$, $V_{\rm min}$ can be estimated. Fig. 9(a) and (b) shows the impact of $V_{\rm DD}$ reduction on yield for the bulk and FD-SOI

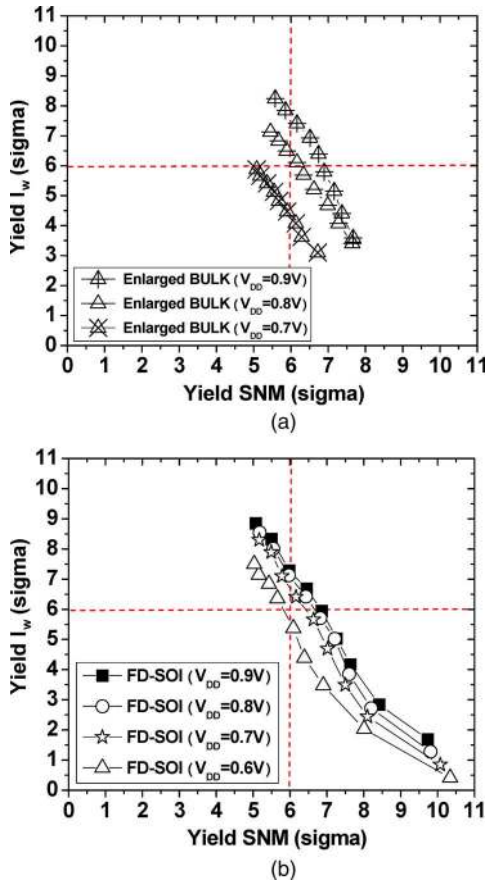


Fig. 9. Dependence of yield on $V_{\rm DD}$: (a) upsized bulk cell and (b) FD-SOI cell. At $V_{\rm DD} \sim 0.8$ V, the bulk cell cannot satisfy the 6σ requirement, in contrast to the FD-SOI cell. $V_{\rm min}$ is significantly lower, i.e., $\sim$0.6 V, for the FD-SOI cell.

TABLE IV
SUMMARY OF SRAM CELL PERFORMANCE METRICS FOR FD-SOI AND ENLARGED BULK SRAM CELLS

	FD-SOI SRAM cell		Enlarged Bulk SRAM cell	
Supply voltage	$V_{\rm min}$ (= 0.6V)	$V_{\rm DD}$ (=0.9V)	$V_{\rm min}$ (= 0.8V)	$V_{\rm DD}$ (=0.9V)
Cell area [μm^2]	0.075	0.075	0.097	0.097
SNM [mV]	123	178	182	200
I_w[μA]	8.2	22.4	17.6	21.8
$I_{\rm read}$[μA]	7.0	20.6	16.3	20.9
$W_{\rm PG}$ [nm] for maximum yield	38	40	65	65

cells, respectively. At $V_{\rm DD} \sim 0.6$ V, the FD-SOI cell can no longer meet the 6σ criterion, i.e., $V_{\rm min} \sim 0.6$ V. At $V_{\rm DD} \sim 0.8$ V, the increased-area bulk cell can no longer meet the 6σ criterion, i.e., $V_{\rm min} \sim 0.8$ V. The FD-SOI cell achieves lower $V_{\rm min}$ because it provides for higher transistor drive current and reduced variability. Table IV summarizes the performance metrics of the FD-SOI and enlarged bulk SRAM cells at $V_{\rm min}$ and nominal $V_{\rm DD}$.

V. Conclusion

Thin-BOX FD-SOI and bulk CMOSFET designs were optimized via 3-D process and device simulations for LOP CMOS technology at the 22-nm node. For the same $I_{\rm OFF}$, the FD-SOI device achieves higher drive current and reduced random $V_{\rm TH}$ variation. Using an analytical model fit to the simulated I–V characteristics for the optimized device designs, 6-T SRAM cell performance metrics (i.e., SNM, I_w, and $I_{\rm read}$) were estimated. For a fixed cell area, FD-SOI technology was found to provide for improved SNM yield (by 1.2σ) and I_w yield (by $2.2\ \sigma$). For fixed yield, the FD-SOI cell provides an area savings of $\sim$25%. The minimum operating voltage for 6σ yield ($V_{\rm min}$) is $\sim$0.6 V for the FD-SOI cell, whereas it is $>$ 0.8 V for the bulk cell. Thus, thin-BOX FD-SOI technology can facilitate the scaling of 6-T SRAM cell area and operating voltage.

Appendix

The analytical MOSFET I–V model used to estimate SRAM performance metrics in this work is

$$
\begin{aligned}
I_{\rm DS} &= \mu_s C_{\rm ox}\frac{W}{2mL}\frac{(V_{\rm GS}-V_{\rm TH})^2}{1+\frac{V_{\rm GS}-V_{\rm TH}}{E_{\rm sat}L}} \\
&\quad\times(1+\lambda V_{\rm DS})+I_{\rm sub}\left(1-e^{\frac{V_{\rm DS}}{V_{\rm TH}}}\right) \\
&\quad \text{if } V_{\rm GS}>V_{\rm TH} \qquad\qquad V_{\rm DS}\geq\tfrac{V_{\rm GS}-V_{\rm TH}}{m} \\
&= \mu_l C_{\rm ox}\frac{W}{L}\frac{V_{\rm DS}\left(V_{\rm GS}-V_{\rm TH}-\frac{mV_{\rm DS}}{V_0}\right)^2}{1+\frac{V_{\rm GS}-V_{\rm TH}}{E_{\rm sat}L}} \\
&\quad\times(1+\lambda V_{\rm DS})+I_{\rm sub}\left(1-e^{\frac{V_{\rm DS}}{V_{\rm TH}}}\right) \\
&\quad \text{if } V_{\rm GS}>V_{\rm TH} \qquad\qquad V_{\rm DS}<\tfrac{V_{\rm GS}-V_{\rm TH}}{m} \\
&= I_{\rm sub}\left(1-e^{\frac{V_{\rm DS}}{V_{\rm TH}}}\right)e^{\frac{V_{\rm GS}-V_{\rm TH}}{S}} \quad \text{if } V_{\rm GS}\leq V_{\rm TH} \qquad (1)
\end{aligned}
$$

where $C_{\rm ox}$ is the gate oxide capacitance per area, L is the gate length, W is the device width, $I_{\rm sub}$ is the current level corresponding to $V_{\rm TH}$, S is the subthreshold swing, and $V_{\rm TH}$ is the threshold voltage, which is dependent on drain bias ($V_{\rm TH}=V_{\rm T0}-{\rm DIBL}*V_{\rm DS}$). μ_l and μ_s are the carrier mobility values in the linear and saturation regimes of operation, respectively. V_0 is defined as $1/(1-\mu_s/2\mu_l)$. $E_{\rm sat}$ is the saturation electric field, which determines the amount of velocity saturation. m is a fitting parameter. As experimentally verified in [22], this model accurately captures bulk MOSFET short-channel effects and operation in the subthreshold, linear, and saturation regimes. So long as the analytical I–V model can be well fit to the simulated (or measured) I–V data for FD-SOI devices, it can accurately represent their behavior as well.

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