Performance and Off-State Current Mechanisms of Low-Temperature Processed Polysilicon Thin-Film Transistors with Liquid Phase Deposited SiO_2 Gate Insulator

Ching-Fa Yeh, Shyue-Shyh Lin, Tzung-Zu Yang, Chun-Lin Chen, and Yu-Chi Yang

***Abstract*—Polysilicon thin-film transistors (poly-Si TFT's) with liquid phase deposition (LPD) silicon dioxide (SiO_2) gate insulator were realized by low-temperature processes (< 620°C). The physical, chemical, and electrical properties of the new dielectric layer were clarified. The low-temperature processed (LTP) poly-Si TFT's with W/L = 200 μm/10 μm had an on-off current ratio of 4.95 × 10^6 at V_D = 5 V, a field effect mobility of 25.5 cm^2/V·s at V_D = 0.1 V, a threshold voltage of 6.9 V, and a subthreshold swing of 1.28 V/decade at V_D = 0.1 V. Effective passivation of defects by plasma hydrogenation can improve the characteristics of the devices. The off-state current (I_L) mechanisms of the LTP poly-Si TFT's were systematically compared and clarified. The I_L is divided into three regions; the I_L is attributable to a resistive current in region I (low gate bias), to pure thermal generation current in region II (low drain bias), and to Frenkel–Poole emission current in region III (high gate bias and drain bias).**

I. Introduction

THIN-film transistors (TFT's) on transparent substrate are important for making the active matrix of a liquid crystal display (LCD). Because polysilicon thin-film transistors (poly-Si TFT's) have a high field-effect mobility, the potential to realize very large area LCD's [1], and a capability for peripheral driver circuit integration [2]–[4], much effort has been devoted to developing high-performance poly-Si TFT's.

Using conventional glass substrate is advantageous for reducing the cost of fabricating TFT's. To realize glass substrate TFT's, the maximum process temperature must be below 600°C. Under this limitation, a high-quality low-temperature processed (LTP) polysilicon active layer and gate insulator are indispensable components for realizing high-performance low-temperature poly-Si TFT's. The solid phase crystallization (SPC) [5] method has been widely used to fabricate the polysilicon active layer, for the SPC method produces a smooth top surface and large grain size. As for the gate insulator, various chemical vapor deposition (CVD) methods have been used to fabricate the dielectric layer [6], [7]. But all of these CVD methods require expensive equipment and the processes involved are very complex. Recently, a new SiO_2 formation technology using the liquid phase deposition (LPD) method has been developed [8]. LPD SiO_2 film has two main advantages in comparison with other CVD methods: First, the substrate temperature during deposition can be greatly reduced, because LPD SiO_2 film can be deposited at room temperature. Second, the apparatus used is simple and inexpensive. LPD SiO_2 technology is thus an economical candidate for replacing high-cost CVD technologies. In this research, poly-Si TFT's with LPD SiO_2 gate insulator are first developed. The physical, chemical, and electrical properties of LPD SiO_2 and the performance of the LTP poly-Si TFT's are then described in detail.

In general, poly-Si TFT's suffer from relatively high OFF current compared with a-Si TFT's. This is a serious problem for pixel TFT's, since the fundamental principle of active matrix displays is based on static operation without leakage current. To hold the signal levels for acceptable image quality, the off-state current has to be as low as 1 pA/μm [9], which is an important criterion for poly-Si TFT's. Hence considerable effort has been devoted to clarifying the conduction mechanisms of I_L. However, as yet no consensus on the nature of the mechanisms has emerged. Some researchers have assumed that the conduction mechanism of I_L is dominated by only one of the mechanisms [10]–[12]. But recently, it has been discovered, shown that the conduction mechanism of I_L is dependent on gate bias (V_{GS}), drain bias (V_{DS}), device size, device structure, and fabrication conditions [13]–[16]. That is, the conduction mechanism is not determined by a unique mechanism. In this paper, the conduction mechanisms of I_L in poly-Si TFT's with LPD SiO_2 gate insulator will be investigated and compared with other conduction mechanisms which have been reported.

II. Experimental

A. Liquid Phase Deposition (LPD) SiO_2

A schematic diagram of the apparatus for preparing LPD SiO_2 is shown in Fig. 1. First, to prepare an immersing solution, 35 g of silica powder was added to 1 liter of hydrosilicofluoric acid (H_2SiF_6) to obtain a silica-saturated H_2SiF_6 solution. Furthermore, to supersaturate the solution

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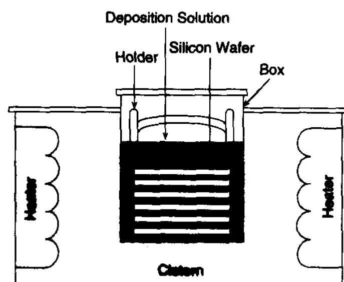
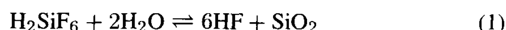


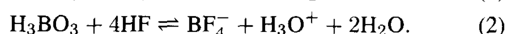
Fig. 1. Schematic diagram of the apparatus for LPD SiO_2 deposition.

with SiO_2, boric acid solution (0.1 M) was continuously added to the solution.

The basic chemical reaction kinetics of SiO_2 deposition are represented by the following two equilibrium processes:



$$H_2SiF_6 + 2H_2O \rightleftharpoons 6HF + SiO_2 \quad (1)$$



$$H_3BO_3 + 4HF \rightleftharpoons BF_4^- + H_3O^+ + 2H_2O. \quad (2)$$

In (1), addition of silica leads to a reaction shift from right to left. Therefore the solution saturated with silica will include minimum hydrofluoric acid. However, this equilibrium can be changed by adding boric acid to the solution. Normally boric acid reacts easily with hydrofluoric acid, as shown in (2), thereby consuming hydrofluoric acid and bringing about the transient state supersaturated with SiO_2 described by (1). This supersaturation of SiO_2 enhances (1) from left to right followed by silica deposition on the substrate.

To investigate the characteristics of LPD SiO_2 film, n-type, (100) silicon substrates with 4–7 Ω-cm resistivity were used in our experiment. Various SiO_2 films were deposited at different temperatures to compare the deposition rate. The SiO_2 films were characterized by measuring their thickness and the refractive index using an ellipsometer. The chemical composition was analyzed by FTIR and Auger electron spectroscopy (AES). The etching rate was examined with P-etch solution (48% HF : 70% HNO_3 : H_2O = 3 : 2 : 60) at room temperature. Electrical properties were investigated on MOS capacitors with aluminum gate contact of 0.12 mm^2 in area. The density of interface trap states was determined by high-frequency (1 MHz) capacitance-voltage (C-V) measurements [17].

B. TFT Fabrication

Fig. 2 shows a cross-sectional view of the fabricated poly-Si TFT. An under-layer of SiO_2 (500 nm thick) was thermally grown on a (100) silicon substrate. The polysilicon layer (100 nm thick) was prepared by the SPC method [5]. After the polysilicon layer was patterned into islands, SiO_2 gate insulator (100 nm thick) was deposited at 40°C by the LPD method. Then gate polysilicon (350 nm thick) was deposited by LPCVD at 620°C and patterned. P^+ (5×10^{15} cm^{-2}, 40 KeV) self-aligned implanted source and drain regions were formed by thermal annealing for 24 hours at 600°C. After the interlayer of insulator was formed, the contact holes were opened, and an aluminum layer (500 nm thick) was evaporated and patterned. Finally, hydrogenation was performed in a plasma reactor at 300°C for 60 min.

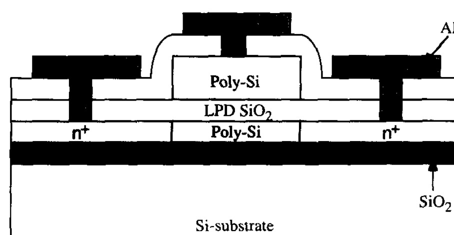


Fig. 2. Cross-sectional view of fabricated LTP poly-Si TFT with LPD SiO_2 gate insulator.

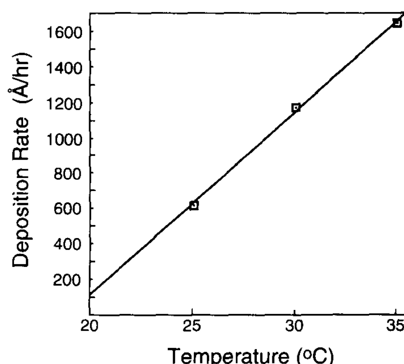


Fig. 3. Dependence of deposition rate on deposition temperature for LPD SiO_2 film.

TABLE I

	LPD-SiO_2	CVD-SiO_2
FTIR Si-O-Si Peak	1092.5 cm^{-1}	1070 cm^{-1}
Refractive Index	1.43	1.45
P-etch Rate	24 A/sec	25A/sec
Leakage Current Density (at 5V)	2.2×10^{-12} A/cm^2	9.0×10^{-12} A/cm^2
Dielectric Breakdown Field	7 MV/cm	5.8 MV/cm
Dielectric Constant (1MHz)	3.5	4.3

III. Results and Discussion

A. Characteristics of LPD SiO_2 Film

The dependence of LPD SiO_2 deposition rate on deposition temperature is shown in Fig. 3, which indicates that the SiO_2 deposition rate is enhanced with the increase in deposition temperature.

The characteristics of LPD SiO_2 film are summarized in Table I, which also compares LPD SiO_2 and CVD SiO_2 [18]. For the LPD SiO_2 film, the refractive index is about 1.42 $\sim$ 1.44, which is lower than the 1.462 of thermal SiO_2 but nearly the same as the value for CVD SiO_2. The lower refractive index may be due to a porous structure [19]. This is consistent with the results for the P-etch rate. The P-etch rate of LPD SiO_2 is about 20 Å/s. This value is larger than that for non-porous oxide (2 $\sim$ 8 Å/s) [19]. The dependence

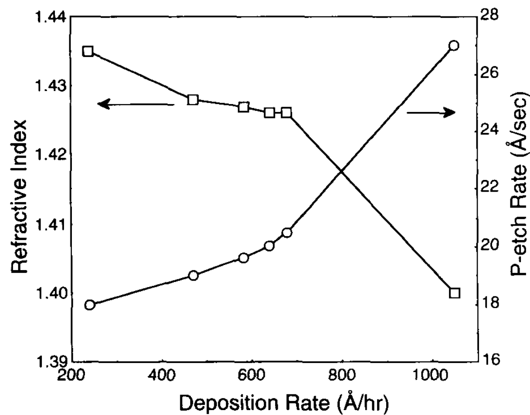


Fig. 4. Dependence of P-etch rate and refractive index on deposition rate for LPD SiO_2 film.

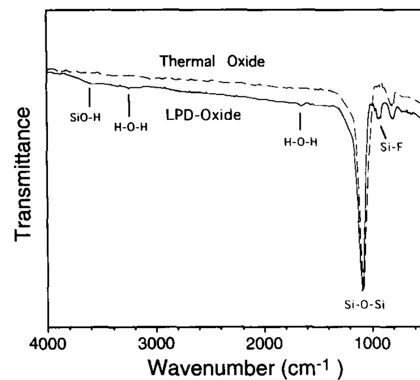


Fig. 5. FTIR spectra of LPD SiO_2 and thermal SiO_2.

of refractive index and P-etch rate on LPD SiO_2 deposition rate is shown in Fig. 4. The refractive index increases but the P-etch rate decreases with a decrease in the deposition rate. This is because the film deposited at lower deposition rate has a denser (less porous) structure, which leads to a larger refractive index and a lower P-etch rate. Thus to control the film quality, it is necessary to select an optimal deposition condition with a low deposition rate.

Typical FTIR spectra of LPD SiO_2 film are shown in Fig. 5. The absorption bands around 1090 cm^{-1} and 810 cm^{-1} are due to Si-O-Si stretching and bending vibration, respectively. These absorption bands are similar to those of thermal oxide, indicating that LPD oxide is amorphous in structure [19]. Another main absorption band around 930 cm^{-1} found in the LPD SiO_2 spectra may be attributed to Si-F stretching vibration. The fluorine (F) contained in the Si-F bond must be incorporated from the H_2SiF_6 solution. At the same time, we find that only a few absorption bands related to water appear in the LPD SiO_2 spectrum. (O-H stretching due to H_2O is shown in the absorption bands around 3300 cm^{-1} and 1640 cm^{-1}, while O-H stretching due to SiO-H is shown in the band around 3650 cm^{-1}.) These bands reveal that LPD SiO_2 film contains only little water. Because this characteristic is very important for the electrical and structural stability of the film, we conclude that the LPD SiO_2 film is of good quality.

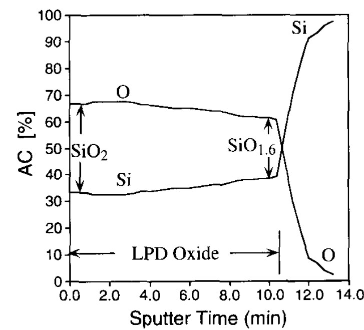


Fig. 6. AES depth profile of LPD SiO_2 film.

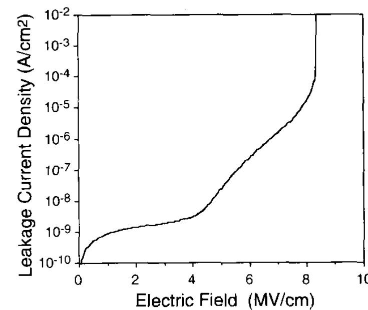


Fig. 7. Characteristics of current density versus electric field for LPD SiO_2 MOS capacitors.

The AES depth profiles of LPD SiO_2 films are shown in Fig. 6. Only silicon (Si) and oxygen (O) atoms are detected in these films. The ratio of Si/O determined by AES is about 1/2 on the surface of the LPD SiO_2 films. However, the ratio of Si/O is larger than 1/2 in the interior of the films. We conclude that LPD oxide films are Si-rich films. The Si-rich composition near the Si/SiO_2 interface thus influences the electrical characteristics of LPD SiO_2 films, as described below.

Fig. 7 is a typical current-voltage (I-V) curve of MOS capacitors with LPD SiO_2 film as dielectric. The leakage current density is about 3 nA/cm^2 at an electric-field of 4 MV/cm, and the maximum breakdown electric-field (E_{BD}) is about 7 $\sim$ 8 MV/cm. The leakage current densities of LPD SiO_2 film are slightly high. This may be due to the Si-rich composition of LPD SiO_2 film. The conduction mechanisms of LPD-oxide are similar to those reported for silicon-rich CVD SiO_2 [20]. That is, the current conduction in the Si-rich LPD SiO_2 film is likely to be due to direct tunneling from one Si-island to an adjacent one, and the characteristic hump in the I-V curve at high field probably results from Poole-Frenkel type conduction. The distribution of breakdown electric field (E_{BD}) is shown in Fig. 8; the maximum E_{BD} of the LPD SiO_2 film is 8 $\sim$ 9 MV/cm.

Fig. 9 shows the C-V curves of MOS capacitors with LPD SiO_2 film as dielectric. The C-V curves reveal the presence of many positive charges, slow states, and fast states in the LPD SiO_2 film, which are related to oxygen vacancies. In addition, injection type hysteresis is observed in the inversion region.

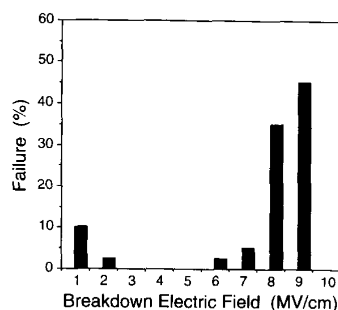


Fig. 8. Distribution of breakdown electric field (E_{BD}) for LPD SiO_2 MOS capacitors.

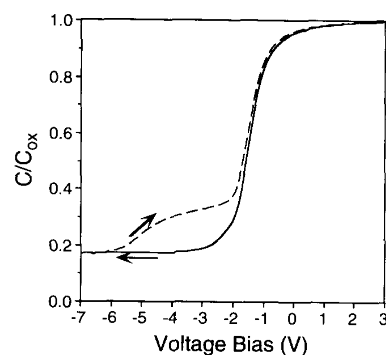


Fig. 9. Typical capacitance versus voltage characteristics for MOS capacitors with LPD SiO_2 as dielectric.

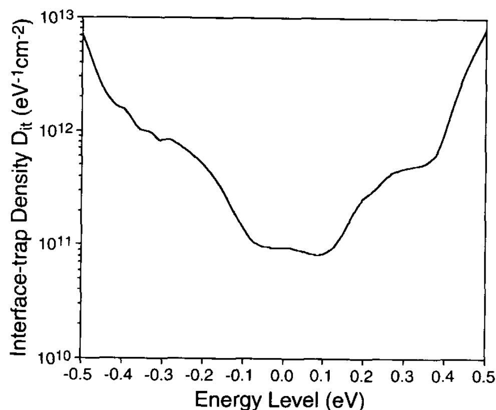


Fig. 10. A typical distribution of interface trap density for MOS capacitors with LPD SiO_2 as dielectric.

It may result from fast trapping centers near the middle-gap correlated with the Si-rich structure. The Terman method [17] was used to calculate a typical distribution of interface-trap density (D_{it}), and the result is shown in Fig. 10. It appears one order of magnitude larger than the 1×10^{10} cm^{-2} eV^{-1} of thermal SiO_2 in the mid-gap, which makes it comparable to the value for CVD SiO_2.

The experimental results on the electrical characteristics of I-V and C-V are summarized in Table I. From the table, we can conclude that LPD SiO_2 film exhibits satisfactory electrical integrity.

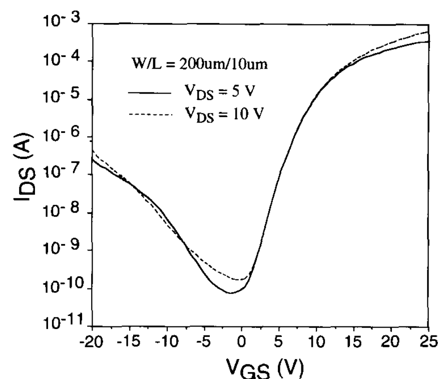


Fig. 11. Typical drain current versus gate bias characteristics for LTP poly-Si TFT's with LPD SiO_2 gate insulator.

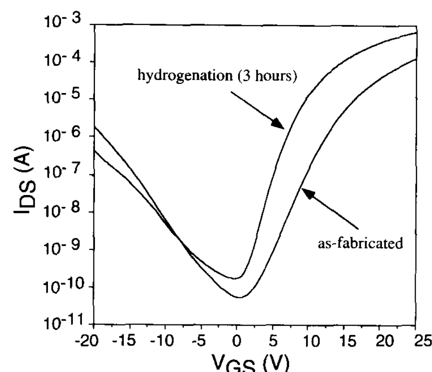


Fig. 12. Comparison of drain current versus gate bias characteristics between as-fabricated and hydrogenated poly-Si TFT's with LPD SiO_2 gate insulator.

B. Performance of LTP Poly-Si TFT's

Fig. 11 shows the drain current versus gate bias (I_D-V_G) characteristics for $W/L = 200$ μm/10 μm poly-Si TFT's with LPD SiO_2 gate insulator under constant drain voltage of 5 V and 10 V. Threshold voltage was determined from the extrapolated curve of the $\sqrt{I_D} - V_G$ characteristics in the saturated region ($V_D = 10$ V). Field-effect mobility was calculated from the maximum transconductance in the linear region ($V_D = 0.1$ V). For these LTP poly-Si TFT's, an on-off current ratio of 4.95×10^6 at $V_D = 5$V, field effect mobility of 25.5 cm^2/V·s at $V_D = 0.1$ V, threshold voltage of 6.9 V, and subthreshold swing of 1.28 V/decade were obtained.

It is well known that carrier trapping, barrier formation, and dopant segregation in the network of grain boundaries and other defects in the Si/SiO_2 interface can cause gross deviation in electronic properties from those of crystalline silicon. Hence to improve device performance, it is essential to reduce trap densities effectively. It has been shown that hydrogen plasma treatment can effectively reduce trap state density and improve device characteristics [21], [22]. A comparison of the I_D-V_G characteristics of as-fabricated and hydrogenated poly-Si TFT's with LPD SiO_2 gate insulator is shown in Fig. 12. The characteristic parameters of poly-Si TFT's obtained before and after hydrogenation are summarized in Table II. The data in

TABLE II

	As-fabricated	Hydrogenation (3 hours)
Field Effect Mobility (cm^2/V· sec)	17.9	25.5
Threshold Voltage (V)	12.9	6.91
Subthreshold Swing (V/dec)	2.11	1.28
Trap State Density (cm^{-2})	7.25×10^{12}	4.2×10^{12}

the table reveal that the field effect mobility has been improved from 17.9 cm^2/V·s to 25.5 cm^2/V·s, and the threshold voltage has been improved from 12.9 V to 6.9 V. Although the three-hour hydrogenation treatment markedly improves the electrical characteristics of poly-Si TFT's, the hydrogenation time must far exceed three hours to greatly improve the performance of poly-Si TFT's [23].

C. Off-State Current (I_L) of LTP Poly-Si TFT's

When negative gate bias (V_{GS}) is applied, a considerable OFF-state current (I_L) will be found. This current results from two basic mechanisms: 1) Resistive current, which arises when the applied V_{GS} is not negatively large enough to form a p-layer in the channel region. In this case I_L can be assumed to be an ohmic current flowing through the polysilicon bulk layer. This situation usually occurs when V_{GS} is smaller than flat band voltage (V_{FB}) but larger than the negative value of the threshold voltage ($-V_{th}$). 2) Junction leakage current, which arises when V_{GS} is more negative than $-V_{th}$. In that case, holes are induced to form a p-type channel region, and subsequently a reverse-biased p-n junction is formed between drain and channel. The junction leakage current is caused by electron-hole pairs generated via grain boundary traps in the depletion region.

There are also three other, related mechanisms through which a trapped hole at an energy level E_t can be generated to the valence band: (a) Pure thermal emission or thermal generation, which is due to thermal excitation of trapped holes in the valence band. (b) Pure field emission or tunneling, which is due to field ionization of trapped hole tunneling through the potential barrier into the valence band. (c) Thermionic field emission or Frenkel–Poole emission, which is due to field-enhanced thermal excitation of trapped holes in the valence band. The applied field causes the barrier to become low and thin enough that either thermal emission or thermal excitation to virtual states prior to tunneling can easily occur.

The pure field emission current has the strongest dependence on the applied field but is essentially independent of temperature, so it dominates at low temperature and high field conditions. The pure thermal emission current is proportional to the intrinsic carrier concentration (n_i) of silicon, and n_i is proportional to $\exp[-E_g/2k_BT]$ (where E_g is the energy gap of silicon). For this reason, the activation energy of the pure thermal emission current should be approximately equal

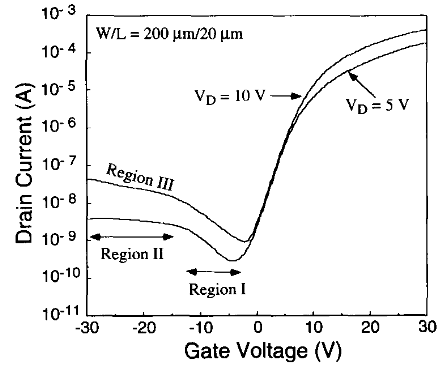


Fig. 13. Dependence of OFF-state current on gate bias with drain bias as a parameter for LTP poly-Si TFT's with LPD SiO_2 gate insulator.

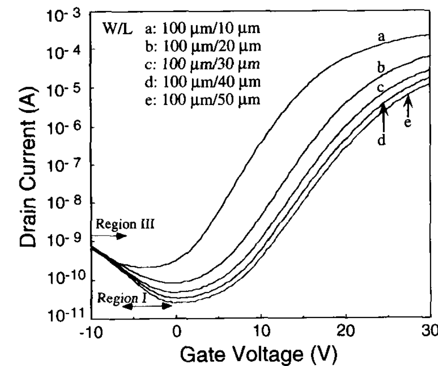


Fig. 14. Dependence of OFF-state current on gate bias at V_D = 5 V for poly-Si TFT's with channel length as a parameter.

to $E_g/2$. In addition, the pure thermal generation current is nearly independent of V_{GS}. On the other hand, both field emission and Frenkel-Poole emission current increase with V_{GS}. The difference between them is that the increase of the field emission current with $|V_{GS}|$ tends to approach a saturation value, while the Frenkel–Poole emission current does not [10]. Furthermore, the activation energy of the latter is larger than that of the former.

Fig. 13 shows the typical dependence of I_L on V_{GS} and V_{DS} for samples with W/L = 200 μm/20 μm, respectively. In order to distinguish the mechanism of the OFF-state current, the leakage current can be divided into three parts: 1) a low gate bias region I (at the region around $-10\ V < V_{GS} < 0$ V), 2) an almost flat region II, in which I_L does not change with a decrease in V_{GS}, and 3) a gate-bias dependent region III at high drain bias. Although I_L increases with negative V_{GS} both in region I and region III, the difference can be distinguished by the relationship between I_L and V_{GS} with channel length (L) as a parameter (Fig. 14). I_L in region II and region III is independent of L, while I_L in region I decreases as L increases. The dependence of I_L on $1/L$, as shown in Fig. 15, indeed indicates that I_L in region I varies linearly with $1/L$. From the above description, it is obvious that I_L in region I is a resistive current and I_L in region II and region III is a junction leakage current.

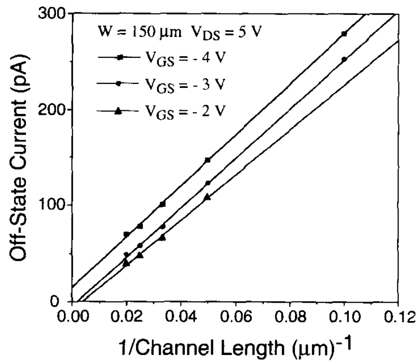


Fig. 15. Dependence of OFF-state current on the reverse of channel length at $V_D = 5$ V for poly-Si TFT's with $W = 150$ μm.

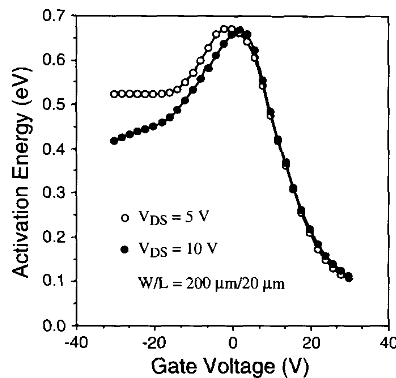


Fig. 16. Dependence of activation energy on gate bias with drain bias at 5 V and 10 V for poly-Si TFT's with LPD SiO_2 gate insulator.

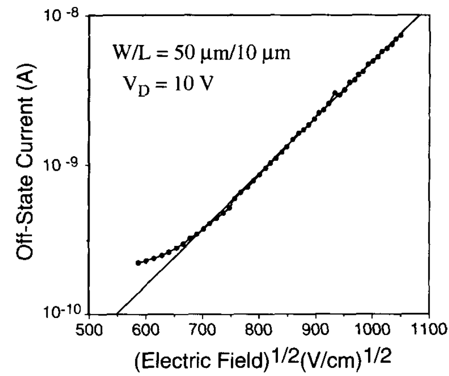


Fig. 17. Measured log I_L versus $(E_{\rm PK})^{1/2}$ at $V_D = 10$ V on a semilog scale for poly-Si TFT's with W/L = 50 μm/10 μm.

To further clarify the mechanism of I_L in region II and III, the temperature dependence was studied. The activation energies were calculated from an Arrhenius plot by means of leakage currents obtained at 25°, 50°, 75°, 100°, and 125° C. The dependence of activation energy on $V_{\rm GS}$ with $V_{\rm DS}$ at 5 V and 10 V is shown in Fig. 16. The activation energies in region II are close to the $E_g/2$ of silicon and almost independent of V_G. In contrast, an increase of negative $V_{\rm GS}$ causes a decrease of activation energy in region III. These results lead to the conclusion that I_L is attributable to pure thermal generation in region II and to Frenkel–Poole emission in region III. The width of region II is dependent on $V_{\rm DS}$. As $V_{\rm DS}$ increases, the width of region II decreases. For devices at $V_{\rm DS} = 5$ V, I_L is almost independent of $V_{\rm GS}$ up to $V_{\rm GS} = -30$ V, and it vanishes when $V_{\rm DS} = 10$ V.

Furthermore, according to [11], the Frenkel–Poole mechanism gives a current $I_{\rm FE}$ of the form

$$I_{\rm FE} = I_0 \exp(\alpha\sqrt{E_{\rm PK}}) \tag{3}$$

where

$$\alpha = \frac{(q)^{3/2}}{(\pi\varepsilon_{\rm Si})^{1/2}kT}. \tag{4}$$

I_0 is the generation current at zero electric field, and $E_{\rm PK}$ is the peak electric field given by

$$E_{\rm PK} = \frac{(V_{\rm GS} - V_{\rm DS} - V_{\rm FB})\varepsilon_{\rm SiO_2}}{t_{\rm ox}\varepsilon_{\rm Si}} \tag{5}$$

where $\varepsilon_{\rm SiO_2}$ is the permittivity of silicon dioxide and $t_{\rm ox}$ is the thickness of silicon dioxide.

Fig. 17 plots log I_L versus $(E_{\rm PK})^{1/2}$ at room temperature for our sample. A straight line fits the data reasonably well in the high electric field region. This also proves that I_L in region III is dominated by Frenkel–Poole emission.

Although the above results and discussion are all in terms of n-channel poly-Si TFT's, similar results were obtained for p-channel poly-Si TFT's. In other words, the basic conduction mechanisms of OFF-state current in p-channel poly-Si TFT's also include resistive current, thermal generation current, and Frenkel–Poole emission current. However, the weight of each mechanism is different for n-channel and p-channel TFT's.

IV. Conclusion

Polysilicon thin film transistors using liquid phase deposition silicon dioxide (SiO_2) as gate insulator were realized by low-temperature processes (< 620°C). The LPD SiO_2 method has been shown to be an economical approach that supplies a good dielectric layer. LTP poly-Si TFT's with $W/L = 200$ μm/10 μm have an on-off current ratio of 4.95 × 10^6 at $V_D = 5$ V, a field effect mobility of 25.5 cm^2/V·s at $V_D = 0.1$ V, a threshold voltage of 6.9 V, and a subthreshold swing of 1.28 V/decade at $V_D = 0.1$ V. Effective passivation of defects by plasma hydrogenation can improve the characteristics of these devices. The behavior of off-state current in LTP poly-Si TFT's has also been clarified. The conduction mechanisms of off-state currents can be divided into two parts, one attributable to a resistive current in the low gate bias region, the other to a junction leakage current in the high gate bias region. The junction leakage currents observed in our samples were due to two basic mechanisms, pure

thermal generation and Frenkel–Poole emission. Clarification of leakage current mechanisms should enable us to find fundamental principles by which to reduce the off-state current.

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