Performance Breakthrough in NOR Flash Memory with Dopant-Segregated Schottky-Barrier (DSSB) SONOS Devices

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ABSTRACT

A novel dopant segregated Schottky barrier (DSSB) SONOS device as a form of double-gate (DG) is demonstrated for NOR Flash memory applications. The DSSB also applies to all-around-gate (AAG) SONOS devices. The source side injection caused by sharp energy band bending in the DSSB device results in a high-speed programming (V_{th} shift of 4.2V @ 320ns) at a low program bias (V_{gs}/V_{ds}=7V/3V). Moreover, faster program speed in a narrower fin width (W_{fin}) due to its low parasitic resistance and enhanced gate controllability is achieved. Drain disturbance-free characteristics in a programmed cell are confirmed as well.

INTRODUCTION

The most critical limit is the gate length scaling in a NOR Flash memory cell, which uses a program method known as channel hot electron injection (CHEI). This method aggravates immunity against punchthrough by making drain voltage high enough to trigger a CHEI. In addition, the low injection efficiency of the hot electrons generated at the drain side and the high parasitic resistance at the source and drain (S/D) also impose a constraint on scaling the cell size down. Consequently, the lower effective program voltage due to the high parasitic S/D resistance in an extremely scaled cell results in a small V_{th} window and thereafter retards the program speed.

Our previous works focused only on a NAND Flash memory cell that utilized the DG DSSB SONOS structure [1]. It improved the programming speed as well as the short-channel effects through lower program bias.

In this work, an intensive analysis of NOR Flash memory, where a similar DG and highly scaled AAG DSSB SONOS devices are employed, is carried out for the first time. It boosts the program speed even at a low program bias owing to the improved CHEI, which is enabled by the inherent sharp band bending of the DSSB at the source side. The DSSB structure provides several benefits, including increased lateral and vertical field, excellent injection efficiency into the charge storage node, and a drain disturbance-free feature against a conventional device composed of a p-n junction, as shown in **Fig. 1**.

DEVICE FABRICATION

The process flow of the DG DSSB FinFET SONOS device is identical to that in our previous work [1] apart from a revamped nickel-silicide junction that uses a three-step RTP for precise control of the junction profile. In contrast, sacrificial oxidation, release, and gate trimming are newly added, and a gate spacer formation was omitted in the AAG DSSB SONOS device. SEM and TEM photographs of DG and AAG DSSB SONOS devices are shown at **Fig. 2** and **Fig. 9**, respectively. They ensure high immunity to short-channel and punchthrough in scaled NOR Flash memory.

RESULTS AND DISCUSSIONS

Fig. 3 shows the program and erase characteristics of NOR Flash for various program conditions. In the case of a conventional p-n junction device, the program efficiency is not as high as that of DSSB due to the lowered effective program voltage that arises from the high parasitic resistance and relatively poor injection efficiency. Conventional NOR Flash memory therefore requires the drain bias to be as high as possible for a large V_{th} window and a high program speed. This creates numerous challenges. However, in the case of the DG DSSB SONOS device, a fast program speed and a large V_{th} shift are attained even with a low V_{ds}. This is attributed to the inherently sharp energy band of the DSSB structure that leads to an increase in both the vertical and lateral electric field at the source side, as explained in **Fig. 1**. However, the erase characteristics do not differ much from those in conventional NOR Flash because the mechanism of electron de-trapping is identical in the two devices.

To identify the location of the trapped electrons, the shift of V_{th} is carefully measured by changing the read V_{ds} in both the forward and reverse read state: i.e., the source and drain electrodes are interchanged, as shown in **Fig. 4**. Both the shifts of V_{th} and I_{off} at the reverse read state are larger compared to those at the forward state. The shift of V_{th} originates from localized electron trapping at the source side. The shift of I_{off} is also understood in terms of the narrowed tunneling width caused by the electrons that are trapped at the drain (i.e., the trapped region in the reverse read state). It is therefore concluded that electrons are captured at the source side in the DSSB structure.

The drain disturbance of a programmed cell with a relatively high program bias (V_{ds} =5V) was also characterized, as shown in **Fig. 5**. Significantly improved immunity against drain disturbances is achieved in the DSSB NOR Flash device, as expected. This is primarily caused by the trapped electrons located at the source side; they inhibit hot holes from being injected into the trapped regions.

Fig. 6 shows the program transient characteristics of the DG DSSB and a conventional device with various W_{fin}. In the conventional device, high parasitic resistance cannot be avoided as the device is scaled down. This high parasitic resistance can result in reducing the effective program bias ($V_{gs,\,eff}$ and $V_{ds,eff}$), thus suppressing the amount of hot electrons that are generated [2, 3]. As a result, the program speed slows as W_{fin} is narrowed in the conventional device. The DSSB device has, however, low parasitic resistance due to the metal silicided S/D, which is one of the advantages of a SB-device. Additionally, it should be noted that the injection efficiency from the source electrode to the channel is enhanced due to the increased gate controllability as W_{fin} is decreased. This is a very important and attractive aspect for extremely scaled devices such as nanowire devices. **Fig. 7** displays the series resistance and potential profile depending on W_{fin}. At a fin width of 30nm, the parasitic resistance of the DSSB device is three times lower compared to that of a conventional device. Moreover, high injection efficiency with a narrowed W_{fin} can be attained due to a thinner tunneling width of the DSSB device.

In terms of reliability, the post cycling retention characteristics are presented in **Fig. 8**. A large V_{th} window and distinctive multiple states after 10 years are attractive for MLC in NOR Flash memory [4].

For ultimately scaled NOR Flash memory, DSSB technology is applied to an AAG device, as shown in **Fig. 9**. A boost in the program speed via the aforementioned DSSB features is attained with a reduced V_{ds} compared to a conventional AAG SONOS device in **Fig. 10**.

CONCLUSIONS

A DG DSSB SONOS device for NOR Flash memory is demonstrated in this work. A high speed, low program voltage, and drain disturbance-free feature were achieved due to a source side injection of electrons. A highly scaled AAG DSSB SONOS device was also successfully demonstrated and applied to NOR Flash memory.

REFERENCES

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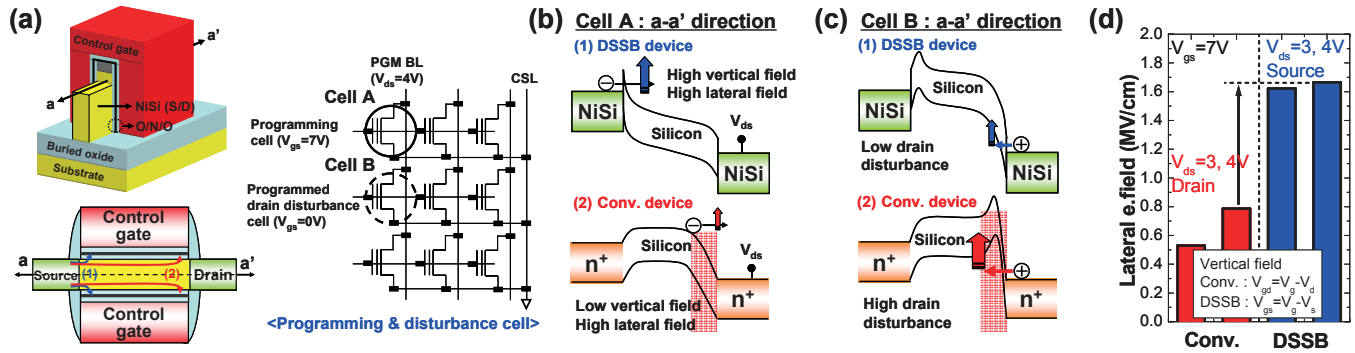

Fig. 1: Description of the NOR Flash memory programming operation in a DSSB SONOS device. (a) Schematic of DSSB SONOS device and the NOR Flash memory cell architecture. (b) Cell A (program cell): In the case of the DSSB device, electrons are captured at the source side rather than the drain side due to the high lateral and vertical electric field caused by sharp band bending at the source side. (c) Cell B (drain disturbance cell): In the case of a conventional device, trapped electrons at the drain side can increase the potential for hot holes to be generated, which results in a drain disturbance. However, the DSSB device shows drain disturbance-free characteristics due to the trapped electrons at the source side. (d) Numerically simulated data of the electric field in both two devices are shown. Even with a low program V_{ds}, high lateral and vertical electric field at the source side are generated in the DSSB device.

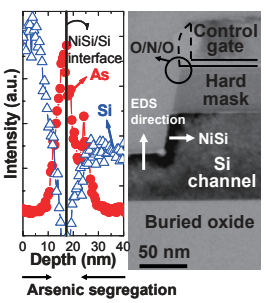

Fig. 2: STEM EDS analysis and TEM image of DG DSSB SONOS (a-a' direction of **Fig. 1(a)**

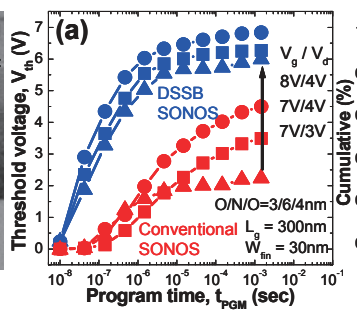

Fig. 3: Program/erase characteristics for DG DSSB and DG conventional SONOS devices: (a) Program transient characteristics. (b) Cumulative plot of programmed states for both devices. (c) Erase transient characteristics.

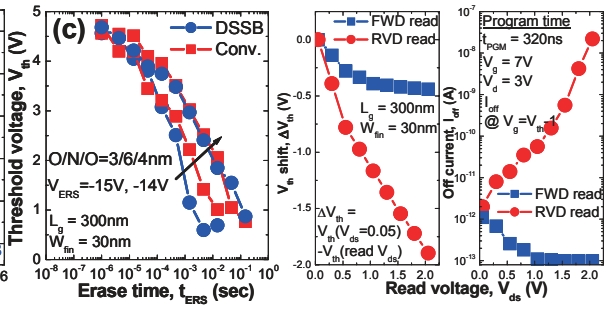

Fig. 4: Verification of source side injection of electrons: Locally trapped electrons at the source side can change V_{th} and I_{off} for the reverse read state.

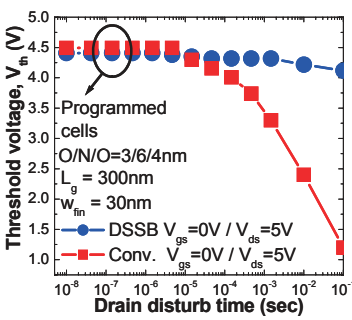

Fig. 5: Drain disturbance of DG DSSB and DG conventional devices: Compared to the conventional device, high immunity to drain disturbance is achieved in the DG DSSB device.

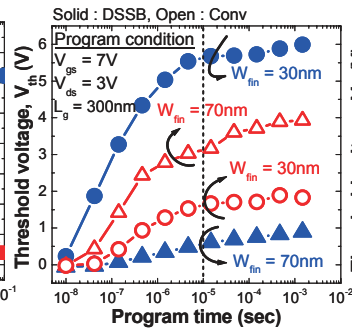

Fig. 6: Program transient characteristics by W_{fin} dependency: As the W_{fin} decreases, high injection efficiency of the electrons from the source electrode to the channel can be attained. This enhances the program speed in the DG DSSB device. However, high parasitic resistance in a conventional device with a narrow W_{fin} can limit fast operation of the device.

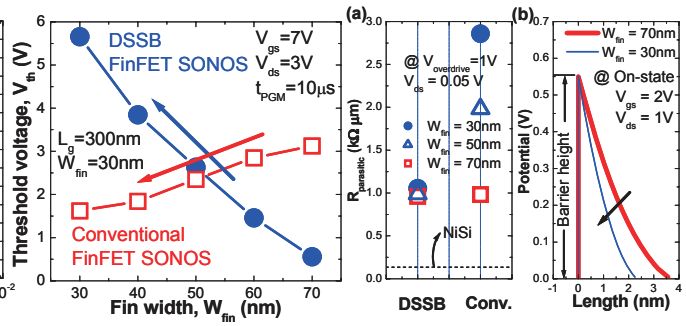

Fig. 7: (a) Measured data of parasitic resistance in DG DSSB and DG conventional devices: (b) Simulated potential of the DG DSSB device along the gate length direction for different W_{fin}

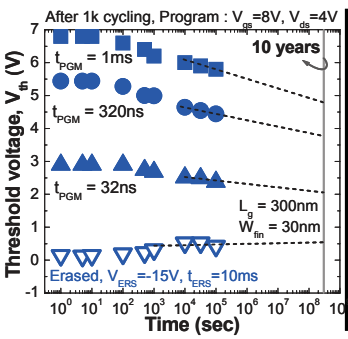

Fig. 8: Retention characteristics of a DG DSSB device for MLC in NOR Flash memory operation

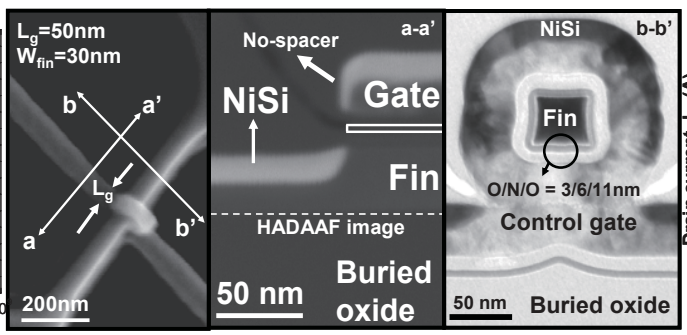

Fig. 9: Fabricated AAG DSSB SONOS device: No spacer process with a three-step RTP for NiSi was used. The gate length and fin width are 50nm and 30nm, respectively.

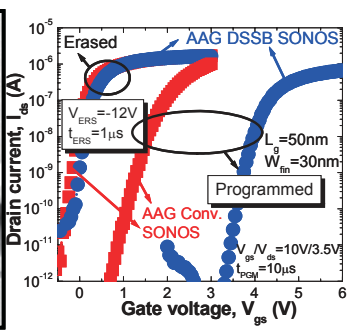

Fig. 10: Measured transfer curve of both the AAG conventional and DSSB devices for program/erase states