Università di Pisa

Performance Comparison of Graphene Nanoribbon FETs With Schottky Contacts and Doped Reservoir

Youngki Yoon
Department of Electrical and Computer Engineering, University of Florida
Gianluca Fiori
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Seokmin Hong
Department of Electrical and Computer Engineering, University of Florida
Giuseppe Iannaccone
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa
Jing Guo
Department of Electrical and Computer Engineering, University of Florida

Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, J. Guo, *Performance Comparison of Graphene Nanoribbon FETs With Schottky Contacts and Doped Reservoirs*, IEEE Transactions on Electron Devices, **55**, 9, pp.2314-2323 (2008)

Performance Comparison of Graphene Nanoribbon FETs With Schottky Contacts and Doped Reservoirs

Youngki Yoon, *Student Member, IEEE*, Gianluca Fiori, Seokmin Hong, Giuseppe Iannaccone, *Member, IEEE*, and Jing Guo, *Member, IEEE*

***Abstract*—We present an atomistic 3-D simulation study of the performance of graphene-nanoribbon (GNR) Schottky-barrier field-effect transistors (SBFETs) and transistors with doped reservoirs (MOSFETs) by means of the self-consistent solution of the Poisson and Schrödinger equations within the nonequilibrium Green's function (NEGF) formalism. Ideal MOSFETs show slightly better electrical performance for both digital and terahertz applications. The impact of nonidealities on device performance has been investigated, taking into account the presence of single vacancy, edge roughness, and ionized impurities along the channel. In general, MOSFETs show more robust characteristics than SBFETs. Edge roughness and single-vacancy defect largely affect the performance of both device types.**

***Index Terms*—Defect, device simulation, graphene field-effect transistor, graphene nanoribbon, impurity, nonequilibrium Green's function (NEGF), quantum transport.**

I. Introduction

In THE last decade, carbon nanostructures have attracted much attention from the device research community because its electrical properties make it very appealing for electronic applications. Carbon nanotubes were demonstrated, for the first time, by Iijima [1], and from there, huge effort has been directed to understand the physical properties of the new material and to exploit its potentials in electronic applications to come after Moore's law and ITRS requirements [2]–[4]. Carbon atoms can not only be combined in the form of tubes of nanoscale dimensions but can also be arranged in a stable 2-D graphene sheet [5]–[7]. Electrons in graphene behave as massless fermions and travel through the lattice with long mean free path, as shown by the high mobility [5]–[7]. Graphene is a zero-gap material, with linear dispersion in correspondence of the Fermi energy, which makes it particularly unsuitable for transistor applications. However, energy gap can be induced by means of lateral confinement [8], which is realized, for example, by etching the graphene sheet in narrow stripes, so-called graphene nanoribbons (GNRs).

Theoretical works have shown that GNRs have energy gap which is inversely proportional to their width [9], [10], and due to their reduced dimensions, edge states play an important role, defining non-null energy gap, for all ribbon widths [11], [12]. GNR field-effect transistors (GNRFETs) have been fabricated very recently [13]–[15]. GNRFETs that are demonstrated experimentally to date are realized by connecting the channel to metals with Schottky contacts [8], [14], therefore obtaining a Schottky-barrier FET (SBFET). In addition, ohmic contacts can, in principle, be obtained by heavily doping the GNR source and drain extensions, which makes device operation MOSFET-like (therefore, it is referred to as a MOSFET in the subsequent discussion). Because fabrication techniques are at the very first steps, simulations can represent an important tool to evaluate device performance. Semiclassical top-of-the-barrier simulations have been performed [16], [17], whereas quantum simulations based on a tight-binding approach have followed [18]–[21] in order to assess device potential. However, due to the embryonic stage of this new field of research, many issues still remain unsolved. It is, for example, not clear how much performance improvement can be obtained by using a MOSFET device structure, as compared to the Schottky-contact counterpart, as well as the extent to which nonidealities can affect device characteristics. State-of-the-art etching techniques are, for instance, far from atomistic resolution, so that edge roughness can play an important role on device performance [22]–[24]. In addition, defects or ionized impurities can represent elastic scattering centers, which can greatly degrade the expected fully ballistic behavior.

In this paper, GNR SBFET and MOSFET are numerically studied in order to establish their potential and the performance that can be expected if technological challenges are met. The approach is based on the self-consistent solution of the 3-D Poisson and Schrödinger equations within the nonequilibrium Green's function (NEGF) formalism [25], by means of a real-space p_z tight-binding Hamiltonian, in which energy relaxation at the GNR edges is considered. Different types of nonidealities have been investigated. In particular, we have studied the effect of a single-vacancy defect, an ionized impurity in the channel, and edge roughness on the device performance. Doped source and drain reservoir devices show better performance as

Manuscript received March 24, 2008. The works of Y. Yoon, S. Hong and J. Guo were supported in part by the Semiconductor Research Corporation and the Office of Naval Research N000140810861. The works of G. Fiori and G. Iannaccone were supported in part by the EC Seventh Framework Program under project GRAND (Contract 215752), by the Network of Excellence NANOSIL (Contract 216171), and by the European Science Foundation EUROCORES Program Fundamentals of Nanoelectronics, through funds from CNR and the EC Sixth Framework Program, under project DEWINT (Contract ERAS-CT-2003-980409). The review of this paper was arranged by Editor M. Reed.

Y. Yoon and J. Guo are with the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611 USA (e-mail: ykyoon@ufl.edu).

G. Fiori and G. Iannaccone are with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, 56122 Pisa, Italy (e-mail: g.fiori@iet.unipi.it).

S. Hong was with University of Florida. He is now with Purdue University, West Lafayette, IN 47907 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2008.928021

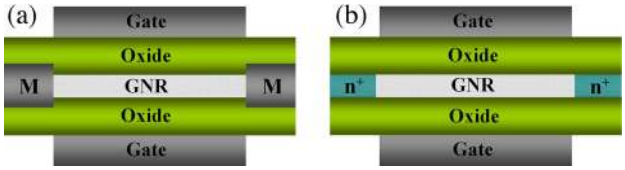


Fig. 1. Simulated device structure. (a) SBFET with metal contacts. (b) MOSFET with doped source and drain extensions. The SiO_2 gate insulator is 1.5 nm thick with a relative dielectric constant $\kappa = 3.9$. $N = 12$ A-GNR is used as a channel material, which is 15 nm long and 1.35 nm wide, and the bandgap is $E_g \approx 0.6$ eV. The SB height in (a) is a half band gap.

compared to Schottky GNRFETs. Vacancies and edge roughness can greatly affect device electrical performance more than ionized impurities actually do.

II. Approach

Device characteristics of GNRFETs are calculated by solving the Schrödinger equation using the NEGF formalism [25] self-consistently with the 3-D Poisson equation [18]–[21]. A tight-binding Hamiltonian with an atomistic p_z orbital basis set is used to describe atomistic details of the GNR channel. Coherent transport is assumed. Simulated device structures are shown in Fig. 1. The source and the drain are doped extensions of GNRs in MOSFETs, and metals in SBFETs with SB height of $\Phi_{\rm Bn} = \Phi_{\rm Bp} = E_g/2$. Double-gate geometry is used through 1.5-nm SiO_2 gate oxide ($\kappa = 3.9$). For an ideal device simulation, perfectly patterned 15-nm-long $N = 12$ [9] armchair-edge GNR (A-GNR) is used as a channel material, which has a width of $\sim$1.35 nm and a bandgap of $\sim$0.6 eV. Edge bond relaxation is treated according to *ab initio* calculation, and a tight-binding parameter of $t_0 = 2.7$ eV is used [11]. Power supply voltage is $V_{\rm DD} = 0.5$ V. Room-temperature ($T = 300$ K) operation is assumed.

Nonidealities are treated as follows. Lattice vacancies or edge roughness are considered as atomistic defects of the channel GNR, where the existence of carriers is essentially prohibited. These atomistic vacancies or edge roughness can be implemented by breaking the nearest bonds ($t_0 = 0$) in the device channel Hamiltonian matrix of the perfect lattice according to the geometry of the defective lattice. For simplicity, it is assumed that the topological structure of GNR is not affected by the defect, which may provide a perturbation to the quantitative results, but the qualitative conclusions of this paper will not be changed. An ionized impurity is treated as an external fixed charge, which can play an important role for the electrostatic potential of the device. In other words, in the self-consistent iterative loop between the transport equation and the Poisson equation, the input charge into the Poisson equation always includes a fixed external charge as well as the output charge from the Schrödinger equation.

III. Results

A. Ideal Structures

We first present results for an SBFET and a MOSFET under ideal conditions. Fig. 2(a) and (b) shows the transfer characteristics for each device. SBFET shows the typical ambipolar behavior [Fig. 2(a)], so that, for a fair comparison, a common off current $I_{\rm off} = 10^{-7}$ A is selected and that the ON state is defined at $V_{\rm on} = V_{\rm off} + V_{\rm DD}$. Then, the operating voltage ranges are shown by the gray windows in Fig. 2(a) and (b) for each device. Through the gate work-function tuning, $V_{\rm off}$ can be shifted to $V_G = 0$ V ($V_D = V_{\rm DD}$), and the transfer characteristics after the work-function engineering are shown in Fig. 2(c): The MOSFET has 50% larger $I_{\rm on}$ (i.e., current for $V_G = V_{\rm DD}$ and $V_D = V_{\rm DD}$) and larger transconductance g_m than the SBFET. This observation agrees to a conclusion in a previous literature that the on current of a ballistic SBFET with positive SB height is smaller than that of a ballistic MOSFET due to the tunneling barrier at the source end of the channel [26]. MOSFETs can have, in addition, a significantly larger maximum on–off ratio than SBFETs due to the absence of ambipolar transport, as shown in Fig. 2(d).

Fig. 3(a) shows the output characteristics for $V_G = 0.5$ V: MOSFET shows a better saturation behavior. This is confirmed by the output conductance g_d defined as the derivative of the output characteristic with respect to V_D. As can be seen in Fig. 3(b), g_d in MOSFET is almost half the value found for SBFET.

We now focus on switching and high-frequency performances of GNR devices. In Fig. 4(a), the cutoff frequency f_T as a function of the applied gate voltage is shown and computed by using the quasi-static approximation [27] as

$$f_T = \left.\frac{g_m}{2\pi C_G}\right|_{V_D = V_{\rm DD}} \tag{1}$$

where g_m is the transconductance and C_G is the gate capacitance computed as the derivative of the charge in the channel with respect to the gate voltage. As can be seen, MOSFET has $\sim$30% higher f_T as compared to the SBFET counterpart. For what concerns the intrinsic switching time τ instead, which represents the typical figure of merit for digital applications, we have used a previously developed comparison method that takes into account the power supply, ON, and OFF states [28]. This quantity is typically used to estimate the time it takes an inverter to switch, when its output drives another inverter. Fig. 4(b) shows the intrinsic delay as a function of on–off ratio: In this case, MOSFET exhibits $\sim$20% faster switching speed than a middle-bandgap SBFET. The very high cutoff frequency and the very small delay shown in Fig. 4 are due to the extremely short channel length (15 nm) and the assumption of purely ballistic transport. In general, f_T is inversely proportional to the channel length, and for longer channel SBFETs, for example, it can be expressed as $f_T \approx 73$ GHz/($L_{\rm ch}$ in micrometers) at the ON state. In addition, additional parasitic capacitance could largely affect the estimated f_T and delay.

B. Atomistic Vacancy

We now focus our attention on the effect of a single-vacancy defect on device performance. Fig. 5(a) and (b) shows the transfer characteristics for SBFET and MOSFET, both in the linear and the logarithmic scale, for different positions of a defect. All defects are placed in the middle of the channel along the width direction, whereas three different positions along the

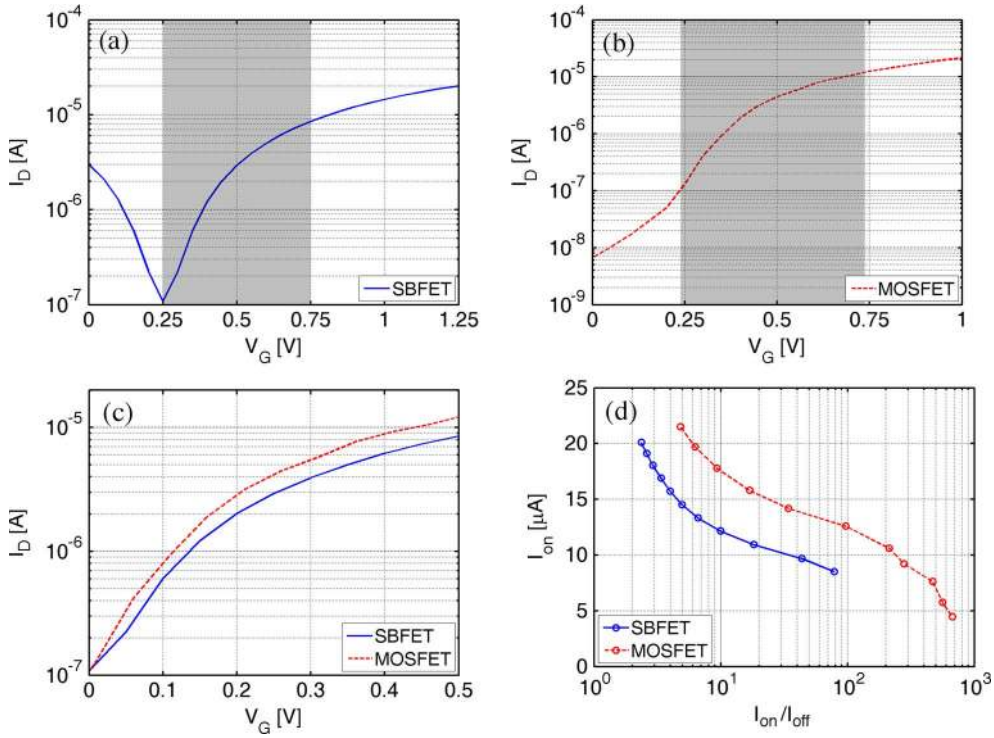


Fig. 2. $I_D - V_G$ characteristics of (a) an ideal SBFET and (b) an ideal MOSFET. For a fair comparison between two different devices, the minimal leakage current $I_{\min}$ of SBFET is chosen as a common off current $I_{\text{off}} = 10^{-7}$ A, and ON state is defined at $V_{\text{on}} = V_{\text{off}} + V_{\text{DD}}$, where $V_{\text{DD}} = 0.5$ V is the power supply voltage. The gray windows in (a) and (b) show the operating voltage ranges of each device. (c) Transfer characteristics of the ideal devices after gate work-function engineering, by which V_{off} can be shifted to $V_G = 0$ V. An ideal MOSFET has 50% larger I_{on} than an ideal SBFET. (d) I_{on} versus $I_{\text{on}}/I_{\text{off}}$. MOSFETs can have a significantly larger on–off ratio than SBFETs.

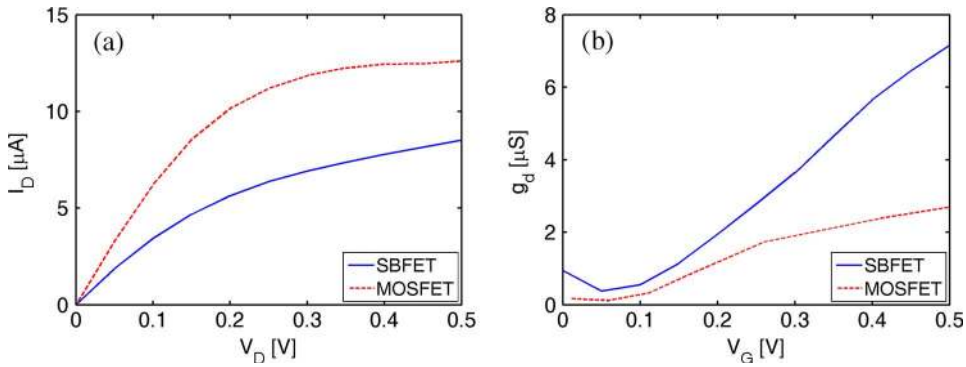


Fig. 3. (a) $I_D - V_D$ characteristics at $V_G = V_{\text{DD}} = 0.5$ V. (b) Output conductance g_d versus V_G for $V_D = V_{\text{DD}}$. MOSFET shows better saturation behavior, which can also be pointed out by smaller g_d.

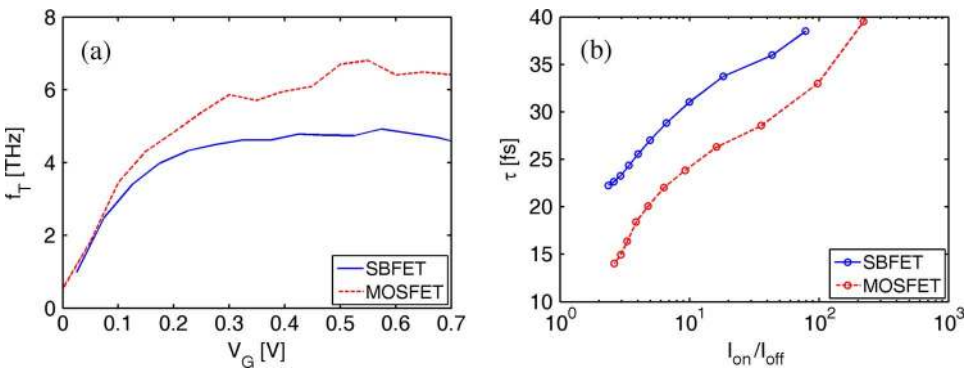


Fig. 4. (a) Cutoff frequency f_T versus V_G. (b) Intrinsic delay τ versus $I_{\text{on}}/I_{\text{off}}$. MOSFETs can have higher cutoff frequency and smaller intrinsic delay than SBFETs.

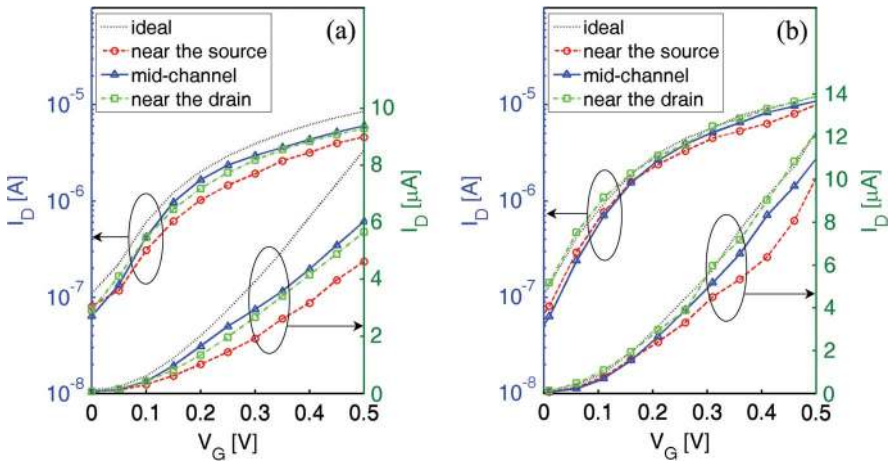


Fig. 5. Effect of a lattice vacancy along the transport direction. $I_D - V_G$ of (a) SBFETs and (b) MOSFETs in the presence of a single lattice vacancy, in (left axis) a log scale and in (right axis) a linear scale. The lattice vacancy is placed in the middle of the channel width direction and at the different positions along the transport direction: near the source, in the middle of the channel, and near the drain.

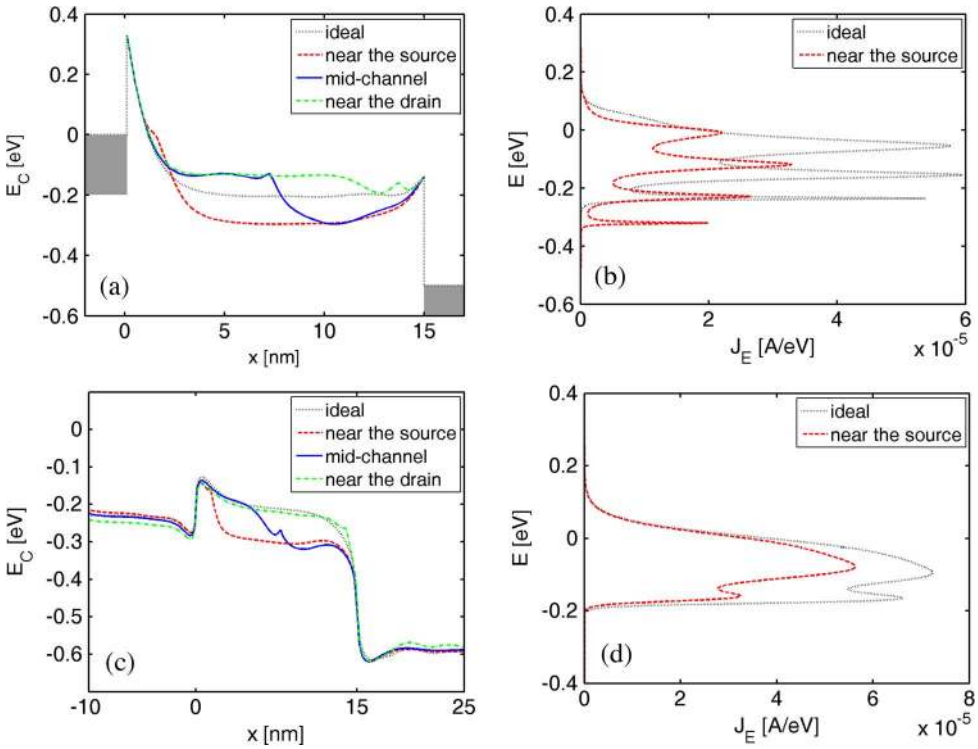


Fig. 6. Conduction band profile along the channel position for (a) SBFETs and (c) MOSFETs in the presence of a lattice vacancy at the ON state. Energy-resolved current spectrum for (b) the SBFET and (d) the MOSFET in the presence of a vacancy near the source.

propagation direction are considered: In particular, the defect has been placed near the source, in the middle of the channel, and near the drain.

As shown in Fig. 5, the defect near the source has the largest effect in both devices. As compared to the ideal device, the defect results in 46% and 17% smaller $I_{\rm on}$ in SBFET and MOSFET, respectively. This is because the carrier transport in the device is totally controlled by the SB at the source end for SBFETs and by the top of the barrier, which is also located near the source, for MOSFETs.

The details of the $I_{\rm on}$ reduction can be explained by the reduced quantum transmission and self-consistent electrostatic effect. For an SBFET with a defect near the source, thicker SB is induced [Fig. 6(a)] due to the electron accumulation, and quantum transmission is reduced [Fig. 6(b)] at the ON state, which result in a smaller $I_{\rm on}$. When a defect is located at halfway along the channel or near the drain of an SBFET, the accumulated electrons lift up the potential barrier and reduce the energy window of electron injection from the source to the channel, which results in reduced current with a lattice vacancy. In case of a MOSFET with a lattice vacancy near the source, the self-consistent potential barrier is not increased, as shown in Fig. 6(c). Instead, the reduced number of propagating states due to the lattice vacancy reduces the transmission probability [Fig. 6(d)], which results in a smaller on current. On the other hand, defects near the drain and in the middle of the channel do

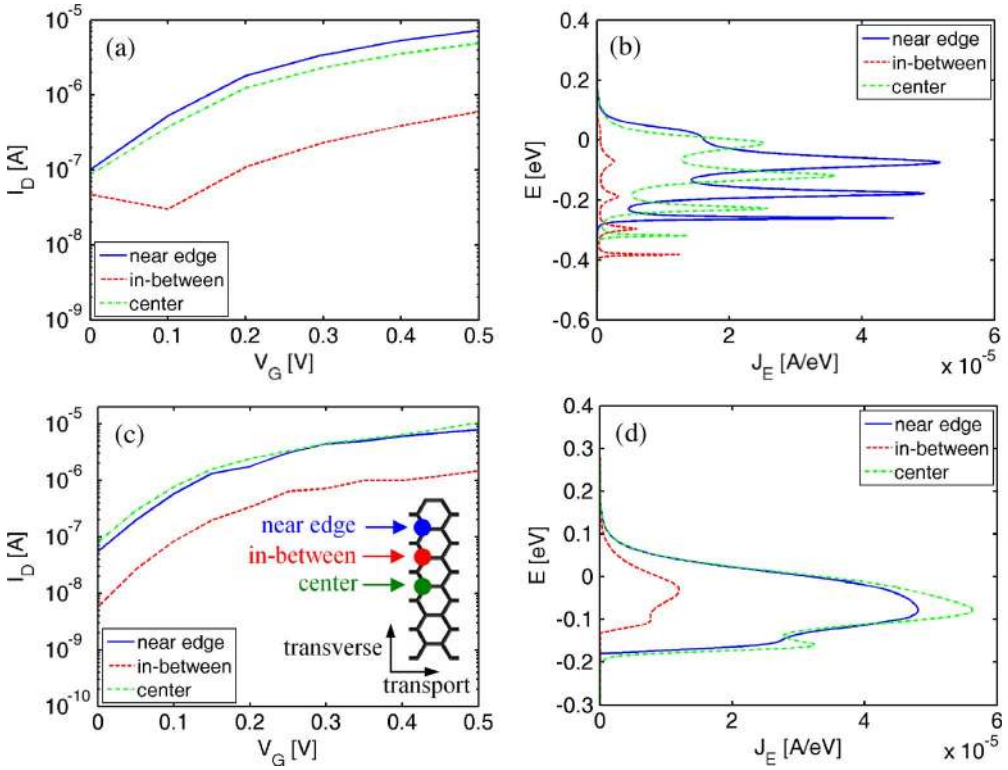


Fig. 7. Effect of a lattice vacancy along the channel width direction. I_D-V_G of (a) SBFETs and (c) MOSFETs in the presence of a single lattice vacancy. The vacancy is located at different positions along the width direction: (solid line) near edge, (dash–dot line) at center, and (dashed line) between the two, as shown in the inset of (c). The position of the defect along the transport direction is close to the source. Energy-resolved current spectrum for (b) SBFETs and (d) MOSFETs.

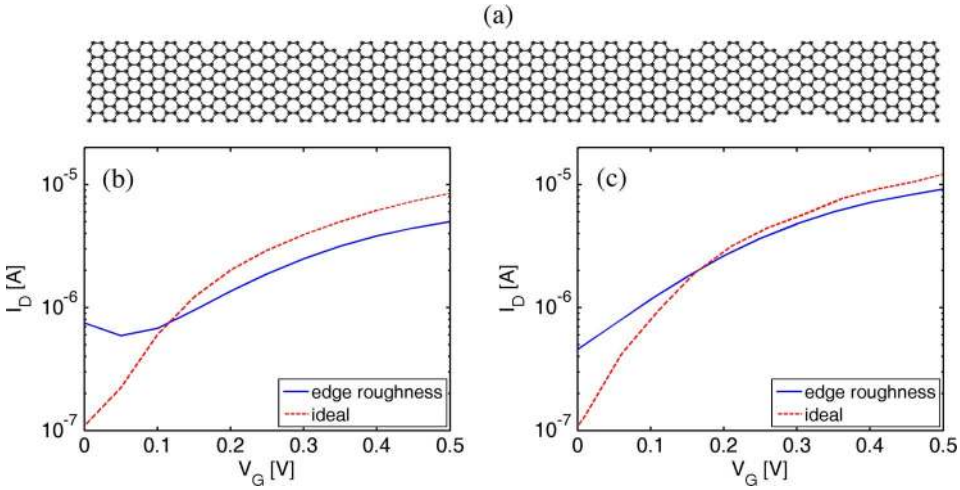


Fig. 8. Effect of edge roughness. (a) Atomistic configuration of a simulated GNR channel in the presence of edge roughness. I_D-V_G characteristics of (b) the SBFET and (c) the MOSFET with the GNR channel shown in (a).

not affect device transfer characteristics as much as the case near the source. Transport is, indeed, mostly determined by the top-of-the-barrier potential, which, as shown in Fig. 6(c), is only partially influenced by the presence of the defect in correspondence of the drain (and in the middle of the channel).

Next we show that the transfer characteristic is also very sensitive to the position along the channel width direction. The position of a defect varies from the center to the near edge, as shown in the inset of Fig. 7(c). For both devices, it has the largest effect on the $I_{\rm on}$ when it is located at the position marked in-between. Because $N = 12$ A-GNR has the largest effective coupling strength at that position [29], the device has severely reduced transmission [Fig. 7(b) and (d)] and, hence, the smallest on current [Fig. 7(a) and (c)]. In comparison, it only has small effects when the defect is at the center or near the edge due to the relatively small effective coupling strength.

C. Edge Roughness

State-of-the-art patterning technique is far from atomic-scale precision, and edge roughness of GNR is always expected in the fabrication process. Therefore, it would be very useful to

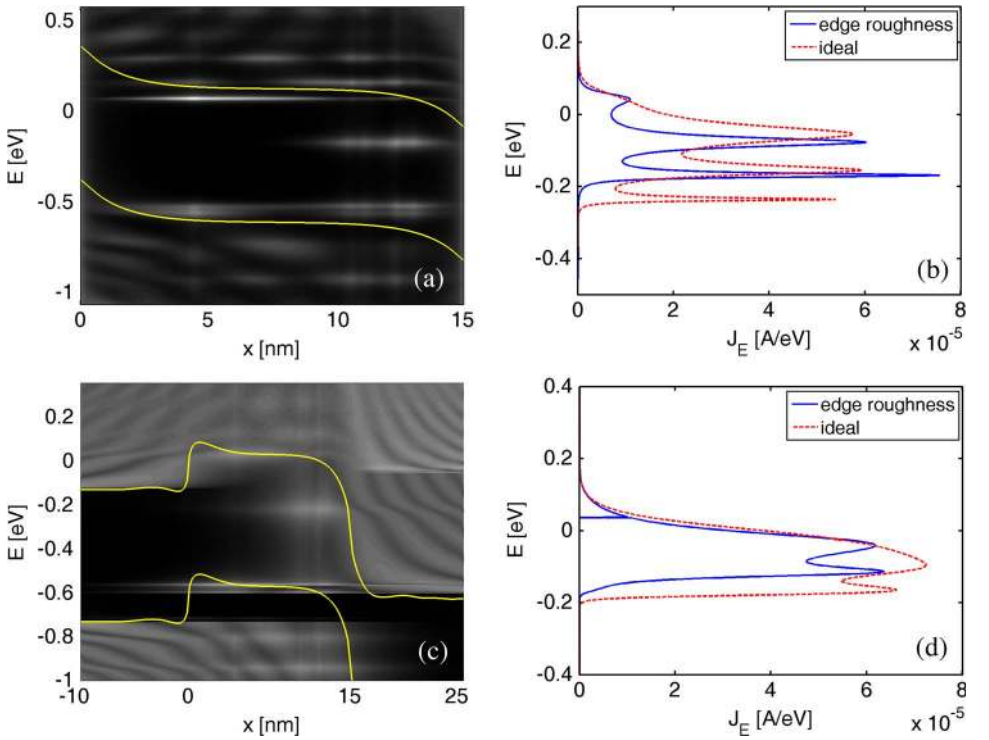


Fig. 9. LDOS at the OFF state ($V_G = 0$ V and $V_D = V_{DD}$) for (a) the SBFET and (c) the MOSFET with the GNR channel of Fig. 8(a). Energy-resolved current spectrum at the ON state ($V_G = V_D = V_{DD}$) for (b) the SBFET and (d) the MOSFET. The solid lines in (a) and (c) show the band profiles of ideal transistors.

examine the effect of edge roughness on device performance. One of the simplest irregular-edge GNRs is shown in Fig. 8(a), which is obtained by removing carbon atoms from both edges in the same probability. In general, the off currents are increased due to the gap states induced in the band-gap region, which enhances the leakage current at the OFF state [22]. Fig. 9(a) and (c) clearly shows the local density of states (LDOS) in the band-gap region for an SBFET and a MOSFET, respectively, at the OFF state. On the other hand, the on currents are generally decreased due to the reduced quantum transport [22]. Even though the gap states near the beginning of the channel may facilitate quantum transport, the overall quantum transmission is reduced by the carrier transport through the imperfect-edge GNR, as shown in Fig. 9(b) and (d). For the structure of Fig. 8(a), $I_{\rm off}$ is increased by factors of seven and four, and $I_{\rm on}$ is reduced by 40% and 20% for an SBFET and a MOSFET, respectively.

In order to investigate the general behavior of GNRFETs with edge roughness, randomly generated 100 samples are simulated. Fig. 10 is a histogram of $I_{\rm on}$ for SBFETs in the presence of edge roughness, where carbon atoms are randomly added into or removed from the edges of GNR with probability $P = 0.05$. The result shows that $I_{\rm on}$ is generally decreased by edge roughness, and the mean value is 25% smaller than the ideal one. In addition, the performance variation can be very large from device to device, which is caused by the different atomistic details of each irregular-edge GNR.

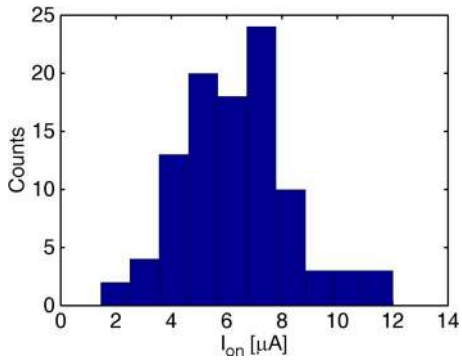


Fig. 10. Histogram of $I_{\rm on}$ for SBFETs in the presence of edge roughness of GNR by adding or removing carbon atoms with probability $P = 0.05$. One-hundred samples are randomly generated and simulated. The mean is 6.36 μA, the median is 6.31 μA, and the standard deviation is 2 μA.

D. Ionized Impurity

The last nonideality is an ionized impurity, which can exist near the GNR channel. In this paper, Li ion is used as impurity, which has a positive 0.4q at 1.84 Å away from the GNR surface according to *ab initio* calculations [30]. It is located in the middle of the GNR width at different positions along the transport direction. Fig. 11 shows $I_D - V_G$ curves in the presence of an ionized impurity. For SBFETs, it has the largest effect with 20% larger $I_{\rm on}$ when located near the source because of the severely reduced SB at the source end [Fig. 12(a)], which is a key factor to determine the carrier transport in tunneling devices. If an impurity is located far from the source, the alteration of SB is significantly reduced, and it only has a small effect on the $I_{\rm on}$. On the other hand, an ionized impurity always has a relatively small effect on the $I_{\rm on}$ of MOSFETs because it has a very limited influence over the barrier height. Regardless of the impurity position, the on current of MOSFET varies by less than 10% [Fig. 11(b)].

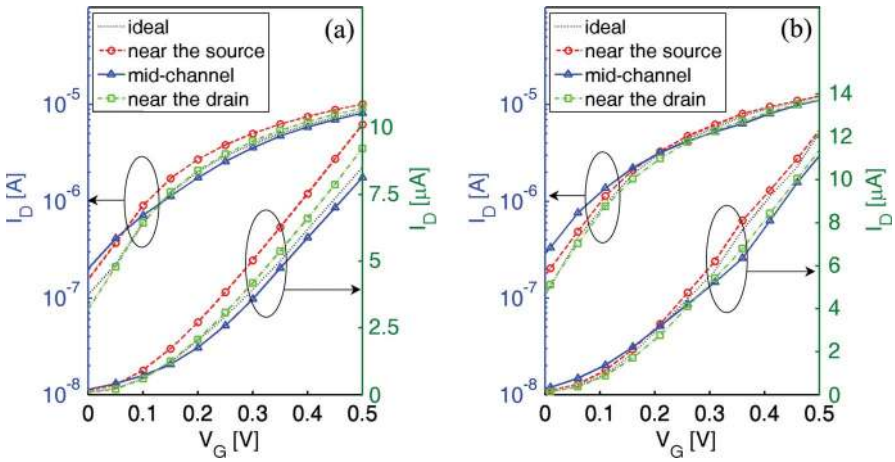


Fig. 11. Effect of a positive ionized impurity. $I_D - V_G$ of (a) SBFETs and (b) MOSFETs in the presence of an ionized impurity, in (left axis) a log scale and in (right axis) a linear scale. The impurity is located in the middle of the GNR width direction and at the different positions along the transport direction. Li ion is used as impurity, which has +0.4q at 1.84 Å away from the GNR surface.

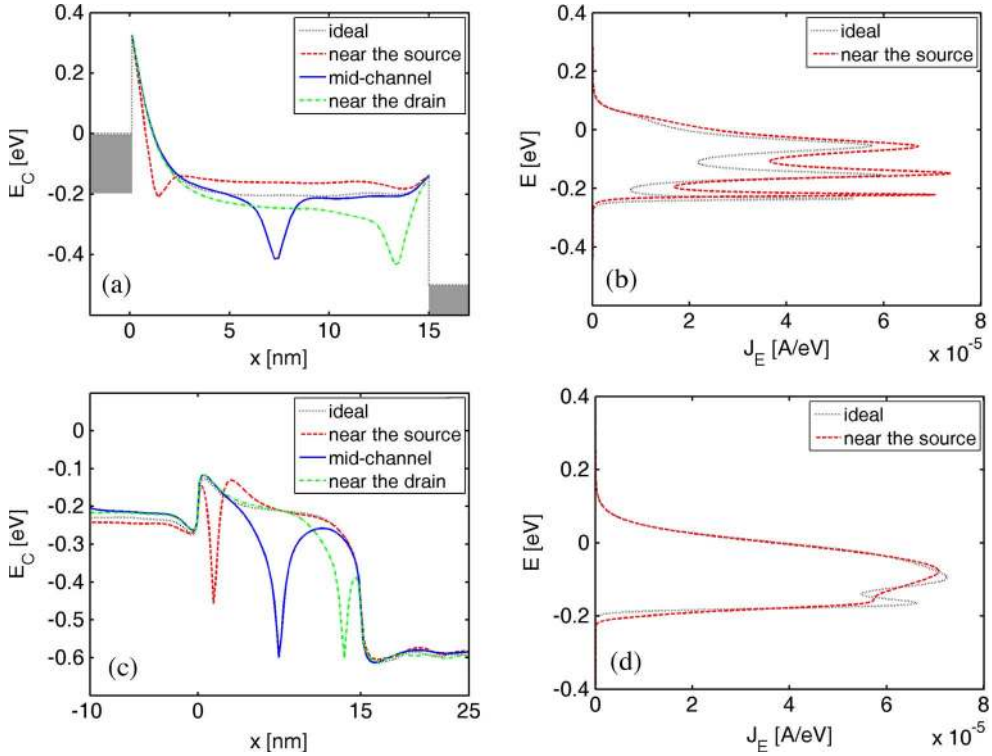


Fig. 12. Conduction band profile along the channel position for (a) SBFETs and (c) MOSFETs in the presence of a positive ionized impurity at the ON state. Energy-resolved current spectrum for (b) the SBFET and (d) the MOSFET in the presence of a positive ionized impurity near the source.

Next, we simulated 100 cases at randomly distributed positions maintaining the distance between Li ion and GNR surface to explore its general effect on the $I_{\rm on}$. Fig. 13(a) is a histogram of $I_{\rm on}$ for SBFETs in the presence of a positive ionized impurity, which shows two distinct groups. The first group has increased $I_{\rm on}$ due to the severely reduced SB when an ionized impurity is very close to source $(0 < x < 4$ nm$)$ or drain electrodes $(13 < x < 15$ nm$)$. Thirty-four percent of the samples are counted in this group. On the other hand, the $I_{\rm on}$ of the second group is reduced, when an impurity is not located near the source or the drain, due to the quantum–mechanical reflection of nonuniform electrostatic potential. For what concerns MOSFET instead, the largest number of samples lays around the ideal value (12.5 μA), whereas the remaining samples differ by less than 8%. Such insensitiveness is due to the fact that, for the considered simulations, the top of the barrier is well below the Fermi level of the source: Local changes of the potential do not influence the overall source-to-drain current.

So far, we focused on a positive ionized impurity near the GNR surface. In order to investigate the effect by a negative-charge impurity, an external impurity of an electron is placed at 0.5 nm away from the GNR surface. The electron is located in the middle of the GNR width at different positions along

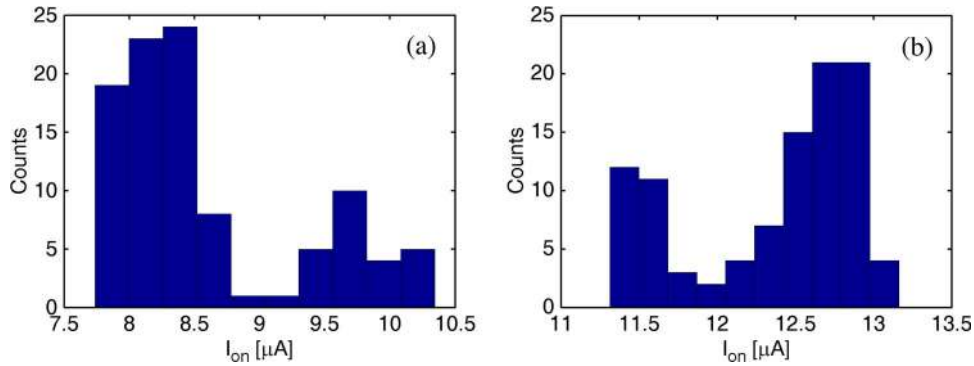


Fig. 13. Histogram of $I_{\rm on}$ for (a) SBFETs and (b) MOSFETs in the presence of an ionized impurity with $+0.4$q at 1.84 Å away from the GNR surface.

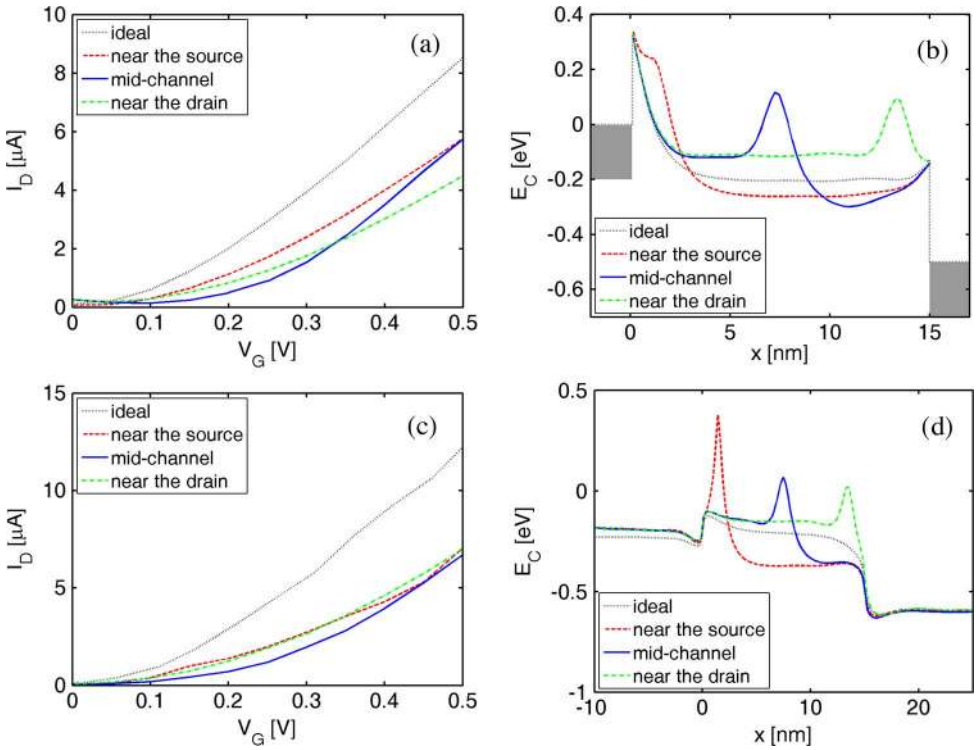


Fig. 14. Effect of a negative-charge impurity. $I_D - V_G$ characteristics of (a) SBFETs and (c) MOSFETs in the presence of a charge impurity with $-$q at 0.5 nm away from the GNR surface. Conduction band profiles along the transport position at the ON state for (b) SBFETs and (d) MOSFETs.

the transport direction. An electron impurity increases the self-consistent electrostatic potential, which is common for both SBFETs and MOSFETs, as shown in Fig. 14(b) and (d). Therefore, the on current is decreased by 33%–47% in the presence of electron impurity. Even though MOSFETs are nearly invariant to a positive ionized impurity, they are very susceptible to a negative-charge impurity.

IV. Conclusion

In this paper, GNR SBFETs and MOSFETs are compared by solving the Schrödinger equation self-consistently with the 3-D Poisson equation. In ideal devices, MOSFETs show better device characteristics over SBFETs: larger maximum achievable on–off ratio, 50% larger on current, larger transconductance, and better saturation behavior with 60% smaller output conductance. Switching and high-frequency performances of GNR devices are also better in MOSFETs, which have 30% higher cutoff frequency and 20% faster switching speed.

Even under the influence of a defect or an impurity, MOSFETs are more robust than SBFETs. In the presence of a single lattice vacancy, the $I_{\rm on}$ of SBFET can be reduced by 46%, which is much larger than that of MOSFET, due to the severely affected SB thickness of the tunneling device. Edge roughness of GNR can, in general, result in larger off current and smaller on current, and the variability of device performance is very large because of the totally different atomistic configuration of GNR in such small channel devices. In the presence of a positive ionized impurity, the $I_{\rm on}$ of SBFET can be increased by 20%, but its effect on MOSFET is very limited because the top of the barrier is nearly invariant to the positive impurity. However, a negative-charge impurity always disturbs the carrier transport of GNRFETs due to the locally increased electrostatic potential.

ACKNOWLEDGMENT

Y. Yoon and G. Fiori equally contributed in this paper.

REFERENCES

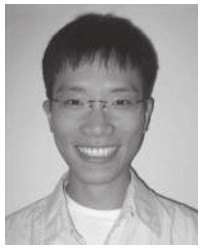
[1] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, no. 6348, pp. 56–58, Nov. 1991.
[2] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, Aug. 2003.
[3] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon nanotube electronics," *Proc. IEEE*, vol. 91, no. 11, pp. 1772–1784, Nov. 2003.
[4] *International Technology Roadmap for Semiconductors*. [Online]. Available: http://public.itrs.net
[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.
[6] Y. B. Zhang, Y. W. Tan, H. L. Stormer, and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," *Nature*, vol. 438, no. 7065, pp. 201–204, Nov. 2005.
[7] C. Berger, Z. M. Song, T. B. Li, X. B. Li, A. Y. Ogbazghi, R. Feng, Z. T. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics," *J. Phys. Chem., B*, vol. 108, no. 52, pp. 19 912–19 916, 2004.
[8] M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, no. 20, p. 206 805, May 2007.
[9] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Phys. Rev. B, Condens. Matter*, vol. 54, no. 24, pp. 17 954–17 961, Dec. 1996.
[10] V. Barone, O. Hod, and G. E. Scuseria, "Electronic structure and stability of semiconducting graphene nanoribbons," *Nano Lett.*, vol. 6, no. 12, pp. 2748–2754, Dec. 2006.
[11] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, no. 21, p. 216 803, Nov. 2006.
[12] C. T. White, J. W. Li, D. Gunlycke, and J. W. Mintmire, "Hidden one-electron interactions in carbon nanotubes revealed in graphene nanostrips," *Nano Lett.*, vol. 7, no. 3, pp. 825–830, 2007.
[13] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.
[14] Z. H. Chen, Y. M. Lin, M. J. Rooks, and P. Avouris, "Graphene nanoribbon electronics," *Physica, E, Low-Dimens. Syst. Nanostruct.*, vol. 40, no. 2, pp. 228–232, Dec. 2007.
[15] X. L. Li, X. R. Wang, L. Zhang, S. W. Lee, and H. J. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, Feb. 2008.
[16] Y. Ouyang, Y. Yoon, J. K. Fodor, and J. Guo, "Comparison of performance limits for carbon nanoribbon and carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 89, no. 20, p. 203 107, Nov. 2006.
[17] G. C. Liang, N. Neophytou, D. E. Nikonov, and M. S. Lundstrom, "Performance projections for ballistic graphene nanoribbon field-effect transistors," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 677–682, Apr. 2007.
[18] G. Fiori and G. Iannaccone, "Simulation of graphene nanoribbon field-effect transistors," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 760–762, Aug. 2007.
[19] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2223–2231, Sep. 2007.
[20] G. C. Liang, N. Neophytou, M. S. Lundstrom, and D. E. Nikonov, "Ballistic graphene nanoribbon metal–oxide–semiconductor field-effect transistors: A full real-space quantum transport simulation," *J. Appl. Phys.*, vol. 102, no. 5, p. 054 307, Sep. 2007.
[21] X. Guan, M. Zhang, Q. Liu, and Z. Yu, "Simulation investigation of double-gate CNR-MOSFETs with a fully self-consistent NEGF and TB method," in *IEDM Tech. Dig.*, 2007, pp. 761–764.
[22] Y. Yoon and J. Guo, "Effect of edge roughness in graphene nanoribbon transistors," *Appl. Phys. Lett.*, vol. 91, no. 7, p. 073 103, Aug. 2007.
[23] D. Basu, M. J. Gilbert, L. F. Register, S. K. Banerjee, and A. H. MacDonald, "Effect of edge roughness on electronic transport in graphene nanoribbon channel metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 92, no. 4, p. 042 114, Jan. 2008.
[24] E. R. Mucciolo, A. H. Castro Neto, and C. H. Lewenkopf, "Conductance quantization and transport gap in disordered graphene nanoribbons," cond-mat/0806.3777.
[25] S. Datta, "Nanoscale device modeling: The Green's function method," *Superlattices Microstruct.*, vol. 28, no. 4, pp. 253–278, Oct. 2000.
[26] J. Guo and M. S. Lundstrom, "A computational study of thin-body, double-gate, Schottky barrier MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 1897–1902, Nov. 2002.
[27] P. J. Burke, "AC performance of nanoelectronics: Towards a ballistic THz nanotube transistor," *Solid State Electron.*, vol. 48, no. 10/11, pp. 1981–1986, Oct./Nov. 2004.
[28] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in *IEDM Tech. Dig.*, San Francisco, CA, 2004, pp. 703–706.
[29] S. Hong, Y. Yoon, and J. Guo, "Metal-semiconductor junction of graphene nanoribbons," *Appl. Phys. Lett.*, vol. 92, no. 8, p. 083 107, Feb. 2008.
[30] K. Rytkonen, J. Akola, and M. Manninen, "Density functional study of alkali-metal atoms and monolayers on graphite (0001)," *Phys. Rev. B, Condens. Matter*, vol. 75, no. 7, p. 075 401, Feb. 2007.

Youngki Yoon (S'08) received the B.E. degree in material science and engineering from Korea University, Seoul, Korea, in 1999, and the M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, in 2005. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Florida.

He is currently with the Computational Nanotechnology Group, University of Florida. His research interests include simulation and modeling of nanoscale devices such as carbon nanotubes, graphene, nanowire, and organic electronics.

Gianluca Fiori received the degree in electrical engineering and the Ph.D. degree from the Università di Pisa, Pisa, Italy, in 2001 and 2005, respectively.

In autumn 2002, he was with Silvaco International, developing quantum models, which are currently implemented in the commercial simulator ATLAS by Silvaco. In summer 2004 and 2005, he was with Purdue University, West Lafayette, IN, working on models for the simulation of transport in nanoscaled devices. Since December 2007, he has been an Assistant Professor with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa. His main field of activity includes the development of models and codes for the simulations of ultrascaled semiconductor devices.



Seokmin Hong received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2003, and the M.S. degree in electrical engineering and computer science from the University of Florida, Gainesville, in 2007. He is currently working toward the Ph.D. degree at Purdue University, West Lafayette, IN.

His research interests include the physics, modeling, and simulation of nanodevices.

Giuseppe Iannaccone (M'98) received the M.S.E.E. and Ph.D. degrees in electrical engineering from the Università di Pisa, Pisa, Italy, in 1992 and 1996, respectively.

In 1996, he was a Researcher with the Italian National Research Council, and in the same year, he was a Faculty Member with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, first as an Assistant Professor and then, since January 2001, as an Associate Professor of electronics. He has authored and coauthored more than 110 papers published in peer-reviewed journals and more than 70 papers in proceedings of international conferences. His interests include transport and noise in nanoelectronic and mesoscopic devices, development of device modeling and TCAD tools, and the design of extremely low power circuits and systems for RFID and ambient intelligence scenarios.

Dr. Iannaccone has coordinated a few European and national projects involving multiple partners and has acted as a Principal Investigator in several research projects funded by public agencies at European and national levels and by private organizations. He is a member of the technical committee of few international conferences and serves as a Referee for the leading journals in the fields of condensed matter physics, device electronics, and circuit design.

Jing Guo (S'02–M'04) received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 2004.

He is currently an Assistant Professor in electrical engineering with the Department of Electrical and Computer Engineering, University of Florida, Gainesville. He has also worked on the simulation of silicon nanotransistors and single-electron devices. He is the Coauthor of the book entitled *Nanoscale Transistors*: *Device Physics*, *Modeling*, *and Simulation* (Springer, 2006). His current research work centers on electronic and optoelectronic devices based on graphene, carbon nanotubes, nanowires, and organic semiconductors, device physics of nanotransistors, and quantum transport in devices.

Dr. Guo is a member of the technical program committees of the International Electron Devices Meeting and the Device Research Conference.