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Performance Evaluation of Si/SiC Hybrid Switch-Based Three-Level Active Neutral-Point-Clamped Inverter

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Abstract In this paper, two types of Silicon (Si) IGBT and Silicon Carbide (SiC) hybrid switch (Si/SiC HyS) based three-level active neutral-point-clamped (3L-ANPC) inverter are proposed for high efficiency and low device cost. The proposed Si/SiC HyS-based 3L-ANPC inverters are compared with the full Si IGBT, full SiC MOSFET, and Si with SiC devices-based hybrid 3L-ANPC solutions on the inverter efficiency, power capacity, and device cost. It is shown that compared with the full Si IGBT 3L-ANPC solution, the inverter efficiency improvement by Si/SiC HyS is 2.4% and 1.8% at light load condition and heavy load condition, respectively. Compared to the full SiC MOSFET solution and 2-SiC MOSFET hybrid scheme, the device cost of 2-Si/SiC HyS-based 3L-ANPC is reduced by 78% and 50% with 0.28% and 0.21% maximum inverter efficiency sacrifices. The testing results show that the proposed Si/SiC HyS-based 3L-ANPC inverter is a cost-effective way to realize high inverter efficiency. Between the two proposed Si/SiC HyS-based 3L-ANPC inverters, the 2-Si/SiC HyS-based 3L-ANPC inverter has lower device cost which makes it more suitable for cost-sensitive and high efficiency applications. While the 4-Si/SiC HyS-based 3L-ANPC inverter has higher output power capacity, making it a better candidate for high power density, high power capacity, and high efficiency applications.

***Index Terms*—Silicon carbide, hybrid switch, three-level, active neutral-point-clamped, efficiency.**

I. INTRODUCTION

POWER inverters have been widely used in electrical vehicles (EV), photovoltaic (PV), and traction systems which play an important role in converting dc-ac powers [1] - [5]. Multilevel inverters have been a good choice for high-voltage and high-power applications. Among the multilevel inverter topologies, three-level (3L) topology is one of the most widely used solutions. Compared to the two-level (2L) inverters, the 3L inverters can operate under higher voltage and have better output power quality [6], [7]. In addition to the benefits on itself, from a system level, the positive impacts on the passive components make the 3L inverters a competitive alternative to the 2L inverters even in low-voltage applications [8].

The three-level neutral-point-clamped (3L-NPC) topology is a well-established solution for the high-voltage and high-power inverters. Among those NPC topologies, the diode clamped NPC topology has been widely used in different applications. But it suffers from the uneven loss distribution and the resulting unsymmetrical semiconductor junction temperature distribution in the topology, limiting the inverter's switching frequency and power output capacity [9] - [11]. To resolve this problem, the three-level active neutral-point-clamped (3L-ANPC) topology, depicted in Fig. 1, is derived. The clamping diodes of the diode clamped NPC topology are replaced by two active switches to obtain more midpoint clamping paths. Thus, more degrees of freedom are provided to design the inverter commutation characteristics and adjust the power loss distribution [12] - [15]. In literature [12] and [13], an adjustable loss distribution (ALD) strategy which combines the loss distribution mechanism of two PWM strategies is proposed

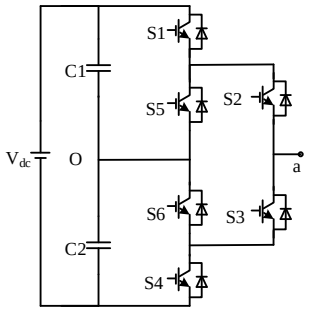

Fig. 1. One-leg 3L-ANPC topology.

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to distribute the high frequency switching losses between the inner and outer switches. The ALD strategy improved the thermal balance of the 3L-ANPC inverter, but Si IGBTs still generate all the switching losses. and the inverter efficiency is not improved.

To achieve better inverter performance on the inverter efficiency, power density, and output power quality, SiC MOSFETs are utilized in the power inverters [16] - [18]. For the 3L-ANPC structure, each inverter leg consists of 6 active switches. A full SiC MOSFET-based 3L-ANPC inverter will greatly increase the device cost. In order to utilize the SiC benefits in 3L-ANPC structure, Si IGBT and SiC MOSFET (Si&SiC) hybrid 3L-ANPC topologies have been proposed [19], [20], and [21]. A cost-effective Si&SiC hybrid scheme for 3L-ANPC, shown in Fig. 2 (a), is proposed in [19]. Only two active switches in each leg are replaced by SiC MOSFETs for the high frequency switching. The inverter efficiency is significantly improved by reducing the switching losses. In [20], a scalable ANPC converter configuration that utilizes the SiC MOSFETs as the high frequency switches and Si IGBTs as the low frequency devices was proposed. The cost for the ANPC legs is reduced and the efficiency is increased compared to the Si solution. In literature [21], 2-SiC MOSFETs and 4-SiC MOSFETs Si&SiC hybrid 3L-ANPC, depicted in Fig. 2 (a) and (b) respectively, are proposed. The inverter efficiency, device cost, and thermal performance of the two Si&SiC hybrid schemes are analyzed and compared experimentally. The device cost has been reduced by the proposed Si&SiC hybrid schemes, but compared to the full Si IGBT solution, the device cost for large current-rated SiC MOSFETs is still relatively high, especially for the 4-SiC hybrid scheme.

The Si IGBT and SiC MOSFET hybrid switch (Si/SiC HyS) consisting of a high current-rated Si IGBT and a low current-rated SiC MOSFET is shown in Fig. 3. Compared with a full current-rated SiC MOSFET, only a small current-rated SiC MOSFET is needed to form the Si/SiC HyS, thereby reducing the device cost compared to a full current-rated SiC MOSFET. Si/SiC HyS has been widely discussed and investigated due to its superior performance on low device cost, low semiconductor loss, and overload capability. The Si/SiC HyS combines the Si IGBT's advantages of low conduction loss, low device cost and SiC MOSFET's advantage of low switching loss [22] - [28]. Different gate driving pattern designs have been reported in [22], [23], [26], [28]. Si IGBT zero-voltage switching (ZVS) is achieved by applying the gate driving sequence of SiC MOSFET turn-on first and turn-off last. This gate driving pattern enables the Si/SiC HyS to operate at high switching frequencies. In addition to those loss and cost benefits brought by the Si/SiC HyS, the parallel structure of the Si/SiC HyS provides its fault-tolerant operation capability. The fault-tolerant inverter operation algorithm for the Si/SiC HyS-based inverter is proposed in [29]. The algorithm was validated on a two-level single-phase Si/SiC HyS-based inverter prototype. The experimental results demonstrated that fault-tolerant control algorithm could prevent the damage of Si IGBT or SiC MOSFET due to overheating in faulty conditions. Some literature also studied the thermal balance issue within the hybrid switch caused by the turn-on, turn-off delay time, and the dynamic current sharing process. In paper [30], a junction temperature balance method was proposed to achieve larger power handling capability and reliable operation of the Si/SiC HyS. It is reported that through the active gate delay time control, the device junction temperatures can be regulated and balanced by redistributing the switching losses and part of the conduction losses. Double pulse test results also presented the trade-off between the device loss and device junction temperature balancing. In paper [31], the Si/SiC HyS was utilized in the 3L-ANPC inverters as the high frequency switching devices S2 and S3 to achieve high efficiency and low device cost. But other types of Si/SiC HyS-based 3L-ANPC topologies, such as four high-frequency switching devices 3L-ANPC inverter are not evaluated. To further investigate the feasibility and performance of Si/SiC HyS-based 3L-ANPC inverter, two types of Si/SiC HyS-based 3L-ANPC hybrid schemes are proposed to realize a high inverter efficiency and further reduce the device cost. Moreover, the inverter performance including device cost, inverter efficiency, and thermal performance is analyzed and compared through simulation and experiment.

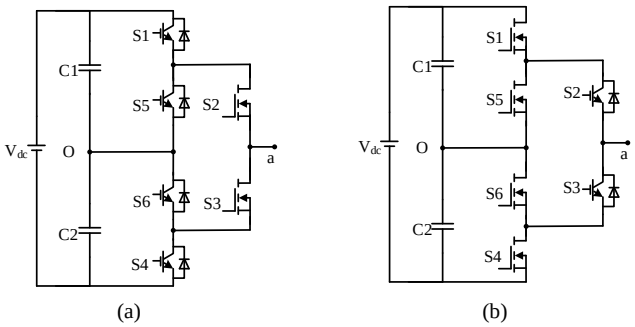

Fig. 2. Two types of Si&SiC hybrid 3L-ANPC topology [19]-[21]. (a). With 2 SiC MOSFETs. (b). With 4 SiC MOSFETs.

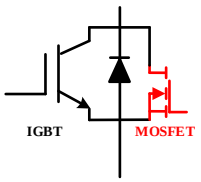

Fig. 3. Configuration Si/SiC HyS.

TABLE I
Output Status of 3L-ANPC Inverter

Output Status	S1	S2	S3	S4	S5	S6
"P" state	1	1	0	0	0	0/1
"O" state-1	0	1	0	0/1	1	0
"O" state-2	0	1	1	0	1	1
"O" state-3	0/1	0	1	0	0	1
"N" state	0	0	1	1	0/1	0

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The rest of this paper is organized as follows: Section II provides a brief introduction about the 3L-ANPC inverter and the two Si&SiC hybrid 3L-ANPC structures proposed in [19], [20], and [21]. Then, two types of Si/SiC HyS-based 3L-ANPC inverters are proposed and analyzed. In section III, loss and thermal models of the Si/SiC HyS-based 3L-ANPC inverters are investigated. Based on the loss and thermal model, the inverter performance between different hybrid schemes is presented in Section IV. Experimental comparisons are carried out on a universal 3L-ANPC prototype in Section V. Finally, the conclusions are presented in Section VI.

II. Proposed Si/SiC HyS-Based 3L-ANPC Inverters

A. 3L-ANPC Inverter

The one-leg 3L-ANPC topology has six active switches with antiparallel diodes. Compared to the diode-clamped NPC inverter, S5 and S6 are replaced by the active switches to obtain more midpoint clamping paths. The dc voltage is divided by the split capacitors and creates three-level output voltage status at the inverter output. The output status and corresponding switch states are listed in Table I, where "P", "O", and "N" states represent the output voltage equal to "+V_{dc}/2", "0", and "-V_{dc}/2". When V_{ao} is +V_{dc}/2, S1 and S2 are turned on. S6 can also be turned on to clamp the device voltage of S3 and S4 to V_{dc}/2. When V_{ao} is 0, three "O" states, named "O" state-1, "O" state-2, and "O" state-3, can be utilized to clamp the midpoint. In "O" state-1, S2 and S5 are turned on to commutate inductor current. Symmetrically, in "O" state-3, S3 and S6 are turned on to conduct current. In "O" state-2, the switches S2, S3, S5, and S6 are all turned on.

By selecting different "O" state paths, the conduction losses of the semiconductor devices in NPC paths can be controlled. The switching losses can be adjusted by the selection of different switching sequences. Two PWM strategies for 3L-ANPC, as illustrated in Fig. 4, were discussed in the literature [12]. In Fig. 4, U_m, U_{c1}, and U_{c2} are the modulation waveform and positive carrier and negative carrier, respectively. G_{S1} to G_{S6} are the gate signals for the active switches S1 to S6, respectively. In the case of PWM-1, S2 and S3 produce the carrier frequency switching losses while the other switches only produce line frequency (50/60Hz) neglectable switching losses. In the case of PWM-2, The high-frequency switching losses only occur in S1, S5, S4, and S6. Other switches only generate conduction losses and line frequency losses. It is noted that the semiconductor losses can be controlled by the selection of NPC paths. Based on this characteristic, the SiC MOSFETs are used in the 3L-ANPC inverters to fully utilize the low switching loss characteristic and improve the inverter performance on efficiency, power quality, etc.. The Si&SiC hybrid 3L-ANPC inverters are proposed in [19], [20], and [21]. Only part of the Si devices are replaced by the SiC MOSFETs to minimize the semiconductor device cost. Fig. 2 (a) shows the topology of hybrid 3L-ANPC with two SiC

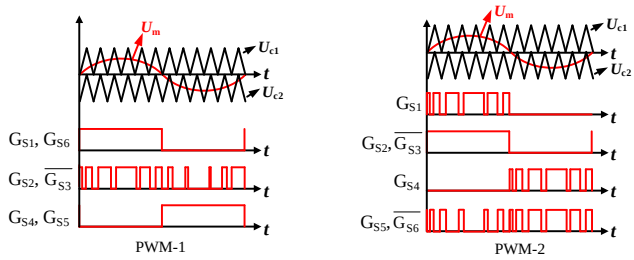

Fig. 4. Two PWM strategies for 3L-ANPC.

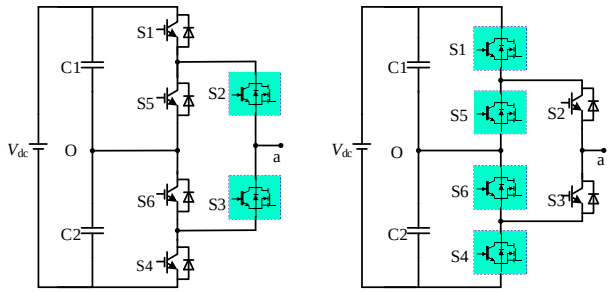

Fig. 5. Proposed two types of Si/SiC HyS-based 3L-ANPC topologies. (a) 2-Si/SiC HyS-based 3L-ANPC. (b) 4-Si/SiC HyS-based 3L-ANPC.

MOSFETs controlled by the PWM-1, illustrated in Fig. 4. All the carrier frequency switching losses only occur in the SiC MOSFETs. In literature [19], the simulation results of a 2-SiC MOSFETs hybrid 3L-ANPC inverter with the specifications of 650 V dc voltage, 21 A output current, and 208 V ac voltage presented that the SiC MOSFETs produce 11.6 W switching losses which is about 26% of the total semiconductor losses at the switching frequency of 45 kHz. Similar results can be found in the literature [21], 6.9 W switching losses which is equal to 27% of the total semiconductor losses are produced by the SiC MOSFETs S2 and S3 on a 2-SiC MOSFETs hybrid 3L-ANPC prototype with the specification of 800 V dc voltage, and 2 kW output power. The 4-SiC MOSFETs hybrid 3L-ANPC inverter utilizing PWM-2 strategy, as shown in Fig. 2 (b), is also proposed in [21] to centralize the switching losses on S1, S4, S5, and S6.

The two types of SiC MOSFET hybrid 3L-ANPC inverter mentioned above both featured a better efficiency performance, but they still have relatively high device cost for the full current-rated SiC MOSFETs. The cost reduction becomes insignificant in the 4-SiC hybrid scheme. To further reduce the semiconductor device cost for the 3L-ANPC inverter while maintaining a high inverter efficiency, the Si/SiC HyS-based 3L-ANPC inverter is proposed and depicted in Fig. 5. The Si IGBTs within the Si/SiC HyS achieve ZVS by the gate driving sequence of SiC MOSFET turns first and turns off last, so the 3L-ANPC inverter can still maintain low switching losses. Additionally, only small current-rated SiC MOSFETs are

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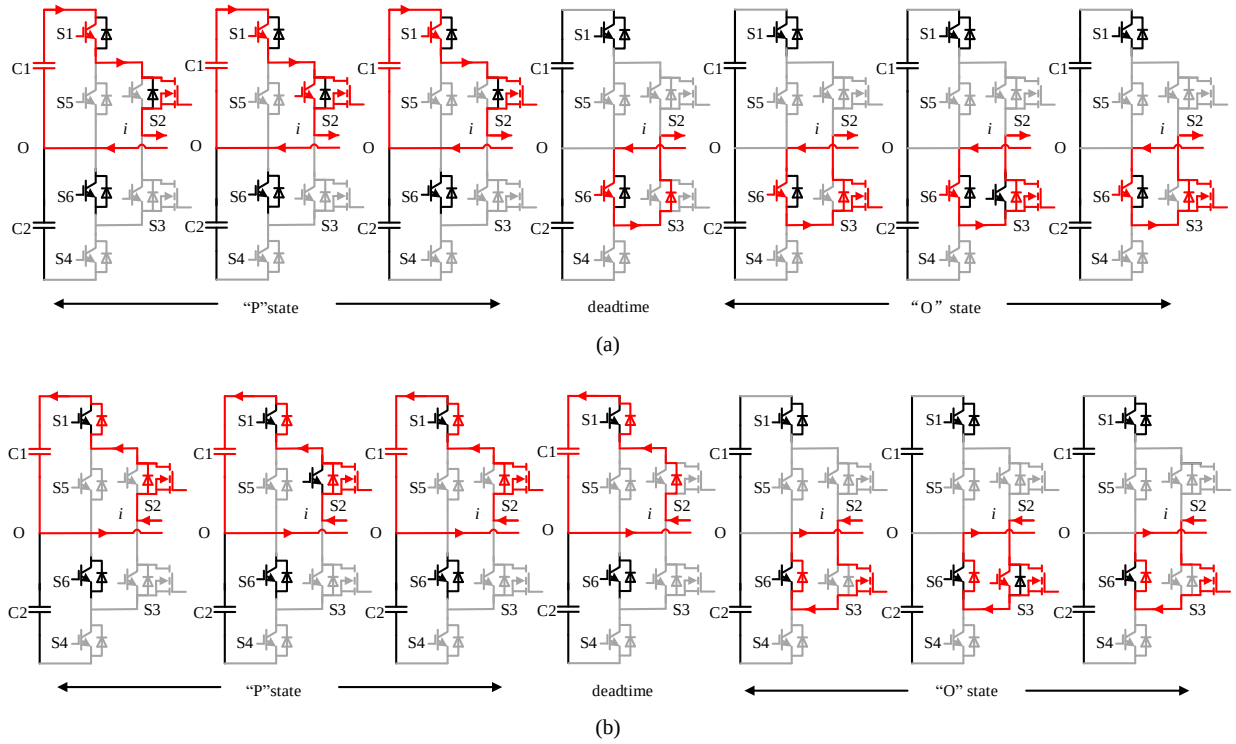

Fig. 6. Commutation analysis of 2-Si/SiC HyS-based 3L-ANPC inverter from "P" state to "O" state. (a) Positive inductor current. (b) Negative inductor current.

needed in the topology, the device cost is also reduced compared to the use of full current-rated SiC MOSFETs.

B. 2-Si/SiC HyS-Based 3L-ANPC Inverter

The 2-Si/SiC HyS-based 3L-ANPC inverter, as illustrated in Fig. 5 (a), utilizes PWM-1 modulation strategy. When the inductor current is positive, the commutation process is demonstrated in Fig. 6 (a) and introduced below.

1) During the "P" state, S1 and S2 are turned on to output $+V_{dc}/2$. S6 is also turned on to clamp the blocking voltage of S3 and S4 to $+V_{dc}/2$. At this state, the SiC MOSFET of S2 is turned on first to commutate the inductor current. After the turn-on delay time, the Si IGBT of S2 is turned on by ZVS and shares the current with SiC MOSFET. At the end of "P" state, the Si IGBT of S2 is turned off first through ZVS. As a result, all the current is forced to the SiC MOSFET of S2. After the turn-off delay time. The SiC MOSFET of S2 is turned off. The SiC MOSFET of S2 produces switching losses.

2) During the deadtime, the current is commutated by S6 and the diode of S3.

3) During the "O" state, the SiC MOSFET of S3 is turned on first and operates at synchronous rectifier mode. After the turn-on delay time, Si IGBT of S3 is turned on. Since the Si IGBT cannot conduct current reversely, the current distribution is unchanged till the S2 is turned off. The diode of S3 generates recovery losses.

When the inductor current is negative, the commutation process is demonstrated in Fig. 6 (b).

1) At "P" state, the SiC MOSFET of S2 is turned on first and operates at synchronous rectifier mode to share the current with the diode of S2. After the turn-on delay time, the Si IGBT is turned on but it will not conduct current. When S2 is about to be turned off, the Si IGBT is turned off first. Then, the SiC MOSFET of S2 is turned off after the turn-off delay time. All the current is forced to the diode of S2.

2) During the deadtime, the current is commutated by the diodes of S2 and S1. At the end of deadtime, the diode of S2 produces recovery losses.

3) During the "O" state, the SiC MOSFET of S3 is turned on first. After the turn-on delay time, Si IGBT of S3 is turned on through ZVS to share the current with SiC MOSFET of S3. At the end of the "O" state, Si IGBT of S3 is turned off by ZVS. Then, the SiC MOSFET of S3 is turned off after the turn-off delay time. SiC MOSFET of S3 generates switching losses.

C. 4-Si/SiC HyS-Based 3L-ANPC Inverter

As depicted in Fig. 5 (b), the 4-Si/SiC HyS-based 3L-ANPC inverter utilizes PWM-2 modulation strategy. When the inductor current is positive, the commutation process is demonstrated in Fig. 7 (a) and introduced below.

1) During the "P" state, S1 and S2 are turned on to output $+V_{dc}/2$. S6 is also turned on to clamp the blocking voltage of S3 and S4 to $+V_{dc}/2$. At this state, the SiC MOSFET of S1 is turned on first to commutate the inductor current. After the turn-on delay time, the Si IGBT of S1 is turned on through ZVS and shares the current with SiC MOSFET. At the end of "P" state, the Si IGBT of S1 is turned off first by ZVS. All the current is forced to the SiC MOSFET of S1. After the turn-off delay time. The SiC MOSFET of S1 is turned off and produces switching losses.

2) During the deadtime, the current is commutated by S2

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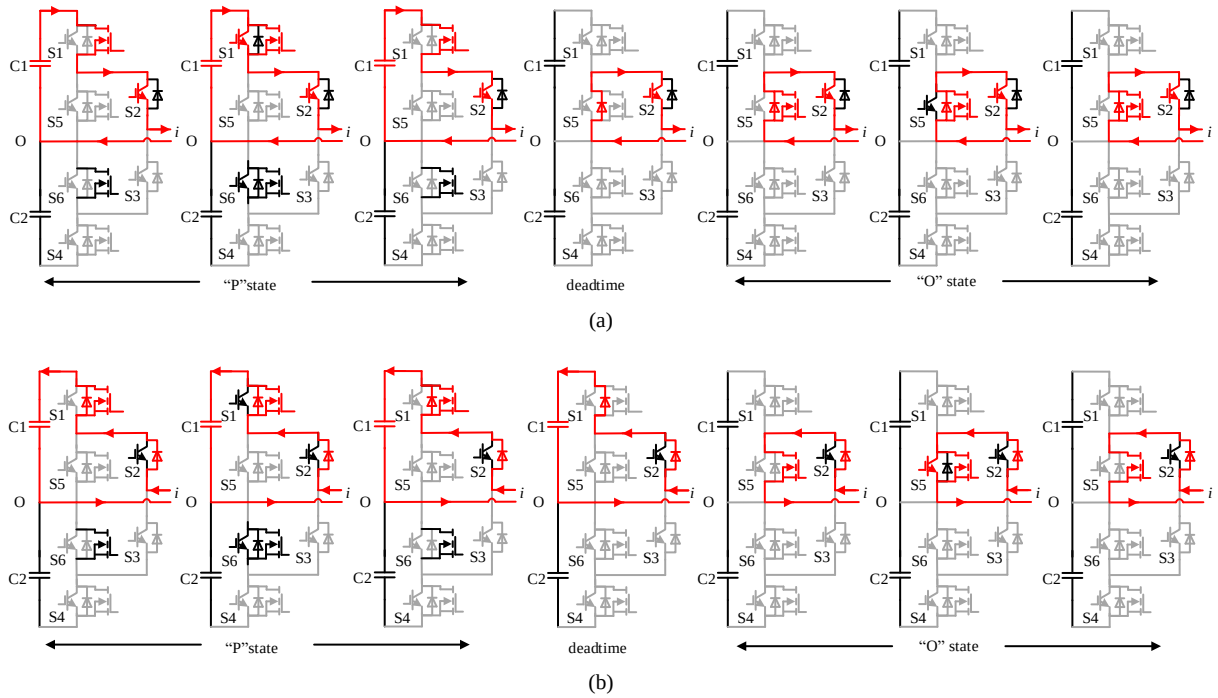

Fig. 7. Commutation analysis of 4-Si/SiC HyS-based 3L-ANPC inverter from "P" state to "O" state. (a) Positive inductor current. (b) Negative inductor current.

and the diode of S5.

3) During the "O" state, the SiC MOSFET of S5 is turned on first and operates at synchronous rectifier mode. After the turn-on delay time, Si IGBT of S5 is turned on but does not conduct current. The current distribution is unchanged till the S5 is turned off. The diode of S5 produces recovery losses.

When the inductor current is negative, the commutation process is demonstrated in Fig. 7 (b).

1) At "P" state, the SiC MOSFET of S1 is turned on and operates at synchronous rectifier mode to share the current with the diode of S1. After the turn-on delay time, the Si IGBT is turned on, but it will not conduct current. When S1 is about to be turned off, the Si IGBT is turned off first. After the turn-off delay time, the SiC MOSFET of S1 is turned off. All the current is forced to the diode of S1.

2) During the deadtime, the current is commutated by the diodes of S1 and S2. When the deadtime period ends, the diode of S1 produces recovery losses.

3) During the "O" state, the SiC MOSFET of S5 is turned on first. After the turn-on delay time, Si IGBT of S5 is turned on through ZVS and shares the current with SiC MOSFET. At the end of "O" state, Si IGBT of S5 is turned off through ZVS. After the turn-off delay time, The SiC MOSFET of S5 is turned off and produces switching losses.

III. Loss and Thermal Modeling

The Si/SiC HyS has great potential in improving the efficiency of the 3L-ANPC inverter. To demonstrate the efficiency and thermal performance of the Si/SiC HyS-based 3L-ANPC inverter, the switching and conduction

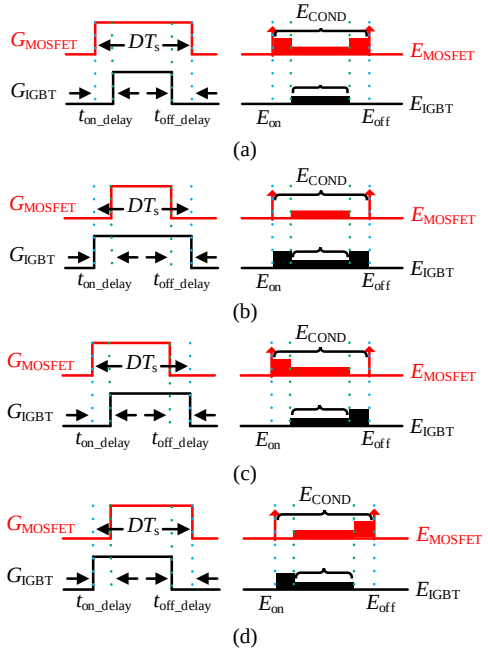

Fig. 8. Si/SiC HyS switching patterns.

characteristics of the Si/SiC HyS are analyzed. Then, the power loss, thermal models, and loss distribution of the Si/SiC HyS-based 3L-ANPC inverter are investigated. The estimated inverter efficiencies between the two types of Si/SiC HyS-based 3L-ANPC and full Si IGBT-based 3L-ANPC inverters are compared. In this paper, the Si/SiC HyS for the 3L-ANPC inverter is formed by a 650 V / 15 A SiC MOSFET SCT3120AL and a 600 V / 28 A Si IGBT IKW20N60T.

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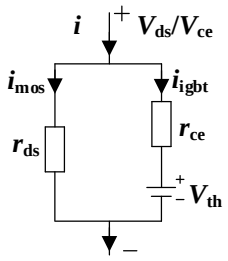

Fig. 9. Steady state conduction model of Si/SiC HyS,

A. Switching Characteristic of Si/SiC HyS

The switching characteristics of the Si/SiC HyS vary with different gate switching patterns for the Si IGBT and SiC MOSFET. Four types of gate switching patterns have been discussed and investigated in literature [22], [23], [26]. Fig. 8 shows the four switching patterns for the Si/SiC HyS and their semiconductor loss distribution. In Fig. 8, G_{MOSFET} and G_{IGBT} represent the gate signals of SiC MOSFET and Si IGBT in the Si/SiC HyS.The t_{on_delay} and t_{off_delay} are the turn on delay time and turn off delay time for the Si/SiC HyS. E_{on}, E_{off}, and E_{CON} are the turn on loss, turn off loss, and conduction loss produced by the devices. T_s is the switching period and D is the corresponding duty ratio. E_{MOSFET} and E_{IGBT} are the semiconductor loss produced by SiC MOSFET and Si IGBT in the switching cycle. Fig. 8 (a) depicts the gate switching pattern of SiC MOSFET turns-on first and turns-off last. The SiC MOSFET produces switching losses and conduction loss. The Si IGBT only generates conduction losses. It is noted that during the turn-on and turn-off delay time, the SiC MOSFET will produce high conduction losses. The gate switching pattern of SiC MOSFET turns-on first and turns-off last will be utilized to achieve low switching loss for the Si/SiC HyS. Fig. 8 (b) shows the gate switching pattern of Si IGBT turns on first and turns off last which means that all the switching losses are produced by the Si IGBT. This gate switching pattern sacrifices the Si/SiC HyS advantage of low switching loss while achieving a higher overload capability for the Si/SiC HyS [22], [23]. Fig. 8 (c) and (d) present the gate switching patterns of SiC MOSFET turns-on first and turns-off first, SiC MOSFET turns-on last and turns-off last, respectively. The two types of gate switching patterns are investigated in literature [30]. The junction temperatures of the SiC MOSFET and Si IGBT within the Si/SiC HyS can be balanced by the optimized gate delay time for the Si/SiC HyS. Although different gate switching patterns has been proposed for different operation condition, in most cases, the switching pattern of SiC MOSFET turns-on first and turns-off last is selected for the Si/SiC HyS due to the lower switching losses. In this work, the main purpose of utilizing Si/SiC HyS is to improve the 3L-ANPC inverter's efficiency while maintaining a low device cost, thus only the gate switching pattern of SiC MOSFET turns-on first and turns-off last is used and discussed.

B. Conduction Characteristic of Si/SiC HyS

Different from the conduction characteristic of a single semiconductor devices, the current flows through Si/SiC HyS is shared by the two paralleled devices. In the steady state, the Si/SiC HyS conduction model is depicted in Fig. 9. The Si IGBT is simplified as a voltage source which stands for the threshold voltage of Si IGBT in series with an on-resistance and the SiC MOSFET is simplified as an on-resistance. The conduction voltage of the Si/SiC HyS can be expressed by:

$$\begin{aligned} V_{ce} &= i_{igbt} \times r_{ce} + V_{th} \\ V_{ds} &= i_{mos} \times r_{ds} \end{aligned} \tag{1}$$

where V_{ce}, V_{ds} are the conduction voltages of Si/SiC HyS. i_{igbt} and i_{mos} are the currents shared by the Si IGBT and SiC MOSFET in steady state. r_{ce} and r_{ds} represent the on-resistances of the Si IGBT and SiC MOSFET. V_{th} is the threshold voltage of Si IGBT. i in Fig. 9 is the conduction current of Si/SiC HyS. The steady state current sharing can be calculated as:

$$i_{igbt} = \begin{cases} 0, & i < \dfrac{V_{th}}{r_{ds}} \\ \dfrac{i r_{ds} - V_{th}}{r_{ds} + r_{ce}}, & i > \dfrac{V_{th}}{r_{ds}} \end{cases} \tag{2}$$

$$i_{mos} = \begin{cases} i, & i < \dfrac{V_{th}}{r_{ds}} \\ \dfrac{i r_{ce} + V_{th}}{r_{ds} + r_{ce}}, & i > \dfrac{V_{th}}{r_{ds}} \end{cases} \tag{3}$$

When the inductor current flows through the Si/SiC HyS in the reverse direction, the inductor current will be shared by the antiparallel diode of Si IGBT and the SiC MOSFET. The conduction characteristic of the antiparallel diode has the same steady state conduction model as the Si IGBT, thus the reverse conduction model of the Si/SiC HyS can still be represented by the model shown in Fig. 9. The current shared by the Si IGBT antiparallel diode and SiC MOSFET can be calculated by (2) and (3) respectively.

C. Loss and Thermal Modeling for the 3L-ANPC Inverter

The switching loss of the semiconductor devices can be calculated by using the curve fitting and the behavioral loss model as follows [32]:

$$E_{Switch} = \begin{cases} E_{on}\left(i,\ T_j\right)\dfrac{V_{dc}/2}{V_{ds\_rated}} \\ E_{off}\left(i,\ T_j\right)\dfrac{V_{dc}/2}{V_{ds\_rated}} \end{cases} \tag{4}$$

where E_{on} and E_{off} are the turn-on and turn-off loss data extracted from the manufacturer's datasheet and they are dependent on the conduction current i, device junction temperature T_j and the drain-source voltage, which is $V_{dc}/2$ for the three-level inverters. V_{ds_rated} is the dc voltage when E_{on} and E_{off} are tested.

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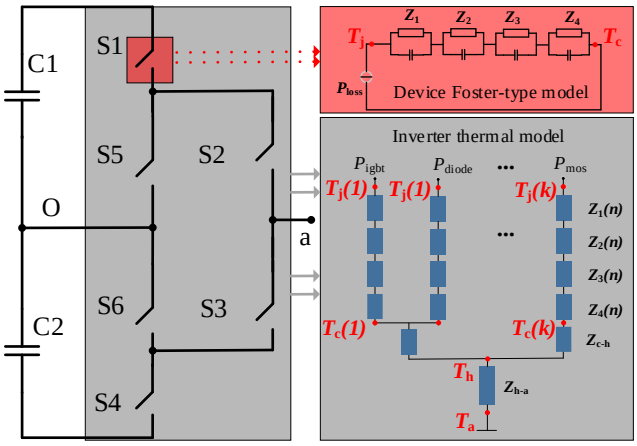

Fig. 10. Thermal model structure for the 3L-ANPC inverter.

It is assumed the switching frequency is f_s. The average switching losses in the n_{th} switching cycle $P_{Switch}(n)$ can be calculated by

$$P_{Switch}(n)=\begin{cases}P_{on}(n)=f_s E_{on}(n)\dfrac{V_{dc}/2}{V_{ds\_rated}}\\ P_{off}(n)=f_s E_{off}(n)\dfrac{V_{dc}/2}{V_{ds\_rated}}\end{cases} \tag{5}$$

where $P_{on}(n)$ and $P_{off}(n)$ are the average turn-on and turn-off power loss.

The recovery loss of antiparallel diode can be expressed by

$$P_{rec}(n)=f_s E_{rec}(n)\frac{V_{dc}/2}{V_{ds\_rated}} \tag{6}$$

where $E_{rec}(n)$ is the average recovery power loss of the antiparallel diode in the n_{th} switching cycle.

The conduction losses for the semiconductor devices can be calculated as

$$V_{ce}=r_{ce}(T_j)i_{igbt}+V_{th}(T_j) \tag{7}$$

$$V_{ds}=r_{ds}(T_j)i_{mos} \tag{8}$$

$$P_{con}=V_{ce}(i,\ T_j)i_{igbt}+V_{ds}(i,\ T_j)i_{mos} \tag{9}$$

it is noted that the conduction losses are dependent on the conduction current and junction temperature.

The conduction losses of the Si/SiC HyS can be estimated according to (2) and (3)

$$P_{con\_HyS\_igbt}(n)=\begin{cases}f_s\left(\dfrac{D(n)}{f_s}-t_{delay}\right)\left(i_{igbt}(n)r_{ce}+V_{th}\right)i_{igbt} & ,\ \dfrac{D(n)}{f_s}>t_{delay}\\ 0 & ,\ \dfrac{D(n)}{f_s}\le t_{delay}\end{cases} \tag{10}$$

$$P_{con\_HyS\_mosfet}(n)=\begin{cases}f_s\left\{\left(\dfrac{D(n)}{f_s}-t_{delay}\right)i^2_{mos}(n)r_{ds}+t_{delay}i^2(n)r_{ds}\right\} & ,\ \dfrac{D(n)}{f_s}>t_{delay}\\ D(n)\cdot i^2(n)r_{ds} & ,\ \dfrac{D(n)}{f_s}\le t_{delay}\end{cases} \tag{11}$$

where t_{delay} is the sum of the turn-on delay time t_{on_delay} and the turn-off delay time t_{off_delay}. $D(n)$ is the duty ratio of n_{th} switching cycle. $i_{igbt}(n)$, $i_{mos}(n)$, and $i(n)$ are the current shared by Si IGBT, SiC MOSFET and the inductor current in n_{th} switching cycle. $P_{con\_HyS\_igbt}$ and $P_{con\_HyS\_mosfet}$ are Si/SiC HyS average conduction losses distributed to the IGBT and MOSFET in n_{th} switching cycle. When the current reversely flow through Si/SiC HyS, the diode shares inductor current with the SiC MOSFET which operates under synchronous rectifier mode. The SiC MOSFET body diode will not conduct current in steady state due to its high conduction voltage. The conduction power loss for the diode and SiC MOSFET can be estimated similarly to (10) and (11) since the diode has the same conduction equivalent circuit as Si IGBT.

The conduction losses for the full Si IGBT and its antiparallel diode are calculated by

$$P_{con\_igbt}(n)=D(n)\cdot\left(i(n)r_{ce}+V_{th\_igbt}\right)i \tag{12}$$

$$P_{con\_diode}(n)=D(n)\cdot\left(i(n)r_{diode}+V_{th\_diode}\right)i \tag{13}$$

where P_{con_igbt} and P_{con_diode} refer to the average conduction loss of the full current-rated Si IGBT and its antiparallel diode in n_{th} switching cycle.

The total average power loss produced in n_{th} switching cycle can be calculated by adding the switching loss (recovery loss for diode) and conduction loss in n_{th} switching cycle.

$$P_{device\_total}(n)=P_{switch}(n)+P_{con}(n) \tag{14}$$

According to loss modeling, the thermal model is also required to complete system loss and thermal analysis by feeding back the device junction temperatures for the switching and conduction loss calculation. In addition, thermal performance analysis is of critical importance to the output capacity, reliability of power inverters.

As illustrated in Fig. 10, four layers Foster-type RC network, including Z_1 to Z_4, representing the thermal model from device junction to case is utilized to model the semiconductor devices. The Foster model only consists of lumped RC values and no physical meanings. In the system thermal model, each device has one more layer from device case to the heatsink $Z_{c\text{-}h}$, which represents the thermal impedance of thermal pad and the thermal grease. The antiparallel diode is packaged along with the Si IGBT, thus they share one device case and have one $Z_{c\text{-}h}$. In Fig. 10, T_j and T_c are the device junction temperatures and case temperatures. T_h and T_a represent the heatsink temperature and ambient temperature.

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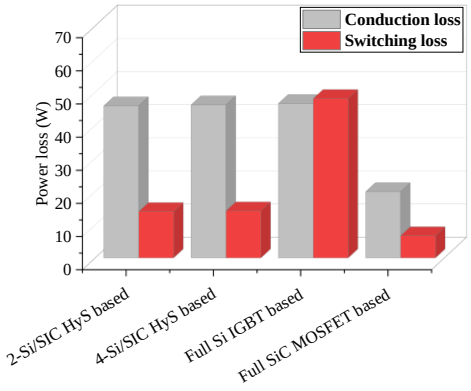

Fig. 11. Loss comparison of different 3L-ANPC inverter solutions.

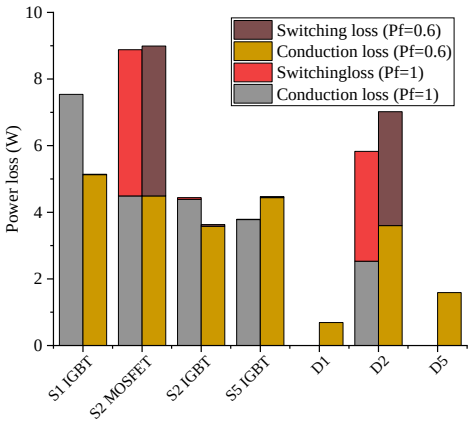

Fig. 12. Loss breakdown for 2-Si/SiC HyS-based 3L-ANPC inverter.

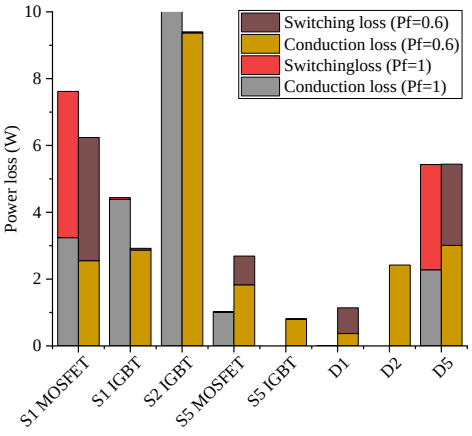

Fig. 13. Loss breakdown for 4-Si/SiC HyS-based 3L-ANPC inverter.

With a proper assumed initial temperature of heatsink, case, or ambient and the thermal parameters provided by manufacturer's datasheets, the device's junction temperature can be estimated by

$$T_{\mathrm{j}} = P_{\mathrm{loss}} \sum_{m=1}^{4} Z_{\mathrm{m}} + T_{\mathrm{c}} = P_{\mathrm{loss}} \sum_{m=1}^{4} \frac{R_{\mathrm{m}}}{\tau_{\mathrm{ms}}+1} + T_{\mathrm{c}} \qquad (15)$$

TABLE II
SYSTEM PARAMETERS

Parameter	Value
Dc voltage, V_{dc}	750V
Switching frequency, f_{s}	40kHz
Output ac voltage V_{o}	220V/50Hz
Output power, P_{o}	4.4kW
$T_{\mathrm{on\_delay}}$, $T_{\mathrm{off\_delay}}$	1μs, 1μs

where T_{j}, P_{loss}, and T_{c} are respectively the junction temperature, pulse power loss profile, and case temperature.

IV. THEORETICAL COMPARISON OF DIFFERENT 3L-ANPC INVERTER SOLUTIONS

In this section, the semiconductor loss comparison is firstly made between the full Si IGBT-based 3L-ANPC inverter, 2-Si/SiC HyS-based 3L-ANPC inverter, and 4-Si/SiC HyS-based 3L-ANPC inverter. Then, the semiconductor loss breakdowns are analyzed. Lastly, the power output capability is evaluated and compared between the two types of Si/SiC HyS-based 3L-ANPC inverters.

The comparisons are made under the system parameters shown in Table II. In the comparison, the Si/SiC HyS is formed by one Rohm SiC MOSFET SCT3120AL (650 V / 15 A) and one Infineon Si IGBT IKW20N60T (600 V / 28 A). The full current-rated Si IGBTs utilized in the 3L-ANPC is Infineon IKW30N60T (600 V / 39 A).

Fig. 11 shows the semiconductor loss comparison between the 2-Si/SiC HyS-based 3L-ANPC, 4-Si/SiC HyS-based 3L-ANPC, the full Si IGBT-based 3L-ANPC, and full SiC MOSFET-based 3L-ANPC inverters. It is illustrated in the figure that the conduction losses are almost the same among the first three solutions. The conduction loss of full SiC MOSFET-based 3L-ANPC inverter is about half of the first three solutions. This is decided by the V-I characteristics of the different semiconductor devices. Benefiting from the fast-switching characteristic of SiC MOSFET, the switching losses of the Si/SiC HyS-based 3L-ANPC inverters are much lower than the full Si IGBT-based solution. For the two Si/SiC HyS-based 3L-ANPC inverters, all the switching losses are produced by the Si/SiC HyS, thereby having the same switching losses. Compared to the full SiC MOSFET-based 3L-ANPC inverter, the switching loss of the proposed two types of Si/SiC HyS-based 3L-ANPC inverter is higher. The first reason is that the SiC MOSFET in the Si/SiC HyS has a lower current rating which means a naturally higher switching loss. The second reason is that the full SiC MOSFET-based 3L-ANPC inverter utilizes the body diode to commutate the load current during the dead time. There will be no recovery loss for the SiC MOSFET body diode. In the Si/SiC HyS, a Si diode (with the Si IGBT) is used as the antiparallel diode, thus there will be recovery losses.

The loss breakdown for the 2-Si/SiC HyS-based 3L-ANPC inverter is shown in Fig. 12. Since the 3L-ANPC inverter operates symmetrically between the top devices S1,

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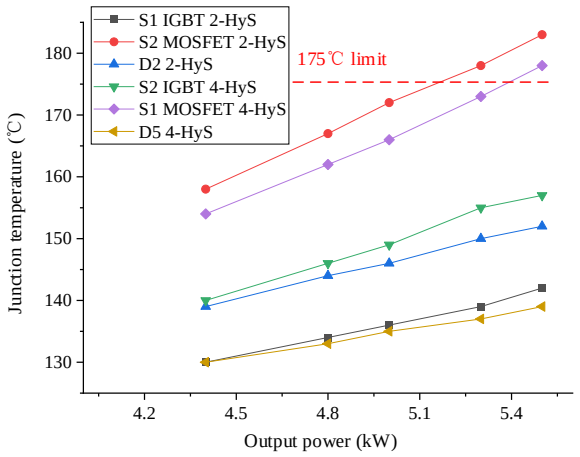

Fig. 14. Device junction temperature estimation under different output power.

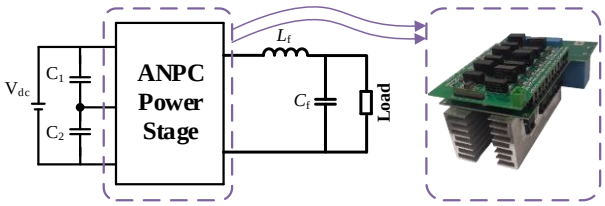

Fig. 15. Half-bridge single-phase universal 3L-ANPC experimental prototype.

S2, S5, and the bottom devices S4, S3 S6, only the top three devices' losses are calculated and presented. It is noted that all the switching losses and recovery losses are produced by the SiC MOSFETs and the antiparallel didoes of S2, respectively. The other four Si IGBTs only produce conduction losses. When the power factor changes from 1 to 0.6 (lagging), the conduction losses produced by S1 IGBT decrease, and the conduction losses generated by the diodes increase. The switching losses are still produced by the middle two switches S2 and S3. For the loss breakdown of 4-Si/SiC HyS-based 3L-ANPC inverter, shown in Fig. 13, when inverter operates at unity power factor, all the switching losses and recovery losses are produced by the SiC MOSFET in S1 and the diode of S5. When it operates at a lower power factor, the switching losses are distributed between the SiC MOSFETs of S1 and S5. The recovery losses are also shared by D1 and D5. The theoretical loss calculation validates that the proposed PWM strategies effectively concentrate all switching losses to the SiC MOSFETs in the Si/SiC HyS-based 3L-ANPC topology.

It is noted that under the Si/SiC HyS configuration of Fig. 3, the antiparallel diode switching characteristic will affect the system efficiency by producing recovery losses. Using an individual SiC diode to replace the antiparallel diode of Si IGBT can avoid the recovery losses but it will also result in a higher device cost and design complexity. Removing the antiparallel diode and utilizing the SiC MOSFET body diode can also avoid the recovery losses, but it leads to higher thermal stress for the SiC MOSFET and increase the conduction losses due to the bad conduction characteristic of the body diode. This discussion about this part is not the focus of this paper, thereby not discussed further.

Based on the loss breakdown analysis of the two types of Si/SiC HyS-based 3L-ANPC inverters, it is also noted that for the 2-Si/SiC HyS-based 3L-ANPC inverter, S1 IGBT, S2 MOSFET, and D2 have higher thermal stress than other devices. In the 4-Si/SiC HyS-based 3L-ANPC inverter, S1 MOSFET, S2 IGBT, and D5 have higher thermal stress than other devices. Thermal performance is an important factor for power inverters. Unbalanced thermal distribution will not only affect the inverter reliability but limit the inverter output capacity. In order to compare the power output capability of the two Si/SiC HyS-based 3L-ANPC inverters, the device junction temperatures are estimated and compared based on the thermal and loss model proposed in Section III.

From the device's datasheet, the maximum allowable junction temperature for both the Si IGBTs and the SiC MOSFET is 175 ℃. The inverter maximum output capacity can be found at the point of the most heated device in the topology reaching the 175 ℃ limit. Assuming the heatsink temperature is 80 ℃, the device junction temperatures can be estimated with the power loss profile for each semiconductor device.

The junction temperatures of the two types of Si/SiC HyS-based 3L-ANPC inverters under different power levels are calculated and depicted in Fig. 14. It is shown that the SiC MOSFETs are always the most heated devices in the two hybrid schemes. With the increase of inverter output power, the 2-Si/SiC HyS-based 3L-ANPC reaches the limit first with the output power of 5.17 kW. While the maximum output power for 4-Si/SiC HyS-based 3L-ANPC is 5.4 kW which is limited by S1 SiC MOSFET. The results show that the 4-Si/SiC HyS-based 3L-ANPC inverter has a higher power output capacity and is more suitable for high power density applications.

V. Experimental Results

To validate the efficiency benefits from the Si/SiC HyS and further investigate the switching and conduction characteristics of the Si/SiC HyS in the continuous inverter operation, a half-bridge single-phase universal 3L-ANPC inverter, as shown in Fig. 15, was developed to evaluate the feasibility of the proposed Si/SiC HyS-based 3L-ANPC inverters. The testing parameters are listed in Table III. In Table III, R_g, V_{gs} represent the gate resistance and gate driving voltages. The inverter efficiency was measured with Tektronix power analyzer PA3000. Rogowski coil current sensor TRCP0300 was utilized to measure the Si IGBT and SiC MOSFET drain-source current.

The normal operation of the Si/SiC HyS-based 3L-ANPC inverters is tested and the waveforms are shown in Fig. 16. The three-level output voltage and current, depicted in Fig. 16 (a), show that the inverter output voltage has three levels: $+V_{dc}/2$, 0, $-V_{dc}/2$ and the inverter has sinusoidal output

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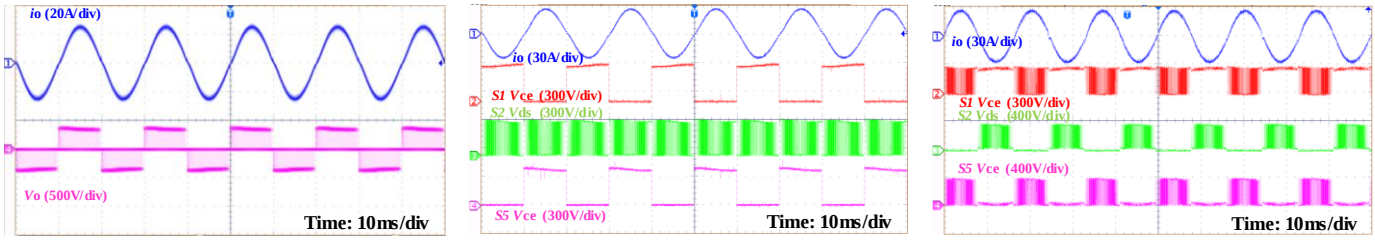
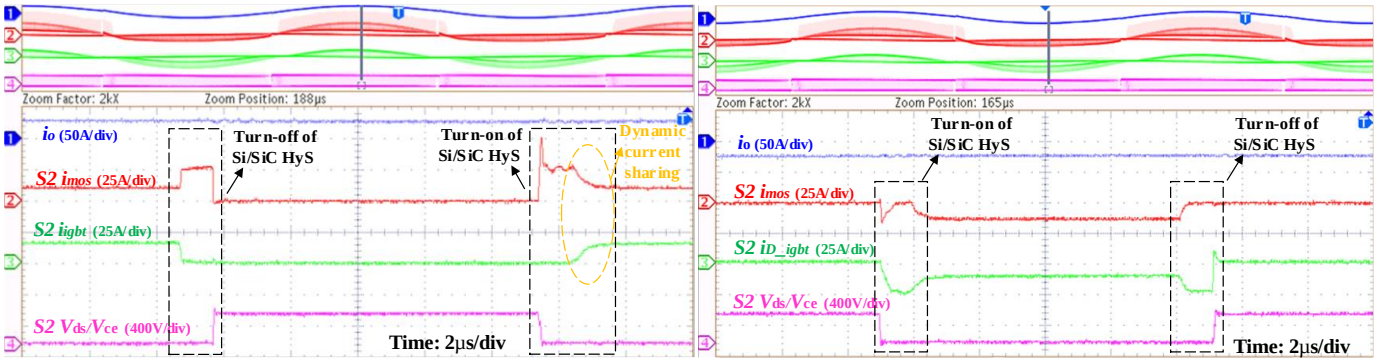


(a) (b) (c)

Fig. 16. Inverter normal operation waveforms. (a). Inverter output voltage and current. (b). 2-Si/SiC HyS-based 3L-ANPC. (c). 4-Si/SiC HyS-based 3L-ANPC.



(a) (b)

Fig. 17. Si/SiC HyS switching waveforms. (a). Forward conduction. (b). Reverse conduction.

TABLE III
TESTING PARAMETERS

Parameter	Value
Dc voltage, V_{dc}	750V
Output ac voltage V_o	220V/50Hz
Output power P_r	4.4kW
Switching frequency f_s	20kHz, 40kHz
Filter inductor L_f	1mH
Filter capacitor C_f	5µF
T_{on_delay}, T_{off_delay}	1µs, 1µs
R_g for SiC MOSFET	7Ω
R_g for Si IGBT	10Ω
V_{gs} for SiC MOSFET	+18V/0V
V_{ge} for Si IGBT	+15V/-9V
Si/SC HyS	SCT3120AL (650 V / 15 A)+ IKW20N60T (600 V / 28 A)
Full Si IGBT	IKW30N60T (600 V / 39 A)
Full SiC MOSFET	SCT3030AL (650 V / 49 A)

current. It is noted that the inverter output voltage and current are unrelated to the 3L-ANPC hybrid schemes and the modulation methods. The drain-source voltage of S1, S2, and S5 for the two types of Si/SiC HyS-based 3L-ANPC inverter are shown in Fig. 16 (b) and Fig. 16 (c), respectively. In Fig. 16 (b), it is noted that S1 and S5 switch at the line frequency (50 Hz). The inner switch S2 switches at high frequency. In Fig. 16 (c), although the gate signal of S1 and S2 are kept constant low in the negative half cycle, the drain-source voltage of S1 and S2 still have two levels. This is because, in the negative half cycle, S5 switches in high frequency with S4. When S4 is turned on, S1 and S2 are clamped to block the voltage $+V_{dc}/2$. When S5 is turned off, S5 and S2 are connected in parallel and in series with S1 to block the voltage $+V_{dc}/2$. Thus, the voltage of $+V_{dc}/2$ is divided based on the off-state equivalent RC networks of S1, S2, and S5.

A. Si/SiC HyS Switching Waveform Analysis

The Si/SiC HyS switching waveforms of forward conduction are depicted in Fig. 17 (a). The inductor current flows forward through the Si/SiC HyS. It is noted that during the turn-on process, the SiC MOSFET is turned on first. After the 1µs turn-on delay time, the Si IGBT is turned on under the SiC MOSFET's conduction voltage which can be seen as a zero-voltage turn-on. After the Si IGBT's turn-on, a dynamic current sharing process which is caused by the parasitic inductance in the internal power loop of Si/SiC HyS is observed. In Fig. 17 (a), the dynamic current sharing process takes about 1.2µs. During the turn-off process, Si IGBT is turned off first. After 1µs turn-off delay time, the SiC MOSFET is turned off.

The switching waveforms of reverse conduction are shown in Fig. 17 (b). The inductor current flows through the Si/SiC HyS in the reverse direction. In the turn-on transient, the SiC MOSFET body diode and the antiparallel diode of Si IGBT commutate the inductor current. Then, due to the low conduction voltage of the antiparallel diode of Si IGBT, the current shared by the antiparallel diode increases and the current shared by body diode of SiC MOSFET decreases. After the dead time, SiC MOSFET is turned on, and the MOSFET channel starts to share current with the antiparallel diode of Si IGBT. In the turn-off process, SiC MOSFET is turned off and all the current is commutated by the

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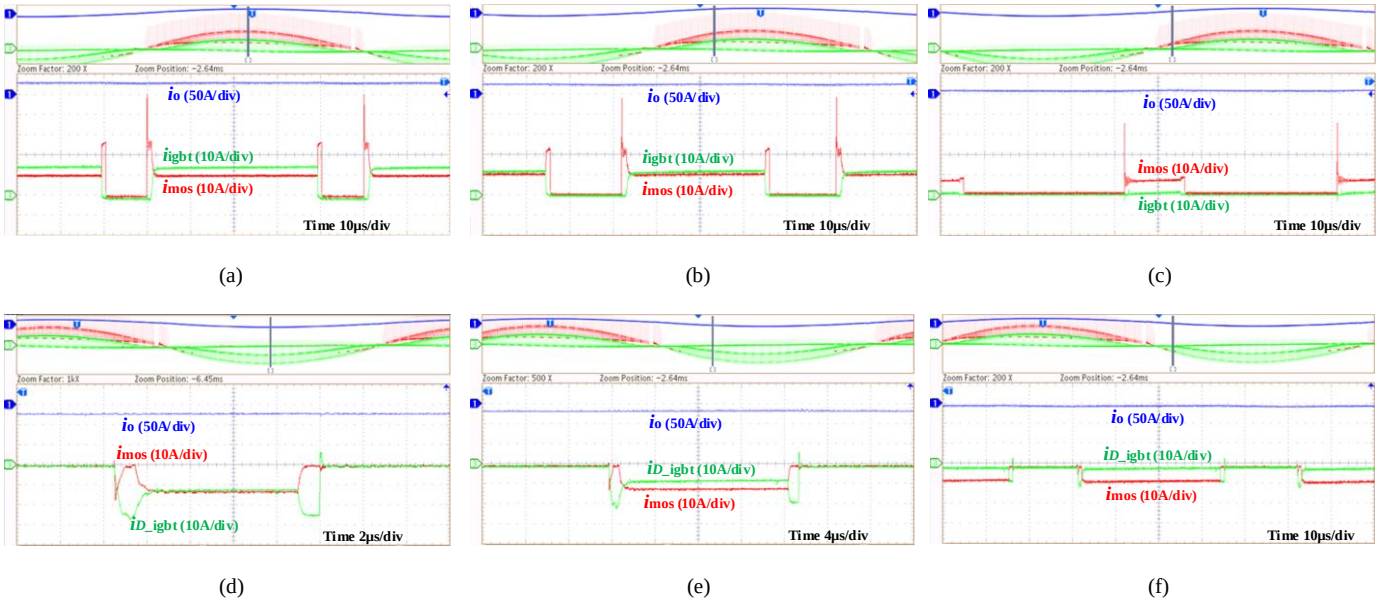

Fig. 18. Steady state current sharing of the Si/SiC HyS. (a). π/2. (b). π/4. (c). π/16. (d). -π/2. (e). -π/4. (f).-π/16.

antiparallel diode during the dead time. Recovery losses are produced by the antiparallel diode.

B. Steady State Current Sharing

The steady state current sharing of Si/SiC HyS is shown in Fig. 18. The forward conduction current sharing waveforms at π/2, π/4, and π/16 of the output current are shown in Fig. 18 (a), (b), and (c) respectively. It is noted that at the peak point of the output current, Si IGBT shares more current than the SiC MOSFET. At π/4, the current ratio shared by Si IGBT decreases. At π/16, all the current is conducted by SiC MOSFET. The Si IGBT will not conduct since the conduction voltage is lower than the Si IGBT threshold voltage. Fig. 18 (d), (e), and (f) show the current sharing in the reverse conduction of Si/SiC HyS. The antiparallel diode shares current with the SiC MOSFET during the conduction. Like the forward conduction, at high current, the diode shares more current. With the decrease of load current, the current ratio shared by SiC MOSFET increase. The results shown in Fig. 18 validate the advantage of Si/SiC HyS in conduction characteristics. It is noted that the Si/SiC HyS has no threshold voltage when conducting low currents. This will help to improve the inverter light load efficiency. When conducting high current, Si IGBT will share more current and thus reducing the conduction voltage. This will help to improve the inverter overload capability.

C. Inverter Efficiency

The inverter efficiencies are tested under the parameters listed in Table III. The inverter efficiency was measured by Tektronix power analyzer PA3000. Fig. 19 demonstrated the inverter efficiency improvement by the Si/SiC HyS in the 3L-ANPC inverter. It is shown that the efficiencies of the two Si/SiC HyS-based 3L-ANPC inverters are very close in the full load range, but their efficiencies are both much higher than the full Si IGBT solution. Especially when the switching frequency increases, the Si IGBT solution shows a

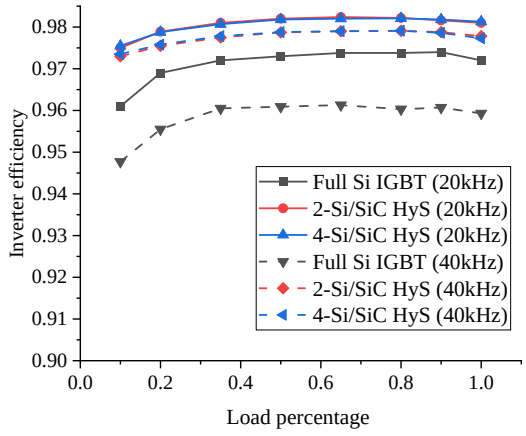

Fig. 19. Inverter efficiency improvement evaluation.

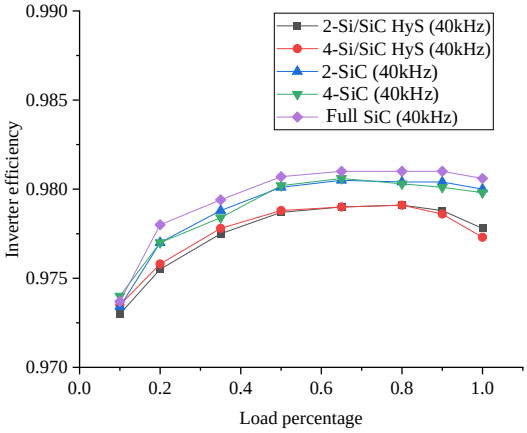

Fig. 20. Inverter efficiency comparison between different 3L-ANPC solutions.

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TABLE IV
TWO SI/SIC HYS-BASED 3L-ANPC SOLUTION COMPARISON

	Full Si IGBT 3L-ANPC (benchmark)	2-Si/SiC HyS-based 3L-ANPC	4-Si/SiC HyS-based 3L-ANPC
Inverter efficiency	94.7% at light load, 95.6% at heavy load	2.4% improvement at light load, 1.8% improvement at heavy load	2.4% improvement at light load, 1.8% improvement at heavy load
Power capability	N/A	5.17 kW	5.4 kW
Device cost	$17.9	$25.8	$33.8
Features	Most cost effective, lower efficiency and power density	Cost effective and high efficiency	High power density, high power capacity, and high efficiency

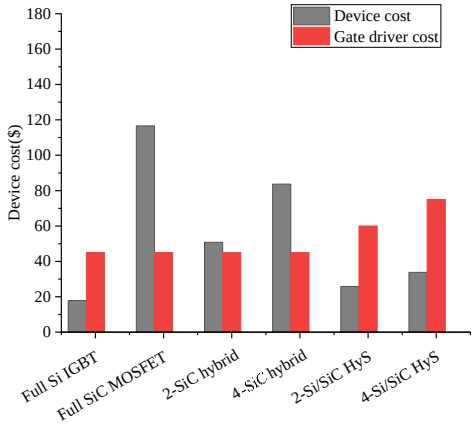

Fig. 21. Cost analysis for different 3L-ANPC solutions.

more significant efficiency drop. At 40 kHz switching frequency, the inverter efficiency improvement by the Si/SiC HyS is 2.4% and 1.8% at light load and heavy load conditions, respectively.

Fig. 20 shows the inverter efficiency comparison between the all SiC MOSFET 3L-ANPC solution, SiC MOSFET hybrid 3L-ANPC solution which is shown in Fig. 2 (a) and (b), and the proposed Si/SiC HyS-based 3L-ANPC solution. It is shown that all SiC MOSFET solution has the overall highest inverter efficiency. While the Si/SiC HyS-based 3L-ANPC solutions have the lowest efficiency, especially in the heavy load condition. A larger efficiency drop is observed in the heavy load condition. Small current-rated SiC MOSFET is used as the switching device in the Si/SiC HyS solution. The thermal stress of SiC MOSFET in the Si/SiC HyS solutions will be much higher than the full current-rated SiC MOSFET at the thermal steady state. Thus, the conduction and switching losses increase of the small current-rated SiC MOSFET is larger. In addition, in the Si/SiC HyS 3L-ANPC solution, the recovery losses of Si diode will also increase a lot due to the temperature rise. While for the other three solutions, full current-rated SiC MOSFETs are utilized. Usually, the SiC MOSFET with a higher current rating has a lower junction to case thermal resistance. For the example in this paper, the SiC MOSFET used in Si/SiC HyS is SCT3120AL (650 V/15 A), which has a junction-to-case thermal resistance of 1.12℃/W and the full current-rated SiC MOSFET used in the comparison is SCT3030AL (650 V/49 A), which has a junction-to-case thermal resistance of 0.44℃/W. The thermal stress of the larger SiC MOSFET will be lower than the SiC MOSFET in the Si/SiC HyS. Thus, the power loss increased by the rise of temperature is lower. In addition, the SiC MOSFET body diode commutates the load current during the dead time and will not produce any recovery losses. It is noted that there has been literature [30], [33] that investigated and provided an effective way to solve the problem of high thermal stress on SiC MOSFET in the Si/SiC HyS-based 3L-ANPC inverter at heavy load condition. The thermal stress problem will not be an obstacle in the development of Si/SiC HyS-based 3L-ANPC inverter.

D. Cost Comparison

The cost comparison including the device cost and the gate driver cost between different 3L-ANPC solutions is made and presented in Fig. 21. The device costs are from Mouser Electronics on a bulky order of 1000 pieces. It is shown that the full Si IGBT solution has the lowest device cost and the full SiC MOSFET solution has the highest device cost which is about 6.5 times the full Si IGBT solution. Compared to the 2-SiC hybrid scheme, the 4-SiC hybrid 3L-ANPC has a 1.7 times device cost while only showing an almost identical inverter efficiency. Compared to the full current-rated SiC MOSFET hybrid solution, the proposed Si/SiC HyS-based 3L-ANPC inverter shows a significantly lower device cost. The 2-Si/SiC HyS scheme only has 1.4 times device cost compared to the full Si IGBT solution.

The gate driver cost comparison shows that the cost for Si/SiC HyS-based 3L-ANPC inverter is higher, especially for the 4 Si/SiC HyS-based 3L-ANPC inverter. This is because that in this paper, two separate gate driver circuits are used for the Si/SiC HyS. But the gate driver cost will not be a big concern for this technology since there have been several papers [34], [35] that proposed the low cost compact gate driver circuit design that only utilized one gate driver and one gate signal for the Si/SiC HyS. The gate delay can be realized by the proposed circuit design. The effectiveness of the low cost gate driver design has been validated experimentally and shows great opportunity to overcome the cost disadvantages of Si/SiC HyS.

VI. CONCLUSION

Two Si/SiC HyS-based 3L-ANPC hybrid schemes are proposed in this paper. The inverter commutation characteristics, loss and thermal model, device cost comparison, efficiency, and thermal performance

comparison are investigated and presented. The evaluation results are concluded in Table IV and decribed as follows.

1) The inverter efficiency of the two proposed Si/SiC HyS-based 3L-ANPC inverters are very close in the full load range. Compared to the full Si IGBT-based 3L-ANPC inverter, the two types of Si/SiC HyS-based 3L-ANPC inverter both have a much higher inverter efficiency, especially when switching frequency increases. At 40kHz switching frequency, the inverter efficiency improvement by the Si/SiC HyS achieves 2.4% and 1.8% at light load and heavy load condition respectively. Meanwhile, the device cost for 2-Si/SiC HyS-based 3L-ANPC inverter is only 1.4 times of the full Si IGBT solution.

2) Compared with the full SiC MOSFET solution, the device cost of 2-Si/SiC HyS scheme is reduced by 78% while the maximum inverter efficiency sacrifice is only 0.28%. Compared with the 2-SiC MOSFET hybrid 3L-ANPC, the device cost is reduced by 50% with 0.21% maximum inverter efficiency drop at heavy load. The 2-Si/SiC HyS-based 3L-ANPC inverter shows great potential in improving the 3L-ANPC inverter's efficiency while maintaining a low device cost. This makes it a great candidate for cost-sensitive applications.

3) Compared to the 2-Si/SiC HyS-based 3L-ANPC inverter, the 4-Si/SiC HyS scheme has a higher power output capability, making it a better candidate for high power density applications.

REFERENCES

[1] S. S. Williamson, A. K. Rathore and F. Musavi, "Industrial electronics for electric transportation: current state-of-the-art and future challenges," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3021-3032, May. 2015.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, pp. 1292-1306, Sep./Oct. 2005.

[3] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D.P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron*., vol. 50, no. 5, pp. 962-981, Oct. 2003.

[4] Q. Li and P.Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron*., vol. 23, no. 3, pp. 1320–1333, May 2008.

[5] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Trans. Power Electron*., vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

[6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Jul. 2010.

[7] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency 3-level active neutral point clamped phase leg building block," *IEEE Trans. Power Electron*., vol. 29, no. 7, pp. 3255–3266, Feb. 2014.

[8] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013

[9] T. Brückner, S. Bernet, and P. K. Steimer, "Feedforward loss control of three-level active NPC converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1588–1596, Nov./Dec. 2007.

[10] C. Hu et al., "An improved virtual space vector modulation scheme for three-level active neutral-point-clamped inverter," *IEEE Trans. Power Electron*., vol. 32, no. 10, pp. 7419–7434, Oct. 2017.

[11] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron*., vol. 61, no. 2, pp. 835–845, Feb. 2014.

[12] D. Floricau, E. Floricau, and M. Dumitrescu, "Natural doubling of the apparent switching frequency using three-level ANPC converter," in *Proc. ISNCC Conf. Rec.*, Lágow, Poland, Jun. 2008, pp. 1–6.

[13] L. Ma, T. Kerekes, P. Rodriguez, X. Jin, R. Teodorescu and M. Liserre, "A New PWM Strategy for Grid-Connected Half-Bridge Active NPC Converters With Losses Distribution Balancing Mechanism," *IEEE Trans. on Power Electron.*, vol. 30, no. 9, pp. 5331-5340, Sept. 2015.

[14] B. Zhang, Q. Ge, P. Wang, X. Wang and Y. Yu, "A novel modulation strategy providing loss balancing and neutral point potential balancing for three-level active neutral-point-clamped converter," in *Proc. 17th Eur. Conf. Power Electron. Appl*., 2015, pp. 1-9.

[15] X. Jing, J. He and N. A. O. Demerdash, "Loss balancing SVPWM for active NPC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo*., 2014, pp. 281-288.

[16] E. Gurpinar and A. Castellazzi, "Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs and GaN HEMTs," *IEEE Trans. Power Electron*., vol. 31, no. 10, pp. 7148–7160, Oct. 2016.

[17] N. He, M. Chen, J. Wu, N. Zhu, and D. X. Ge, "20 kW zero-voltage-switching SiC-MOSFET grid inverter with 300 kHz switching frequency," *IEEE Trans. Power Electron*., vol. 34, no. 6, pp. 5175–5190, Jun. 2019.

[18] N. He, Y. Li, C. Du, C. Liu, C. Hu, and D. Xu, "SiC MOSFET zero-voltage-switching SVM controlled three-phase grid inverter," in *Proc. IEEE Energy Convers. Congr. Expo*., Milwaukee, WI, USA, 2016, pp. 1–8.

[19] Q. Guan et al., "An extremely high efficient three-level active neutral-point-clamped converter comprising SiC and Si hybrid power stages," *IEEE Trans. Power Electron*., vol. 33, no. 10, pp. 8341-8352, Oct. 2018.

[20] M. Abarzadeh, N. Weise and S. Caron, "A Generalized Scalable Configuration of Hybrid "Si+SiC" Paralleled Modular ANPC Converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2021, pp. 2791-2797.

[21] L. Zhang et al., "Evaluation of different Si/SiC hyrbid three-level active NPC inverters for high power density," *IEEE Trans. Power Electron*., vol. 35, no. 8, pp. 8224–8236, Aug. 2020.

[22] T. Zhao and J. He, "An optimal switching pattern for "SiC+Si" hybrid device based voltage source converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 1276–1281.

[23] J. He, R. Katebi, and N.Weise, "A current-dependent switching strategy for Si/SiC hybrid switch-based power converters," *IEEE Trans. Ind. Electron*., vol. 64, no. 10, pp. 8344–8352, Oct. 2017.

[24] A. Deshpande and F. Luo, "Practical design considerations for a Si IGBT + SiC MOSFET hybrid switch: Parasitic interconnect influences, cost, and current ratio optimization," *IEEE Trans. Power Electron*., vol. 34, no. 1, pp. 724–737, Jan. 2019.

[25] X. Song, A. Q. Huang, M. Lee, and C. Peng, "High voltage Si/SiC hybrid switch: An ideal next step for SiC," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices ICs*, 2015, pp. 289–292.

[26] Y. Wang, M. Chen, C. Yan, and D. Xu, "Efficiency improvement of grid inverters with hybrid devices," *IEEE Trans. Power Electron*., vol. 34, no. 8, pp. 7558–7572, Aug. 2019.

[27] X. Song, A. Q. Huang, P. Liu, and L. Zhang, "1200V/200A FREEDMpair: Loss and cost reduction analysis," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl*., Fayetteville, AR, USA, 2016, pp. 152–157.

[28] Z. Peng et al., "A variable-frequency current-dependent switching strategy to improve tradeoff between efficiency and SiC MOSFET overcurrent stress in Si/sic-Hybrid-Switch-Based inverters," *IEEE Trans. Power Electron*., vol. 36, no. 4, pp. 4877–4886, Apr. 2021.

[29] Z. Peng, J. Wang, Z. Liu, Y. Dai, G. Zeng, and Z. J. Shen, "Fault-tolerant inverter operation based on Si/SiC hybrid switch," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 8, no. 1, pp. 545–556, Mar. 2020.

[30] J. Wang, Z. Li, X. Jiang, C. Zeng, and Z. J. Shen, "Gate control optimization of Si/SiC hybrid switch for junction temperature balance

and power loss reduction," *IEEE Trans. Power Electron*., vol. 34, no. 2, pp. 1744–1754, Feb. 2019.

[31] D. Woldegiorgis, Y. Wu, Y. Wei and A. Mantooth, "A High Efficiency and Low Cost ANPC Inverter Using Hybrid Si/SiC Switches," in *IEEE Open J. Ind. Appl*., vol. 2, pp. 154-167, 2021.

[32] L. Wang, T. Han, J. He, and T. Zhao, "Model predictive control with secondary objective functions for power module loss reduction," in *Proc. IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, USA, 2019, pp. 225–231.

[33] H. Liu and T. Zhao, "Optimal Gate Driving Strategy for Si/SiC Hybrid Switch-Based 3L-ANPC Inverter with Improved Output Capacity," in *Proc. IEEE Appl. Power Electron. Conf*., 2021, pp. 741-746.

[34] X. Song, L. Zhang and A. Q. Huang, "Three-Terminal Si/SiC Hybrid Switch," *IEEE Trans Power Electron*., vol. 35, no. 9, pp. 8867-8871, Sept. 2020.

[35] Y. Fu, Z. Ma and H. Ren, "A Low Cost Compact SiC/Si Hybrid Switch Gate Driver Circuit for Commonly Used Triggering Patterns," *IEEE Trans Power Electron.*, vol. 37, no. 5, pp. 5212-5223, May 2022.