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Performance Evaluation of Split Output Converters with SiC MOSFETs and SiC Schottky Diodes

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***Abstract*—The adoption of silicon carbide (SiC) MOSFETs and SiC Schottky diodes in power converters promises a further improvement of the attainable power density and system efficiency, while it is restricted by several issues caused by the ultra-fast switching, such as phase-leg shoot-through ('crosstalk' effect), high turn-on losses, electromagnetic interference (EMI), etc. This paper presents a split output converter which can overcome the limitations of the standard two-level voltage source converters when employing the fast-switching SiC devices. A mathematical model of the split output converter has been proposed to reveal how the split inductors can mitigate the crosstalk effect caused by the high switching speed. The improved switching performance (e.g. lower turn-on losses) and EMI benefit have been demonstrated experimentally. The current freewheeling problem, the current pulses and voltage spikes of the split inductors, and the disappeared synchronous rectification are explained in detail both experimentally and analytically. The results show that, the split output converter can have lower power device losses compared with the standard two-level converter at high switching frequencies. However, the extra losses in the split inductors may impair the efficiency of the split output converter, which is verified by experiments in the continuous operating mode. A 95.91% efficiency has been achieved by the split output converter at the switching frequency of 100kHz with suppressed crosstalk, lower turn-on losses, and reduced EMI.**

***Index Terms*—Silicon carbide (SiC), split output converters, crosstalk, efficiency, electromagnetic interference (EMI).**

I. Introduction

Silicon carbide (SiC) is superior to silicon (Si) with wider bandgap, greater electric-breakdown field strength, and higher thermal conductivity. Compared with Si devices, the SiC counterparts can block higher voltage, achieve higher power density, and promise a further improvement of the attainable system efficiency [1], [2].

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The SiC MOSFETs have no tail current during switching, which characterizes the switching of Si IGBTs, resulting in the faster switching speed and dramatically reduced switching losses. The adoption of SiC MOSFETs enables the converters to operate at higher switching frequencies with reduced size and weight of the passive filters. However, the converters with high switching speed are more susceptible to the parasitic elements of the power circuits, e.g. the parasitic inductance of printed circuit board (PCB) traces and the parasitic capacitance of switching devices [3]. High *dv*/*dt* caused by the high switching speed can intensify the interaction between the two complementary SiC MOSFETs of the same phase leg (crosstalk [4]), inducing spurious gate voltage which may lead to the shoot-through failure of the converters. Besides, the high *dv*/*dt* and *di*/*dt* will bring more serious electromagnetic interference (EMI) problem [5]. Another issue for the adoption of SiC MOSFETs is that, the intrinsic body diode of the SiC MOSFET tends to have relatively higher forward voltage drops and larger reverse-recovery losses compared to the purpose-designed diode. Anti-paralleling a better performance SiC Schottky diode is preferred in some applications [6]. However, even if the anti-parallel SiC Schottky diode features zero reverse recovery current, its output capacitance can still increase the total parallel capacitance of SiC MOSFETs contributing to the turn-on losses [3].

The split output converters [7]–[9], which are also known as the dual-buck converters [10]–[14], can transcend the above limitations of the standard two-level converters by adding auxiliary inductors to decouple the upper SiC MOSFET and the lower SiC MOSFET of the same phase leg, as shown in Fig. 1. Q_1~Q_6 are SiC MOSFETs and D_1~D_6 are SiC Schottky diodes; L_{load} is the load/filtering inductor. For the sake of clear description, the auxiliary inductors in split output converters, e.g. L_{s1} and L_{s4} in Fig. 1, are called the 'split inductors'. With different modulation strategies, there can be two operation modes in the split output converter according to the features without or with the synchronous rectification [10], [11]. Taking the case where the current flows out of Phase C for example, without the synchronous rectification, the current flowing path will alternate between the channel of the upper SiC MOSFET Q_5 and the lower SiC Schottky diode D_2; with the synchronous rectification (by turning Q_2 on), the current flowing path will alternate between the channel of the upper SiC MOSFET Q_5 and the lower SiC Schottky diode D_2 in parallel with the channel of the lower SiC MOSFET Q_2.

As seen in Fig. 1, the split inductors separate the upper SiC MOSFET from the lower SiC MOSFET, as well as the SiC MOSFET from its anti-parallel SiC Schottky diode (e.g. Q_1 and D_1), while the commutation loop remains low inductive to guarantee the fast switching speed. Consequently, with the split inductors the crosstalk effect will be suppressed with lower induced spurious gate voltage avoiding the shoot-through failure. The charging current of the output capacitance and the

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reverse recovery current of the body diode will be both attenuated by the split inductors resulting in lower turn-on losses of the SiC MOSFET. In addition, if regarding the nodes O_a, O_b, and O_c in Fig. 1 as the outputs of the converter, the *dv/dt* of the output voltage will also be suppressed with mitigated EMI.

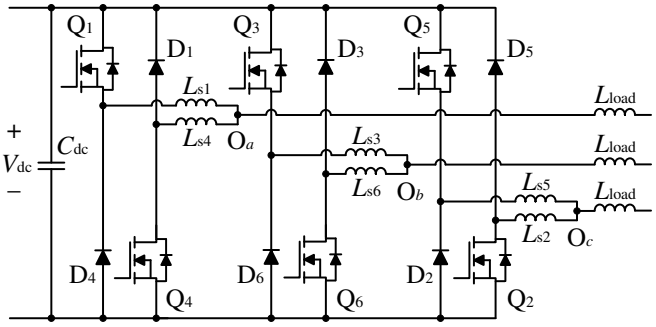


Fig. 1. Three-phase split output converter.

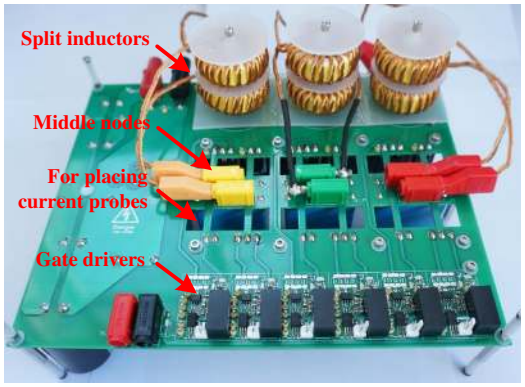
Regarding the study of the converters based on the split output topology, there have been several publications focusing on the modulation [10], [11], control [12], and extension for specific topologies, e.g. the three-level converters [13] and the cascade converters [14]. Meanwhile, for the high-switching-frequency applications based on wide bandgap power devices, the advantages of the split output converter have been generally described in [7]. The current commutation mechanism in the split output converter has been analyzed in [8]. And in [9], the additional challenges, e.g. the current pulses and voltage spikes of split inductors, have been presented. However, there is a lack of systematic and conclusive investigation into the split output converters regarding the crosstalk effect, the switching performance, EMI, and the specific issues of the split output converters, which should be concerned in high-switching-frequency applications.

This paper therefore aims to investigate the split output converter both experimentally and analytically and to reveal the advantages, disadvantages, and challenges of the split output converter in high-switching-frequency applications. The remaining parts of this paper are structured as follows. In Section II, the designed three-phase split output converter and the measurement equipment are described. A mathematical model of the split output converter is proposed in Section III, to reveal how the value of the split inductors affects the crosstalk caused by the high switching speed. In section IV, the improved switching performance and EMI benefits in the split output converter are verified by the captured switching transients. In addition, the current freewheeling problem, the current pulses and voltage spikes of split inductors, and the disappeared synchronous rectification, which can together increase the converter losses, are investigated in Section V. Based on the measured switching losses and the conduction characteristics from datasheets, the power device losses without and with split inductors are calculated in Section VI. The theoretical results from calculation indicate that, the split output converter can have lower power device losses at high switching frequencies compared with the standard two-level converter. However, the experimental results of continuous operating mode in Section VII show that, the efficiency of the split output converter is impaired by the additional split inductor losses. Lastly in Section VIII, the advantages, disadvantages, and challenges of the split output converter are concluded on the basis of the study in this paper.

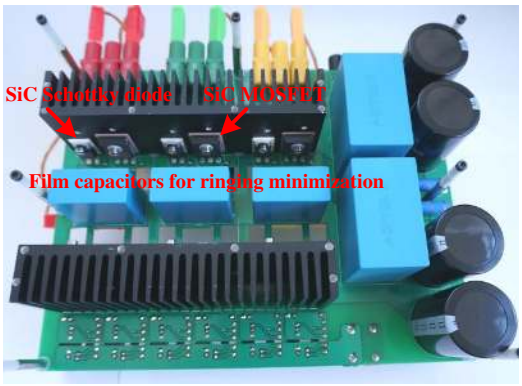
II. Designed Split Output Converter and Measurement Equipment

A three-phase split output converter is designed with the scheme in Fig. 1 for the experimental study of this paper. The top view and bottom view of the designed converter are shown in Fig. 2. The dc-link voltage is designed as 600V, and the rated ac line voltage is 380V (RMS). The SiC MOSFET C2M0080120D (20A, 1200V, 80mΩ) and the SiC Schottky diode C4D20120A (20A, 1200V) both from Cree are used. With 20% margin of the device rated current, the rated ac current of the converter is about 11A (RMS) with a rated capacity of 7.5kVA.

Regarding the measurement equipment, a 350MHz bandwidth 10:1 passive voltage probe with a short ground lead is used for the gate voltage measurement. A differential voltage probe from Agilent Technologies (N2790A, 100MHz) is employed to measure the switching voltage. Given the non-galvanic isolation of the coaxial shunt and the low bandwidth of Rogowski coil [15], the split core current probe also from Agilent Technologies (N2783A, 100MHz, 30A) is adopted for the current measurement.



(a)



(b)

Fig. 2. The designed three-phase split output converter: (a) top view and (b) bottom view.

There is a tradeoff between the convenience of the current measurement and the low parasitic inductance of the switching path. Square holes, as shown in Fig. 2(a), are designed on the board for placing the current probes. While leaving enough space for placing the current probes, the switching path is designed with minimal length and on both sides of the PCB, to minimize the parasitic inductance. The parasitic inductance of the switching path between the upper and the lower power devices is measured as 40.8nH by the Wayne Kerr 65120B Precision Impedance Analyzer. The dc-link film capacitors shown in Fig. 2(b) are mounted closely to the switching devices

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for suppressing the current/voltage ringing generated by the high speed switching [16]. In addition, the middle nodes shown in Fig. 2(a) are used to connect the split inductors of various values according to the requirements. The output voltage of the gate driver IXDN609SI is designed as -5V/+20V. The negative low-state gate voltage (-5V) is used to provide the margin of preventing the potential shoot-through failure caused by the induced spurious gate voltage. The high-state gate voltage should be as high as possible while within the maximum rated gate voltage, to minimize the conduction losses of SiC MOSFETs [17], and +20V is selected.

III. Crosstalk Analysis Based on a Proposed Mathematical Model of the Split Output Converter

In this section, a mathematical model of the split output converter is proposed to analyze the crosstalk effect. How the split inductance and the gate resistance influence the induced spurious gate voltage and the current overshoot at the turn-on transient will be analyzed using this model. To simplify the analysis of the model, the parasitic inductance of the power circuits is neglected, and only the split inductance and the parasitic capacitance of the devices are considered. The load capacitance is not analyzed here, though it can be added to the model if required. Taking Phase C of the split output converter for example, the circuit which can be used to analyze the Q_5 turn-on transient is shown in Fig. 3(a). The parameters of the circuit are given in Table I. Note that, all the parameters except R_{g_ex} and V_{dc} in Table I are obtained from datasheets, and the highly-nonlinear parasitic capacitances in Table I are obtained from datasheets at the voltage of 600V, which equals to the dc-link voltage of the proposed model. The voltage source V_s in Fig. 3(a) represents the voltage at the middle node M of the left phase leg when Q_5 turns on. The influence of V_s on the right phase leg with different split inductances and gate resistances will be analyzed in the following.

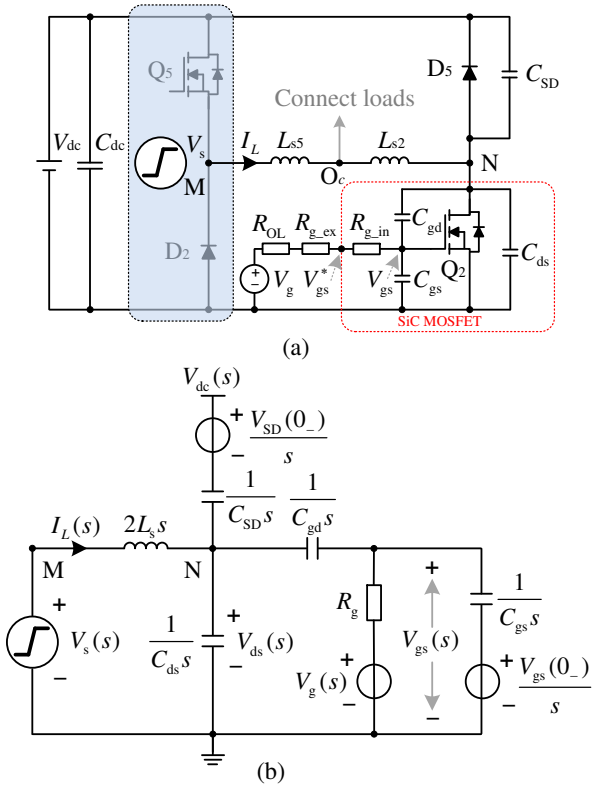

Fig. 3. Mathematical model of the split output converter: (a) circuit for the analysis of Q_5 turn-on transient and (b) equivalent circuit in s domain.

TABLE I
Parameters of the Mathematical Model

Symbol	Parameter	Value
C_{SD}	Parasitic capacitance of SiC Schottky diode	80pF
C_{gd}	Miller capacitance of SiC MOSFET	6.5pF
C_{gs}	Gate to source capacitance of SiC MOSFET	943.5pF
C_{ds}	Drain to source capacitance of SiC MOSFET	73.5pF
R_{g_in}	Internal gate resistance of SiC MOSFET	4.6Ω
R_{OL}	Low-state output resistance of the gate driver	0.4Ω
R_{g_ex}	External gate resistance	Optional
V_{dc}	DC-link voltage	600V

The equivalent circuit of the split output converter in s (frequency) domain is shown in Fig. 3(b), where R_g is the total gate resistance (R_g=R_{OL}+R_{g_ex}+R_{g_in}); L_s refers to the split inductance, L_s=L_{s5}=L_{s2}; $V_{SD}(0\_)$ and $V_{gs}(0\_)$ are the initial voltage on C_{SD} and C_{gs}, $V_{SD}(0\_)$=V_{dc}, $V_{gs}(0\_)$=V_{gL} (V_{gL} is the low-state gate voltage). The initial voltages on C_{gd} and C_{ds} can be neglected compared to the voltages after they are fully charged (both approximately equal to the dc-link voltage after fully charged). To simplify the calculation, the piecewise voltage source $V_s(s)$ [18] is idealized as a step function. With the node-voltage method, selecting $V_{gs}(s)$ and $V_{ds}(s)$ as the node voltages, the circuit shown in Fig. 3(b) can be described as

$$\begin{cases} -C_{gd}sV_{ds}(s)+\left(C_{gd}s+\dfrac{1}{R_g}+C_{gs}s\right)V_{gs}(s) \\ \qquad =\dfrac{1}{R_g}V_g(s)+\dfrac{V_{gs}(0\_)}{s}C_{gs}s \\ \left(\dfrac{1}{2L_s s}+C_{ds}s+C_{gd}s+C_{SD}s\right)V_{ds}(s)-C_{gd}sV_{gs}(s) \\ \qquad =\dfrac{1}{2L_s s}V_s(s)+\left[V_{dc}(s)-\dfrac{V_{SD}(0\_)}{s}\right]C_{SD}s \end{cases} \tag{1}$$

where $V_g(s)=\dfrac{V_{gL}}{s}$ and $V_s(s)=V_{dc}(s)=\dfrac{V_{dc}}{s}$.

The gate voltage $V_{gs}(s)$ and the drain-source voltage of the SiC MOSFET $V_{ds}(s)$ can be derived from (1) as

$$V_{gs}(s)=\frac{\dfrac{1}{2L_s s}V_s(s)+\left(\dfrac{1}{2L_s s}+C_{ds}s+C_{gd}s+C_{SD}s\right)\left(\dfrac{1}{R_g}+C_{gs}s\right)\dfrac{1}{C_{gd}s}V_g(s)}{\left(\dfrac{1}{2L_s s}+C_{ds}s+C_{gd}s+C_{SD}s\right)\left(C_{gd}s+\dfrac{1}{R_g}+C_{gs}s\right)\dfrac{1}{C_{gd}s}-C_{gd}s}, \tag{2}$$

$$V_{ds}(s)=\frac{1}{C_{gd}s}\left[\left(C_{gd}s+\frac{1}{R_g}+C_{gs}s\right)V_{gs}(s)-\left(\frac{1}{R_g}+C_{gs}s\right)V_g(s)\right]. \tag{3}$$

The current flowing through the split inductors can be expressed as

$$I_L(s)=\frac{V_s(s)-V_{ds}(s)}{2L_s s}. \tag{4}$$

The corresponding time domain values can be obtained by

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the inverse Laplace transform. It should be noted that V^*_{gs} in Fig. 3(a) is different from V_{gs} when the gate drive circuit is in the dynamic state. V^*_{gs} can be derived from V_{gs} using Ohm's law. The value of V^*_{gs} can be measured outside the device to compare with its theoretical value.

As seen in Fig. 3(a), after V_{ds} rises to V_{dc}, the split inductor current I_L will be freewheeled by the diode D_5. At the time of V_{ds} rising to V_{dc}, V^*_{gs} and I_L will reach the maximum value. This time can be calculated by (3). Afterwards, the maximum value $V^*_{gs\_max}$ and I_{L_max} at this time can be obtained from (2) and (4), respectively. $V^*_{gs\_max}$ can be taken as the induced spurious gate voltage. And I_{L_max} can partly represent the current overshoot of the SiC MOSFET at the turn-on transient, due to the parasitic capacitances of D_2 and Q_5 are not taken into account.

The theoretical results using the models in (2)~(4) and the experimental results using the double pulse test (DPT) with varying L_s and R_{g_ex} are shown in Fig. 4. L_s=0 represents the case where no split inductors are used (as in a standard two-level converter). In order to minimize the influence of ringing on the experimental results, the external gate resistance of the switching SiC MOSFET Q_5 is selected as 33Ω which is relatively large, to slow down the switching speed for ringing suppression. The external gate resistance of the lower SiC MOSFET Q_2 is selected as required, e.g. varying from 6.2Ω to 100Ω. The theoretical and experimental results generally agree with each other. Due to some simplifications are made in the proposed model, e.g. the parasitic inductance of the power circuit is neglected and V_s(s) is idealized as a step function, the measured spurious gate voltages and current overshoots have some discrepancies with the theoretical results.

The split inductor currents and the induced spurious gate voltages with L_s=0μH and L_s=10μH (R_{g_ex}=33Ω) are shown in Fig. 5. It should be noted in Fig. 4(a), the discrepancy between the theoretical and experimental results without split inductors (L_s=0μH) is mainly caused by the ringing at the top of the measured current in Fig. 5(a). While the other experimental results in Fig. 4(a) with split inductors match well with the theoretical results, due to no ringing in the measured current with split inductors as seen in Fig. 5(b).

As seen in Fig. 4(a) and Fig. 4(b), the current overshoot I_{L_max} and the induced spurious gate voltage $V^*_{gs\_max}$ are gradually reduced with the increasing split inductance. The phenomena can be simply explained as follows. Without the split inductors, V_s will directly charge C_{ds} and C_{gd}, discharge C_{SD}, causing the large current overshoot, and the charge of the Miller capacitor C_{gd} will induce the high spurious gate voltage. After the split inductors are added, the charging/discharging processes of C_{ds}, C_{gd}, and C_{SD} are buffered with smaller current overshoot and lower spurious gate voltage. Meanwhile, as seen in Fig. 4(c), $V^*_{gs\_max}$ increases with the increasing external gate resistance R_{g_ex}, which can be explained based on the generation mechanism of the spurious gate voltage. During the charging process of the Miller capacitor C_{gd}, the charging current will also flow through C_{gs} and the resistance on the gate drive path, as seen in Fig. 3(a). The larger gate resistance will increase the parallel impedance of the gate resistance and C_{gs}, generating higher spurious gate voltage. Note that, even though the larger gate resistance can slow down the switching speed with reduced the spurious gate voltage, the increased spurious gate voltage as analyzed above can outweigh the reduced spurious gate voltage, making the spurious gate voltage increase with the increasing gate resistance.

It should be also noted that, even if the low-state gate voltage is selected as -5V in this paper, the spurious gate voltage with a large external gate resistance and no split inductors can still be close to the gate threshold voltage of the SiC MOSFET ($V_{gs(th)}$ =1.7V for C2M0080120D). In contrast, the split inductors can effectively suppress the crosstalk with reduced spurious gate voltage preventing the potential shoot-through failure. The proposed model can be used as a reference for the selection of the external gate resistance and the split inductance.

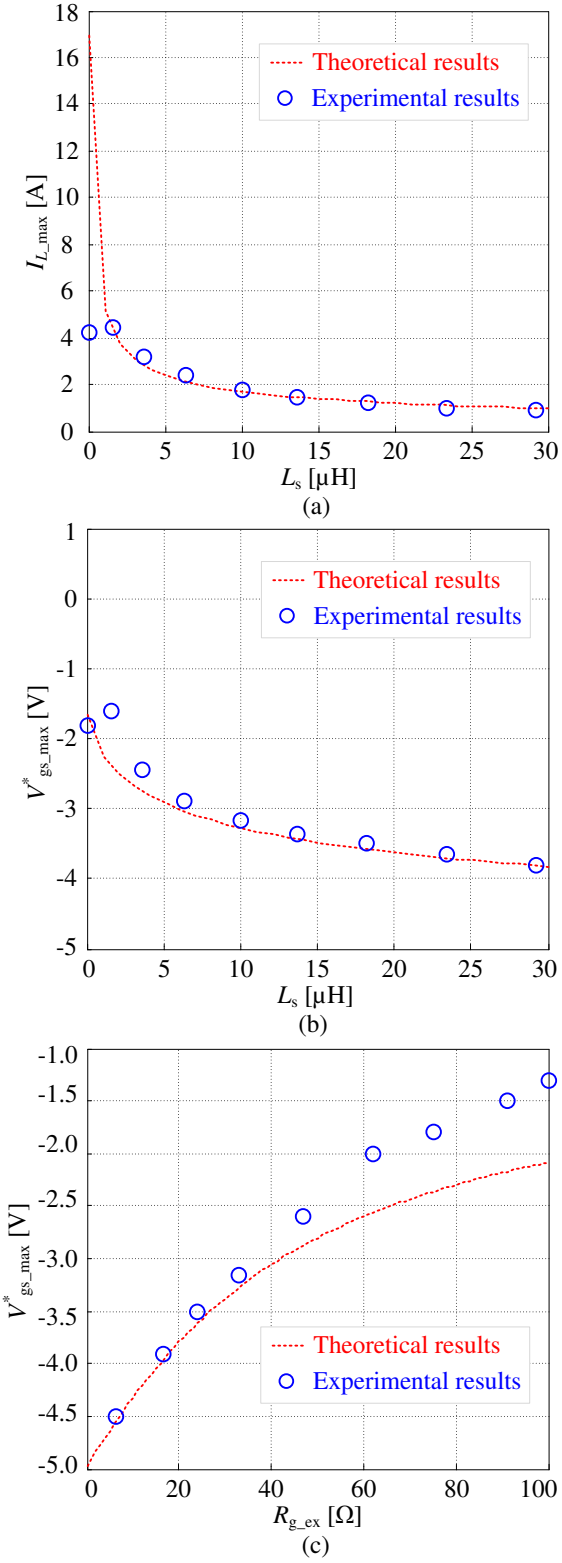

Fig. 4. Theoretical results from the proposed model and experimental results: (a) I_{L_max} with varying L_s (R_{g_ex}=33Ω), (b) $V^*_{gs\_max}$ with varying L_s (R_{g_ex}=33Ω), and (c) $V^*_{gs\_max}$ with varying R_{g_ex} (L_s=10μH).

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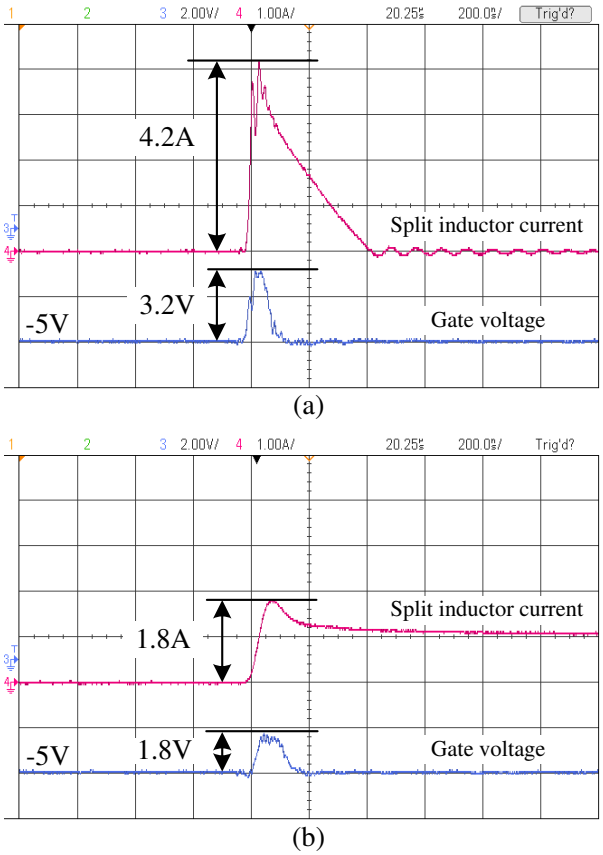

Fig. 5. The split inductor currents and the induced spurious gate voltages (R_{g_ex}=33Ω): (a) L_s=0μH and (b) L_s=10μH.

IV. Improved Switching Performance and EMI Benefit of the Split Output Converter

A. Influence of Split Inductors on Switching Performance

In the switching performance test, a relatively small external gate resistor of 6.2Ω is adopted to achieve the fast switching speed. And the split inductors of 10μH are employed. It is considered that, the DPT with an optimally designed load inductor may not sufficiently represent a more complex configuration of actual converters and loads, e.g. the SiC-based inverter for induction motor drives, where the power cable and induction motor have large parasitic capacitances and other parasitic elements [19]. Therefore, a load inductor of 6.2mH with relatively large parasitic capacitance is selected for the DPT, trying to mimic the practical applications. With the probe delays ('skew') compensated by the oscilloscope, the waveforms at turn-on and turn-off transients are captured respectively without and with split inductors, as show in Fig. 6.

Comparing Fig. 6(a) and Fig. 6(c), with the split inductors adopted, the current overshoot at the turn-on transient is reduced from 11A to 3A, and the low-frequency current ringing during the turn-on transient is suppressed. Comparing Fig. 6(b) with Fig. 6(d), the current and voltage distortions at the turn-off transient are smoothed by the split inductors. However, the split inductors have little influence on the high-frequency ringing of the current and voltage at both turn-on and turn-off transients. In addition, the turn-on energy is reduced from 920μJ to 725μJ by 195μJ, while the turn-off energy is increased from 100μJ to 180μJ by 80μJ.

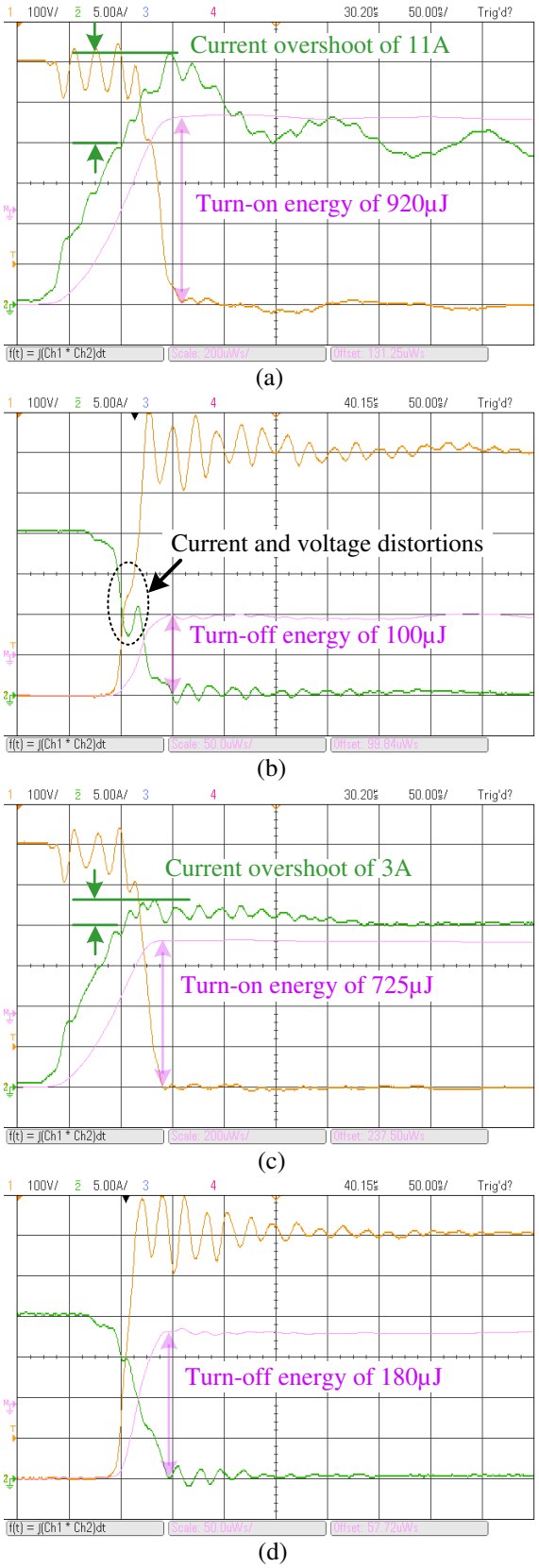

Fig. 6. Switching waveforms with conduction current of 20A and R_{g_ex} of 6.2Ω: (a) turn-on transient and (b) turn-off transient without split inductors, (c) turn-on transient and (d) turn-off transient with split inductors of 10μH.

In order to explain the phenomena, the circuit of the split output converter for DPT with parasitic elements considered [20] is established as shown in Fig. 7, where L_{px} (x=1, 2, 3 ...) is the parasitic inductance of the circuit; C_{p_L} is the parasitic capacitance of the load inductor; C_{oss} is the output capacitance

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of the SiC MOSFET, $C_{oss}=C_{ds}+C_{gd}$. The parasitic capacitances of the load inductor and the split inductor are measured by Wayne Kerr 65120B Precision Impedance Analyzer. The parasitic capacitance of the load inductor is 122.6pF, which is comparable with that of the devices, while the split inductor has a negligible parasitic capacitance of 2.1pF.

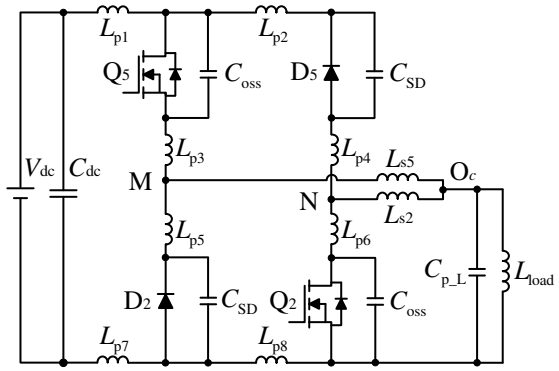

Fig. 7. Circuit of the split output converter for DPT with parasitic elements considered.

As seen in Fig. 7, the split inductors separate the switching MOSFET Q_5 from the parasitic capacitances of D_5, Q_2, and the load. The total parallel capacitance of Q_5 is dramatically reduced due to the addition of the split inductors. The split inductors can effectively buffer the charge and discharge of the parasitic capacitors resulting in the reduced current overshoot in Fig. 6(c). In addition, the results of the mathematical model in Section III have also shown the capability of the split output converter to suppress the turn-on current overshoot.

Regarding the reverse recovery current in the body diode of the SiC MOSFET which can also cause the current overshoot in the complementary SiC MOSFET [20], due to the voltage drop of the SiC Shottky diode is lower than that of the body diode of the SiC MOSFET, no current or only small current will flow through the body diode, as further detailed in Section V-D. Consequently, the reverse recovery current of the body diode can be neglected in the designed split output converter. Note that, even if a large current flows through the body diode of the SiC MOSFET generating significant reverse recovery current in the switching process, e.g. using the lower current-rating Schottky diode with higher voltage drop, the split inductors are also able to buffer this part of reverse recovery current to reduce the current overshoot at turn-on transient.

At the turn-off transient of Q_5, the voltage change at M and N nodes will cause the charge and discharge of the capacitors. The current and voltage distortions shown in Fig. 6(b) are generated by the ringing in the charging/discharging processes [3]. Given the charging/discharging processes in the right phase leg and the load are buffered by the split inductors, the current and voltage distortions at the turn-off transient are suppressed, as shown in Fig. 6(d).

The low-frequency ringing in Fig. 6(a) is generated by the interaction between the parasitic inductance and the large parasitic capacitance in the right phase leg and the load. While the high-frequency ringing is caused by the parasitic inductance and the relatively small parasitic capacitance of the left phase leg. As seen in Fig. 7, the split inductors can block the charge/discharge of the parasitic capacitance in the right phase leg and the load, however, have no influence on the charge/discharge of the parasitic capacitance in the left phase leg. Therefore, the low-frequency ringing is effectively suppressed, but the high-frequency ringing cannot be affected.

Due to the fact that capacitors can slow down the voltage changing speed, after adding the split inductors, the reduced parallel capacitance of the SiC MOSFET enables the switching voltage to rise or fall faster, while the current changing speeds at the turn-on and turn-off transients both remain almost the same. This can be seen by comparing Fig. 6(a) with Fig. 6(c), and Fig. 6(b) with Fig. 6(d), respectively. Therefore, the current and voltage overlap area at the turn-on transient will be reduced with smaller turn-on energy, and the current and voltage overlap area at the turn-off transient will be increased resulting in larger turn-off energy. During turn-on, there is significant current overshoot. With the faster voltage changing speed, the turn-on energy will be reduced significantly, which is higher than the increased turn-off energy, thus leading to an overall reduced switching energy.

To further illustrate the influence of the split inductors on switching energies, the turn-on, turn-off, and total switching energies are measured in experiments using various split inductor values with conduction currents of 10A and 20A, respectively, as plotted in Fig. 8. As seen, as the split inductance increases, with both low and high conduction currents, the turn-off energies will gradually increase, while the turn-on energies and the total switching energies will gradually decrease. It should be noted that, there is little influence of split inductors on the switching energies as the split inductance is larger than about 10μH.

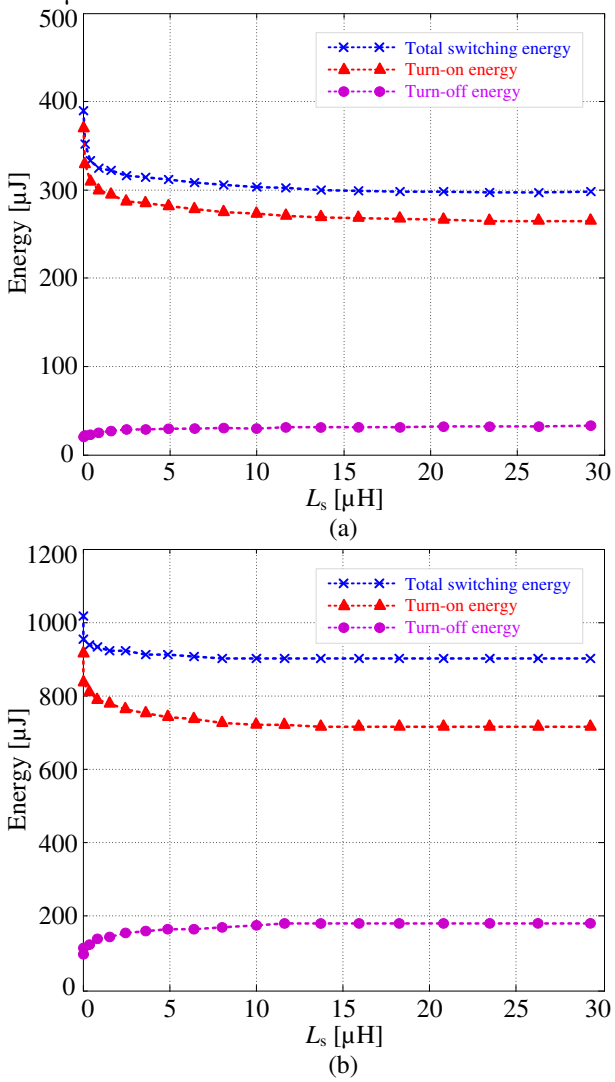

Fig. 8. Turn-on, turn-off, and total switching energies: (a) with conduction current of 10A and (b) with conduction current of 20A.

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B. EMI Benefit of the Split Output Converter

The voltage at the O_c node in Fig. 7, which can be treated as the output voltage of the split output converter, is measured with and without split inductors, as shown in Fig. 9. Comparing Fig. 9(a) with Fig. 9(b), after applying the split inductors, the *dv*/*dt* at the rising and falling edges are reduced from 11.765kV/μs and 19.335kV/μs to 3.529kV/μs and 5.455kV/μs, respectively. And the voltage overshoot and undershoot, as well as the ringing of about 7MHz shown in Fig. 9(a) are effectively suppressed. These improvements in the output voltage of the split output converter can together lead to the EMI reduction. For motor drive applications, the split output converter can relieve the high-frequency voltage stresses on the winding insulation systems [21].

The reduced *dv*/*dt* of the output voltage in the split output converter can be analyzed as follows. Given the split inductors can effectively buffer the charge and discharge of the parasitic capacitors, significant voltage drops (L_s·*di*/*dt*) will be generated on the split inductors, forming the voltage spikes shown later in Fig. 13. Consequently, the *dv*/*dt* of the output voltage in the split output converter is reduced by the significant voltage drops on the split inductors compared to the standard two-level converter without split inductors.

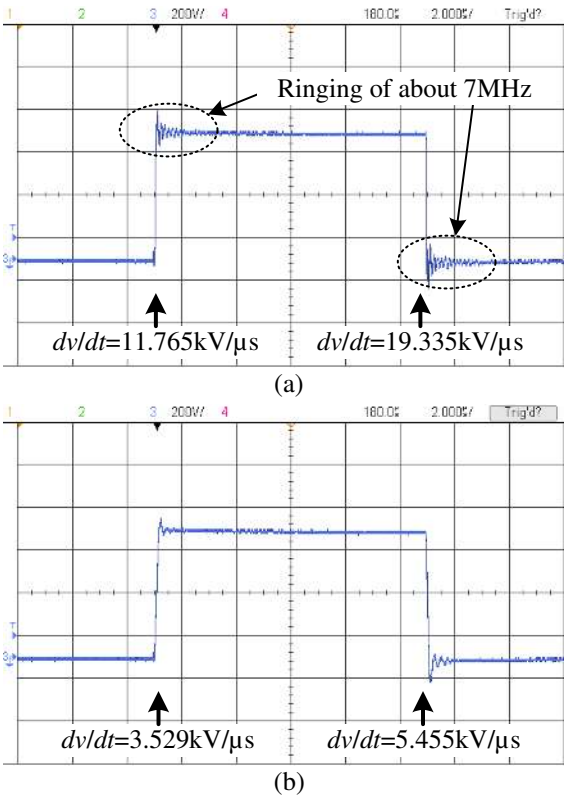

Fig. 9. Output voltage waveforms: (a) without split inductors and (b) with split inductors of 10μH.

The spectra of the output voltages are computed for EMI generation analysis. In the measurement, the employed Agilent Technologies MSO-X 3014A oscilloscope has a bandwidth of 100MHz and 4GSa/s maximum sampling rate. The probe for the voltage measurement (Agilent Technologies, N2790A) has the same bandwidth of 100MHz, which should be sufficient for the required measurement bandwidth. However, for a 'single-shot' measurement, the useful measurement bandwidth can be reduced by the large noise floor [22]. Therefore, in order to extend the useful measurement bandwidth, the double pulse test is repeated 100 times, and the captured 100 output voltage waveforms are synthesized into one signal to average the random noises. Then, the voltage spectra are computed by Discrete Fourier Transform (DFT). Fig. 10 shows the magnitude spectra of the output voltages without and with split inductors, which can clearly show the EMI benefit of the split output converter. As seen, the spectral amplitude between 3MHz and 25MHz is effectively reduced by the split inductors. Specifically, the reduced spectra magnitude around 7MHz can represent the suppressed ringing of about 7MHz in Fig. 9.

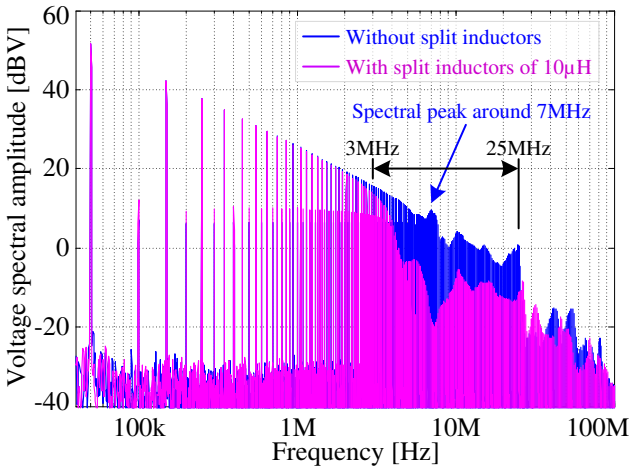

Fig. 10. Magnitude spectra of the output voltages without and with the split inductors of 10μH.

V. Several Issues of the Split Output Converter

Apart from the above benefits of the split output converter, there are also several issues brought by the split inductors [8], [9]. These issues need to be well addressed for the application of the split output converter.

A. Current Freewheeling caused by Split Inductors

An issue of the split output converter is the current freewheeling caused by the split inductors [8]. The following analysis will be based on the switching process of the SiC MOSFET Q_5 illustrated in Fig. 11, where the parasitic inductance of the circuit is not shown to make the figure clear. As seen in Fig. 11(a), at the turn-on transient of Q_5, the parasitic capacitances of D_5 and Q_2 will be discharged and charged, respectively. Once the discharging and charging processes are finished, the current will be freewheeled by L_{s2} and D_5, forming a current freewheeling loop in L_{s2}, D_5, Q_5, and L_{s5} until the energy stored in L_{s2} is gradually dissipated, as illustrated in Fig. 11(b). The similar phenomenon happens at the turn-off transient as well, the charging/discharging current will be freewheeled by L_{s2} and the body diode of Q_2, as seen in Fig. 11(c) and Fig. 11(d).

Fig. 12 experimentally shows the charging, discharging, and freewheeling currents without and with split inductors, which are measured by the current probes located at the dashed ellipses in Fig. 11. As seen in Fig. 12(a), without the spilt inductors, the charging/discharging peak currents are large with short falling edges. In Fig. 12(b), after adding the split inductors, the charging/discharging peak currents are effectively suppressed, while the falling edges caused by the current freewheeling become much longer, which may cause extra potential conduction losses in the SiC Schottky diode and the body diode of the SiC MOSFET.

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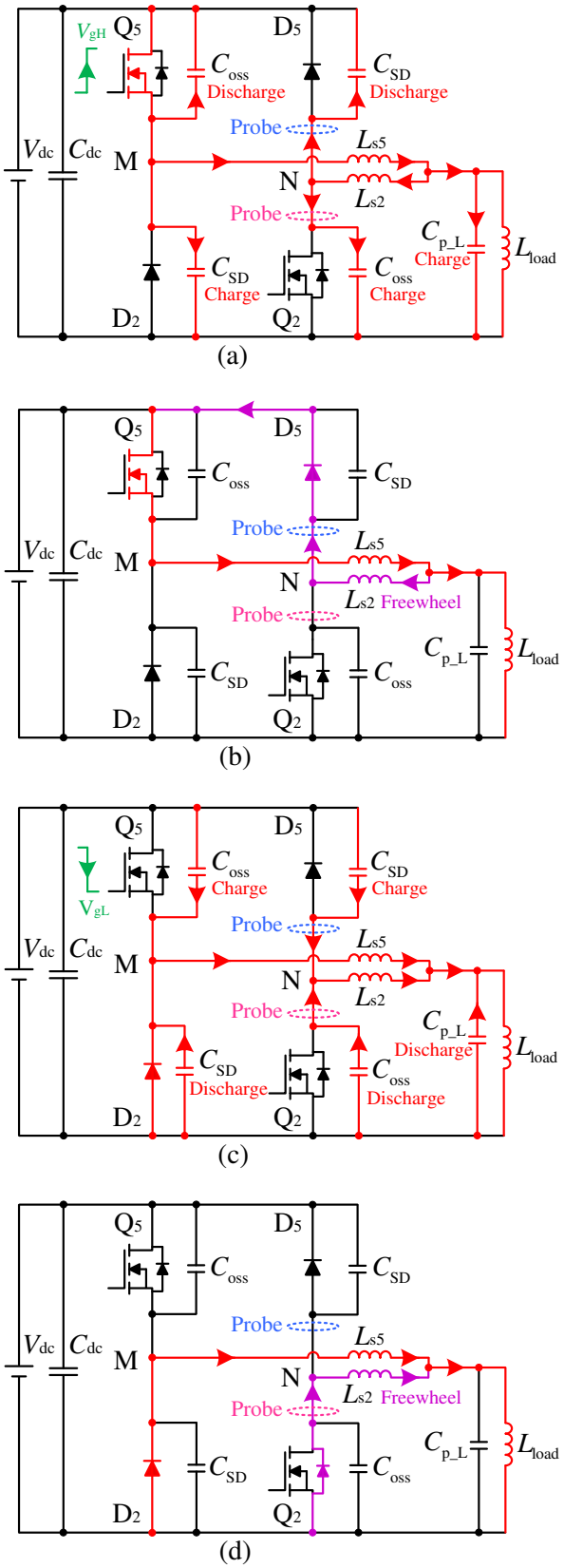

Fig. 11. Analysis of the current freewheeling caused by split inductors: (a) capacitor charging and discharging at the turn-on transient of Q_5, (b) current freewheeling after the turn-on transient of Q_5, (c) capacitor charging and discharging at the turn-off transient of Q_5, and (d) current freewheeling after the turn-off transient of Q_5.

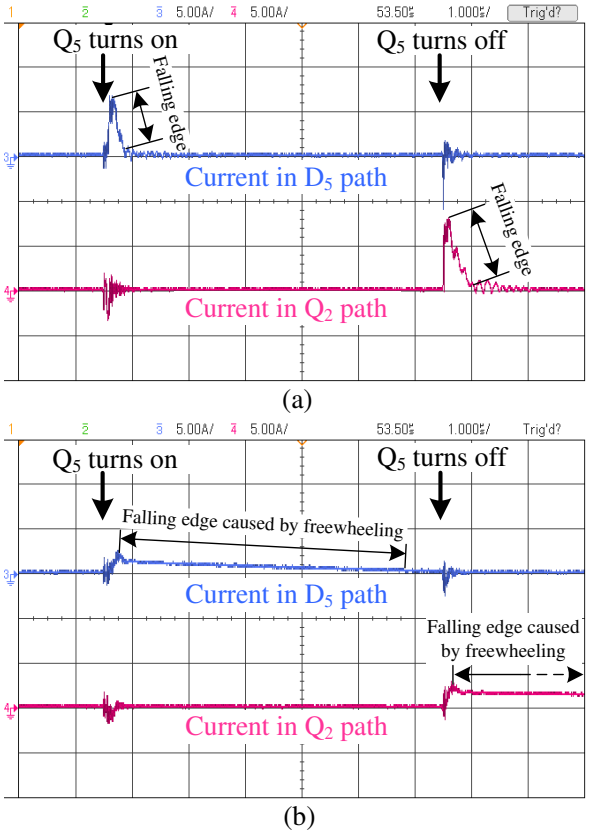

Fig. 12. The charging, discharging, and freewheeling currents: (a) without split inductors and (b) with split inductors of 10μH.

B. Current Pulses and Voltage Spikes of the Split Inductors

The measured current pulses and voltage spikes of the split inductors [9] are given in Fig. 13, where the voltage spikes are measured between the middle nodes of the phase leg, i.e. the M and N nodes in Fig. 11.

The current pulses of the split inductors can also be explained by the switching process illustrated in Fig. 11. When the circuit is switched from Fig. 11(b) to Fig. 11(c), or switched from Fig. 11(d) to Fig. 11(a), the current in L_{s2} (i_{Ls2}) will change direction, generating the current pulses in L_{s2}. Assuming the load current (i_{load}) is constant in the switching process, the current pulses in L_{s2} will also make the current in L_{s5} (i_{Ls5}) oscillate. In addition, regarding the switching transient of the SiC MOSFET, it is always associated with the charge/discharge of the parasitic capacitance. Given the split inductors can buffer the charging/discharging currents, significant voltage drops (voltage spikes) will be generated on the split inductors at the switching transients. And also owing to the voltage drops on the split inductors, the split output converter can have the EMI benefit mentioned in Section IV-B.

The value of the split inductance can affect the current pulses and voltage spikes, which can be seen by comparing Fig. 13(a) with Fig. 13(b). As the split inductance decreases, the amplitude of current pulses will become larger, and the width of the voltage spikes will become narrower. In addition, the frequency of the current pulses and voltage spikes is the same with the switching frequency. Significant losses will be generated in the split inductors at high switching frequencies due to the the current pulses and voltage spikes, which may affect the system efficiency.

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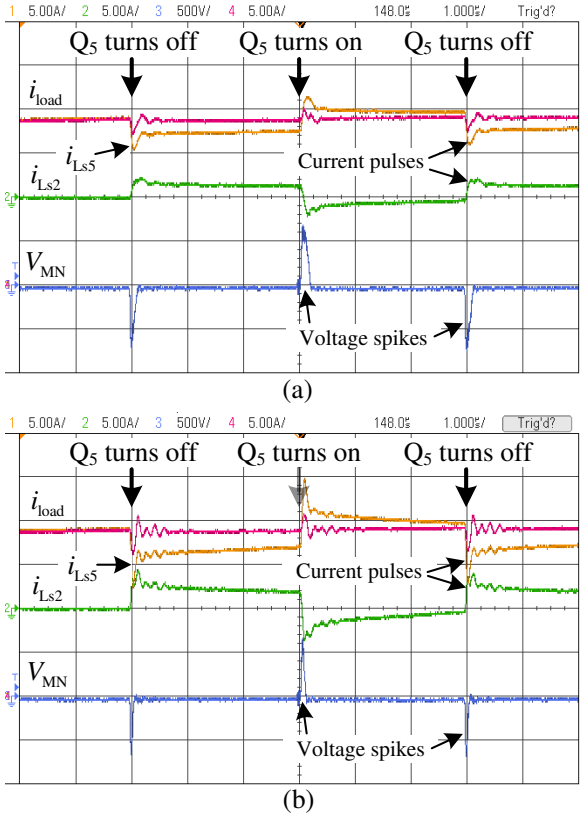

Fig. 13. Current pulses and voltage spikes of the split inductors with split inductance of (a) 10μH and (b) 2.5μH.

C. Influence of the Split Inductors on Synchronous Rectification

The synchronous rectification has been widely used to improve the converter efficiency, which incorporates the MOSFET channel in the current freewheeling path as a bypass of the freewheeling diode [23]. In this section, how the split inductors influence the synchronous rectification in the split output converter is analyzed. The synchronous rectification is tested with and without the split inductors, the currents flowing through D_2 and Q_2 are measured and divided into three parts for clear descriptions, as shown in Fig. 14. In Part 1 and Part 3, Q_5 and Q_2 are both in off state, the freewheeling current will not flow through the channel of the SiC MOSFET. In Part 2, Q_5 is off while Q_2 is on, the circuit is in synchronous rectification mode.

Fig. 14(a) shows the experimental results without split inductors. As seen in Part 2 of Fig. 14(a), when Q_2 turns on, the current freewheeled by the SiC Schottky diode D_2 is partly switched to the channel of the SiC MOSFET Q_2, making the circuit in the synchronous rectification mode. Meanwhile, Fig. 14(b) shows the results with split inductors of 10μH, the current of Q_2 in Part 2 has become very small, making the synchronous rectification mode almost disappeared.

The reason why the synchronous rectification is affected by the split inductors can be given as follows. After Q_2 turns on, the circuit is in synchronous rectification mode, where the current flowing through D_2 will fall while the current flowing through the channel of Q_2 will rise. At this time, the electromotive forces of the synchronous rectification path can be illustrated in Fig. 15. The falling current in the D_2 path will generate a forward-electromotive force V_{Ls5} on L_{s5}, which will counteract the falling current in the D_2 path. Meanwhile, the rising current in the Q_2 path will generate a counter-electromotive force V_{Ls2} on L_{s2}, which will be against the rising current in the Q_2 path. How much current flowing through the channel of Q_2 depends on the voltage difference of $V_f - V_{Ls5} - V_{Ls2}$, where V_f is the voltage drop on the SiC Schottky diode D_2. The split inductors associated with the rising and falling currents can generate the comparable electromotive force with V_f, making the synchronous rectification mode susceptible to the value of the auxiliary split inductors.

The disappeared synchronous rectification in the split output converter makes almost all the freewheeling current flow through the SiC Schottky diode. Given the equivalent on-state resistance of the SiC Schottky diode in parallel with the channel of the SiC MOSFET is smaller than that of a single SiC Schottky diode, the disappeared synchronous rectification can increase the conduction losses of the converter.

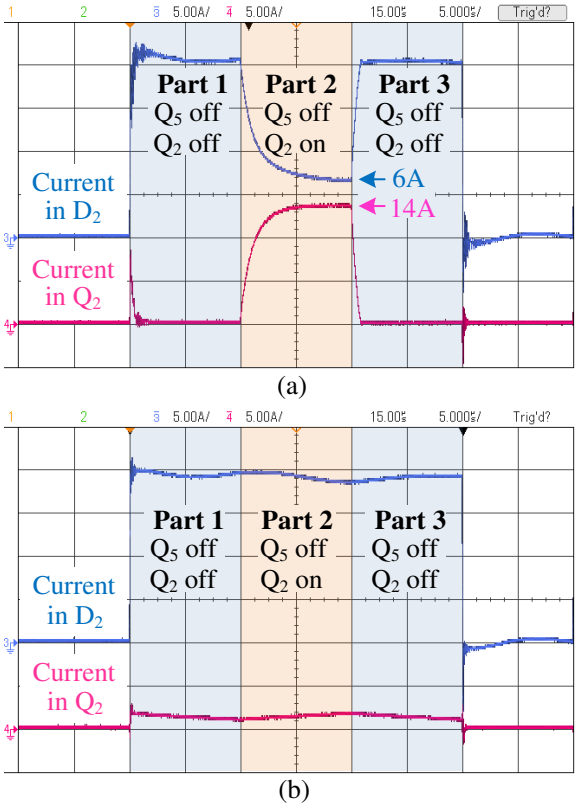

Fig. 14. Synchronous rectification: (a) without split inductors and (b) with split inductors of 10μH.

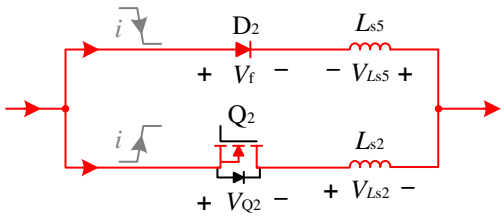

Fig. 15. Electromotive forces of the synchronous rectification path.

D. Current Sharing between the SiC Schottky Diode and the SiC MOSFET

The current sharing between the SiC Schottky diode and the body diode of the SiC MOSFET, as well as the current sharing between the SiC Schottky diode and the channel of the SiC MOSFET will be analyzed in this section.

The current sharing between the SiC Schottky diode and the

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body diode of the SiC MOSFET can be analyzed based on the current waveforms shown Fig. 14(a). As seen in Part 1 and Part 3, when Q_2 is turned off, all the freewheeling current of about 20A flows through D_2, and no current flows through the body diode of Q_2 in steady state. It proves that the voltage drop of the SiC Schottky diode is much lower than that of the body diode of the SiC MOSFET. When the SiC MOSFET is off, the current will only flows through the SiC Schottky diode, and never be shared by the body diode of the SiC MOSFET in steady state, even with the rated current of 20A.

When Q_2 is on, as seen in Part 2 of Fig. 14(a), the current will be shared between the SiC Schottky diode and the channel of the SiC MOSFET, making the circuit in synchronous rectification mode. The current sharing in steady state is determined by the device conduction characteristics shown in Fig. 16. Note that the third quadrant-characteristic of the SiC MOSFET is adopted, since the freewheeling current in synchronous rectification mode flows through the channel of the SiC MOSFET in reverse direction. To work out the exact sharing of the current, the following two conditions should be met: (1) the voltage drops on the SiC Schottky diode and the SiC MOSFET are the same; (2) the sum of the currents flowing through the two devices equals to the total freewheeling current. Intersections are marked in Fig. 16 according to the conditions, the current of 6A flows through the SiC Schottky diode, while the current of 14A flows through the channel of the SiC MOSFET, which agrees with the current sharing shown in Part 2 of Fig. 14(a).

It should be noted that the current sharing between the SiC Schottky diode and the SiC MOSFET is measured and analyzed at room temperature (25°C). Similar conclusions can be drawn by the device characteristics from datasheets at a higher temperature, e.g. 150°C.

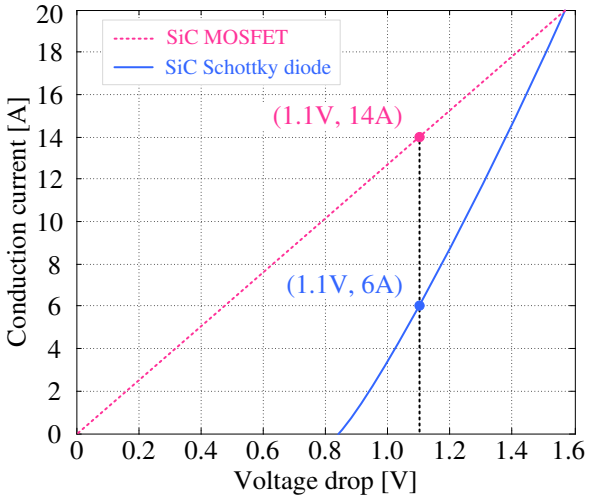

Fig. 16. Typical third quadrant characteristics of the SiC MOSFET C2M0080120D (V_{gs}=20V) and the forward characteristic of the SiC Schottky diode C4D20120A both with junction temperature of 25°C.

VI. Power Device Loss Calculation without and with Split Inductors

A. Power Device Loss Calculation based on SiC MOSFETs

In this section, the total power device losses in the three-phase split output converter are calculated without and with the split inductors, respectively, to reveal the influence of split inductors on the converter efficiency. The conduction losses and the switching losses are considered separately in the calculation.

With the reverse conduction capability of the SiC MOSFET channel, the conduction loss calculation based on SiC MOSFETs is different from that based on IGBTs [24]. The conduction losses can be divided into the forward conduction losses caused by the current flowing forward the SiC MOSFET channel and the freewheeling conduction losses in current freewheeling stage. The forward conduction losses can be calculated based on the forward conduction-characteristic of the SiC MOSFET. However, the freewheeling conduction losses are relatively complicated due to the synchronous rectification, which should be considered respectively without and with split inductors:

1) **Without the split inductors:** The freewheeling current is shared by the SiC MOSFET channel and the SiC Schottky diode. The conduction characteristic of the SiC MOSFET channel in parallel with the SiC Schottky diode is a piecewise function, as seen from the device conduction characteristics at 150°C in Fig. 17. To simplify the calculation, the piecewise conduction characteristic is replaced by a quadratic function obtained by curve fitting, as seen the freewheeling conduction-characteristic function $v_{fre}(i_c)$ without split inductors in Fig. 17, based on which the freewheeling conduction losses without split inductors can be calculated.
2) **With split inductors:** The freewheeling current almost only flows through the SiC Schottky diode, as analyzed in Section V-C. The freewheeling conduction losses with split inductors can be calculated using the characteristics of the SiC Schottky diode, as seen the conduction-characteristic function $v_{fre}(i_c)$ with split inductors in Fig. 17.

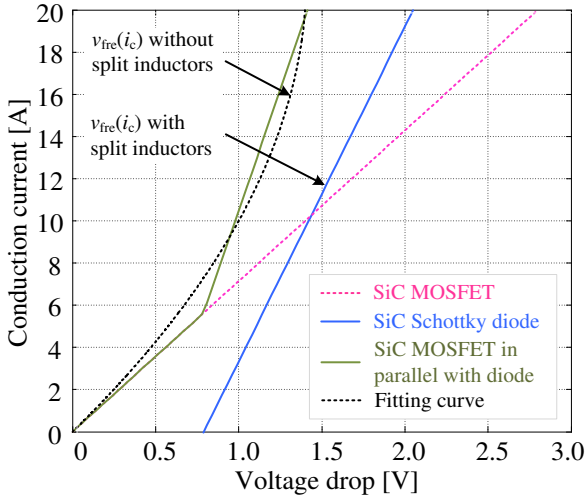

Fig. 17. The device conduction characteristics adopted in the calculation with junction temperature of 150°C.

Various factors, e.g. the gate drivers and power circuit layout, can affect the switching losses of SiC MOSFETs, making it difficult to match the switching losses given in datasheets [25]. Considering the influence of temperature on switching losses is small, the measured switching losses based on the designed circuit at room temperature without and with the split inductors are adopted in the calculation. The switching losses of SiC MOSFETs can be divided into the forward switching losses and the switching losses during the transients alternating between dead time and synchronous rectification. The forward switching loss calculation based on SiC MOSFETs can be the same as that based on IGBTs [24]. While the switching losses of SiC

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MOSFETs during the transients alternating between dead time and synchronous rectification can be neglected, due to the small switching voltage in the process of current communication between the SiC Schottky diode and the SiC MOSFET. In addition, with the adoption of the SiC Schottky diode with zero reverse recovery current, essentially no switching loss is generated by the SiC Schottky diode.

In the calculation, the conventional bipolar sinusoidal pulse width modulation (SPWM) [11] is adopted, and the dead time effect is not taken into account. The average forward and freewheeling conduction losses ($P_{\text{forw\_con}}$ and $P_{\text{fre\_con}}$) over one fundamental cycle can be respectively expressed as

$$P_{\text{forw\_con}} = \frac{1}{2\pi}\cdot\int_0^{\pi}\left[\frac{1+M\sin(\omega t+\varphi)}{2}\cdot v_{\text{forw}}(i_{\text{c}})\cdot I_{\text{cm}}\sin(\omega t)\right]d\omega t \quad (5)$$

$$P_{\text{fre\_con}} = \frac{1}{2\pi}\cdot\int_0^{\pi}\left[\frac{1-M\sin(\omega t+\varphi)}{2}\cdot v_{\text{fre}}(i_{\text{c}})\cdot I_{\text{cm}}\sin(\omega t)\right]d\omega t \quad (6)$$

where M is the modulation index; φ is the power factor angle; ω is the angular frequency; I_{cm} is the amplitude of conduction current i_{c}. $v_{\text{forw}}(i_{\text{c}})$ and $v_{\text{fre}}(i_{\text{c}})$ are the forward and freewheeling conduction-characteristic functions, respectively. $v_{\text{forw}}(i_{\text{c}})$ can be obtained directly from the datasheet of the SiC MOSFET, while $v_{\text{fre}}(i_{\text{c}})$ should be considered respectively without and with split inductors, as shown in Fig. 17.

The experimentally measured switching energies in the designed converter can be modelled as

$$E_{\text{switch}} = \frac{v_{\text{DS}}}{v_{\text{DSN}}}(A_0 + B_0\cdot i_{\text{c}} + C_0\cdot i_{\text{c}}^2) \quad (7)$$

where A_0, B_0, and C_0 are the coefficients of the quadratic function; v_{DSN} is the drain-to-source voltage, at which the switching energies are measured; v_{DS} is the actual drain-to-source voltage [26].

The average (forward) switching losses over one fundamental cycle can be given by

$$P_{\text{switch}} = \frac{f_{\text{s}}}{2\pi}\cdot\frac{v_{\text{DS}}}{v_{\text{DSN}}}\cdot\int_0^{\pi}\left\{A_0 + B_0\cdot I_{\text{cm}}\sin(\omega t) + C_0\cdot\left[I_{\text{cm}}\sin(\omega t)\right]^2\right\}d\omega t \quad (8)$$

where f_{s} is the switching frequency.

In addition, the losses caused by the current freewheeling problem in Section V-A are related to the energy stored in the split inductors, which can been estimated as follows. The freewheeling peak current i_{peak} is about 2A as shown in Fig. 12(b). At the switching frequency f_{s} of 100kHz with split inductors of 10μH, the energy stored in one split inductor can be calculated as $E_{\text{s}}=0.5L_{\text{s}}\cdot i^2_{\text{peak}}=20\mu\text{J}$, the corresponding power loss is $P_{\text{s}}=E_{\text{s}}\cdot f_{\text{s}}=2\text{W}$. And considering there are six split inductors in the three-phase split output converter, if all the calculated split inductor energy is dissipated in the current freewheeling loop shown in Fig. 11(b), this part of losses would be very large compared to the total power device losses. However, in the actual continuous operation of the converter, before the energy totally dissipated, the circuit state may have been changed (e.g. from Fig. 11(b) to Fig. 11(c)). And this is also the reason why there are current pulses in the split inductors as seen in Fig. 13. That is to say, in the continuous operation of the converter, the energy stored in the split inductors will not be totally dissipated in each switching period. Besides, the split inductor losses calculated based on the current pluses in the next section have also partly included the energy stored in the split inductors. The above analysis indicates that, the current freewheeling losses can be overestimated by simply using the energy stored in the split inductors. More detailed study on the current freewheeling losses caused by the split inductors can be the future work on the basis of this paper. This part of losses is therefore not included in the calculated total power device losses.

B. Results of the Power Device Loss Calculation

The total power device losses of the three-phase split output converter are six times the sum of $P_{\text{forw\_con}}$, $P_{\text{fre\_con}}$, and P_{switch}. Taking various factors (I_{cm}, f_{c}, M, and φ) into account, the calculation results without and with the split inductors of 10μH are plotted in Fig. 18. It should be noted that, each subfigure in Fig. 18 is plotted with a single varying variable while the other three variables are constant, which has been detailed in the corresponding captions of the subfigures.

As seen in Fig. 18(a), the total power device losses are directly proportional to the switching frequencies. Since the split inductor can affect the synchronous rectification with increased freewheeling conduction losses, the total power device losses with the split inductors are higher than those without the split inductors at low switching frequencies. However, given the split inductors can reduce the switching losses as analyzed in Section IV-A, as the switching frequency increases, the total power device losses with the split inductors become smaller than those without the split inductors.

As the conduction current becomes larger, both the conduction losses and the switching losses will increase, leading to increased total power device losses, as seen in Fig. 18(b).

In Fig. 18(c), as the modulation index increases, the power device loss rising speed without split inductors is faster than that with split inductors, which can be explained as follows. The larger the modulation index is, the wider the positive drive pulse will be, making the ratio of the current flowing forward the SiC MOSFET channel to the freewheeling current become larger ($|\varphi|<\pi/2$). It will decrease the advantage of the synchronous rectification in current freewheeling stage when without split inductors.

Similarly, when the power factor angle φ is smaller than $\pi/2$ (inverter mode), more currents will flow forward the SiC MOSFET channel compared with the freewheeling currents, making the forward conduction losses dominate the total conduction losses. While the freewheeling conduction losses will dominate the total conduction losses when φ is larger than $\pi/2$ (rectifier mode). Moreover, the forward characteristics of the SiC MOSFET channel are worse than the conduction characteristics in the current freewheeling stage, which can be seen from the datasheets of the adopted devices in this paper, making the power device losses decrease with the increasing φ in Fig. 18(d).

Overall, the power device losses with split inductors are lower than those without split inductors at high switching frequencies, due to the reduced switching losses can outweigh the increased freewheeling conduction losses. The reduced power device losses can lead to a smaller and lighter heatsink. However, the efficiency of the split output converter should also include the split inductor losses, which will be discussed in next section.

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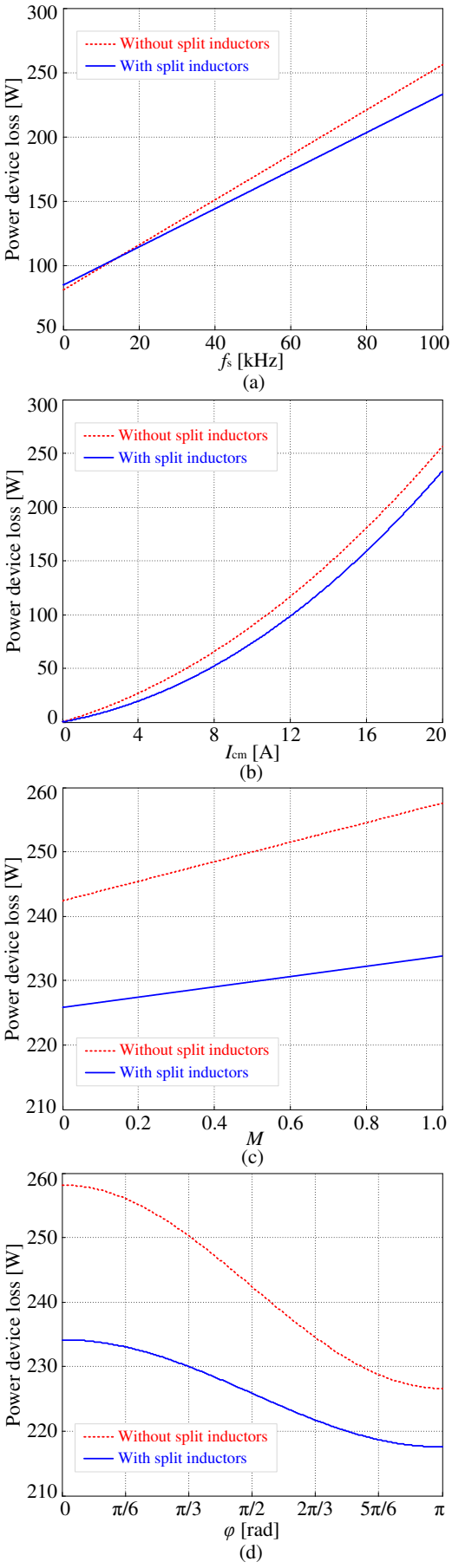

Fig. 18. The total power device losses of the three-phase split output converter without and with the split inductors of 10μH: (a) with f_c varying (I_{cm}=20A, M=0.9, φ=π/6), (b) with I_{cm} varying (f_c=100kHz, M=0.9, φ=π/6), (c) with M varying (f_c=100kHz, I_{cm}=20A, φ=π/6), and (d) with φ varying (f_c=100kHz, I_{cm}=20A, M=0.9).

VII. Experiments in Continuous Operating Mode

The previous sections have shown the DPT results. In this section, the results with the continuous operation of the converter will be shown. The power is drawn from a dc power supply and a three-phase *R-L* load is used. The parameters of the system are given in Table II.

TABLE II
Parameters of the Test System

Symbol	Parameter	Value
V_{dc}	DC-link voltage	600V
R_L	Load resistance	44Ω
L_{load}	Load inductance	6.2mH
L_s	Split inductance	10μH
R_{g_ex}	External gate resistance	6.2Ω
M	Modulation index	0.9
t_d	Dead time	1μs

The three-phase currents and line voltage at switching frequency of 100kHz are shown in Fig. 19. As seen, the three-phase currents without split inductors in Fig. 19(a) have much larger high-frequency harmonics than the currents with split inductors in Fig. 19(b), which further verifies the EMI benefit brought by split inductors. It should be noted that, the low-frequency distortions in the currents are caused by the dead time effect, which is observable at high switching frequencies. In addition, the PWM voltage waveform in Fig. 19(a) is not as clean as that in Fig. 19(b), due to the overshoot, undershoot, and ringing of the output voltage without split inductors, as analyzed in Section IV-B.

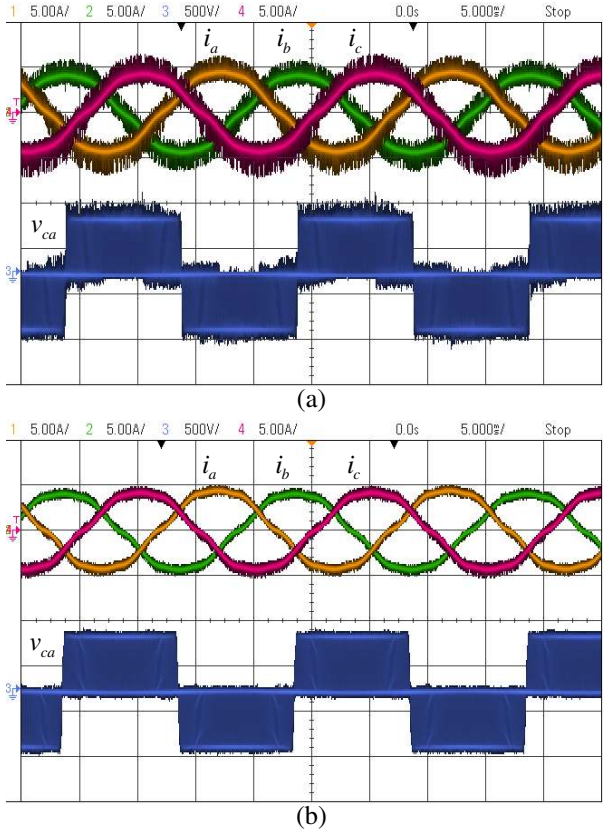

Fig. 19. Three-phase currents and line voltage at switching frequency of 100kHz: (a) without split inductors and (b) with split inductors of 10μH.

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Fig. 20(a) shows the current and voltage of the split inductors in continuous operating mode at the switching frequency of 100kHz. The current pulses and voltage spikes of switching frequency can be seen from the zoomed-in waveforms in Fig. 20(b). As seen, there are both low-frequency (50Hz) and high-frequency (100kHz) currents in the split inductors. The high-frequency current pulses together with the voltage spikes will generate significant losses in the split inductors. Special attention should be paid to the inductor losses when designing the split inductors.

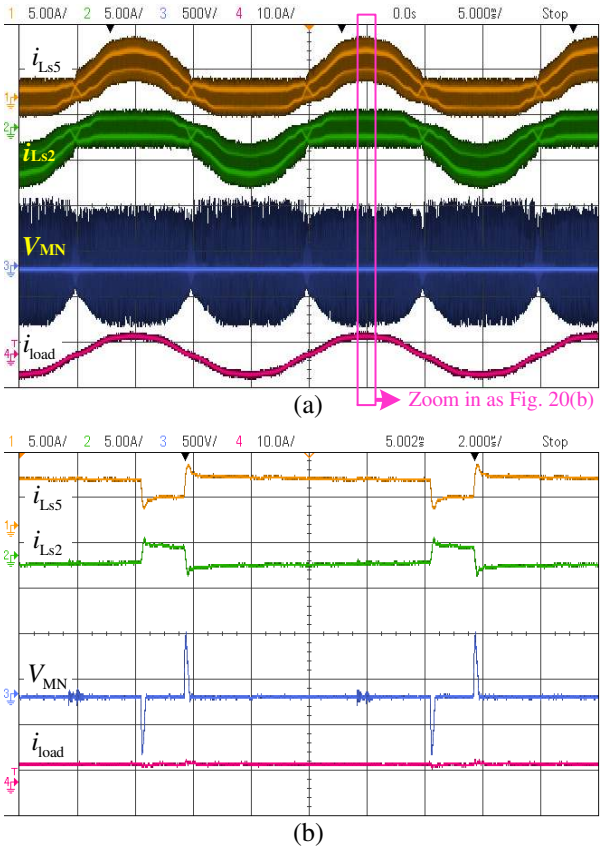

Fig. 20. Current pulses and voltage spikes of split inductors in continuous operating mode at switching frequency of 100kHz: (a) waveform overview and (b) zoomed-in details.

The efficiencies of the converter are measured without and with the split inductors of 10μH. During the efficiency measurement, a broad bandwidth power analyzer NORMA 3000 for precise power measurement is used to measure the output ac power. Meanwhile, with the dc offsets of the current and voltage probes corrected, the input dc power is calculated by the average dc current and voltage obtained by the oscilloscope. Nevertheless, the high efficiency at low operating power indicates small losses of the converter, which is challenging to be measured precisely. Therefore, after the measured efficiencies are plotted in Fig. 21, the efficiency measurement is further repeated several times to make sure the efficiencies in Fig. 21 have errors within an acceptable range. It should be noted that, as the switching frequency increases, the voltage loss between the reference voltage and the actual output voltage caused by the dead time will also increase, leading to the reduced operating powers, which are also plotted in Fig. 21.

As seen in Fig. 21, the converter efficiencies with split inductors are always lower than those without split inductors at each switching frequency. This phenomenon is clear at the switching frequency of 100kHz, where the converter efficiency with split inductors is 0.73% lower than that without split inductors (95.91% vs. 96.64%). The reduced power device losses by using the split inductors are calculated as 8.15W. Whereas the total split inductor losses are estimated about 13.77W based on the captured current waveforms in Fig. 20. The reduced power device losses are outweighed by the split inductor losses, which agrees with the reduced efficiency at 100kHz. In addition, smaller split inductances, e.g. 4.9μH, 2.5μH, and 0.9μH, have also been tested in the experiments, however the total efficiencies are still lower than those without split inductors.

The efficiency results based on the designed circuit show that, the reduced power device losses in the split output converter can be outweighed by the split inductor losses, impairing the efficiency of the split output converter. To further improve the efficiency, the split inductors with lower losses need to be employed, which may however increase the size and cost of the inductor and the converter.

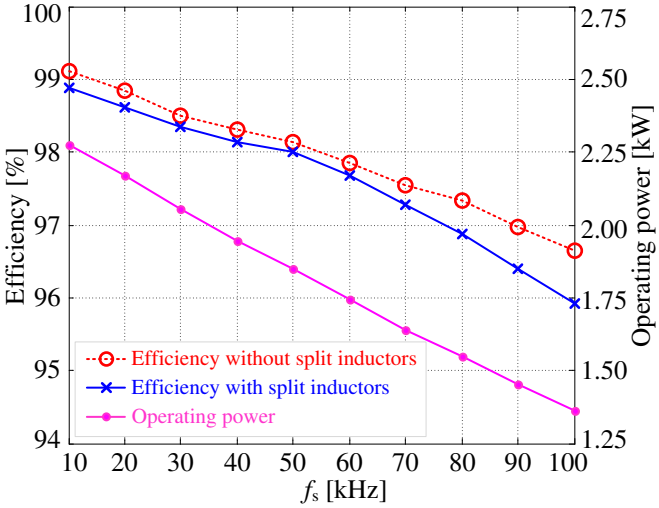

Fig. 21. Measured efficiencies without and with the split inductors of 10μH, and the corresponding operating power.

Regarding how the split inductances influence the converter efficiency, many factors should be taken into account. Firstly, as detailed in Section IV-A, V-A and V-C, both the reduced switching losses and the increased losses of the converter (caused by the current freewheeling problem and the disappeared synchronous rectification) can vary with different split inductances. Secondly, as shown in Section V-B, split inductors of different values can have different current pulses and voltage spikes generating different split inductor losses. And the design of split inductors (e.g. using different magnetic materials) can also influence the split inductor losses. Therefore, optimization of the choice of split inductances and the design of split inductors would be a challenging area of research, which may improve the efficiency of the split output converter to maximize its potential benefits in high-switching-frequency applications.

In addition, considering the split output converters with Si IGBTs, given the split inductors can buffer the reverse recovery current and the charging current of the output capacitance, the turn-on losses of Si IGBTs should also be reduced in the split output converter. Due to the unidirectional conductivity of the Si IGBT channel, there is essentially no synchronous rectification in Si IGBT-based converters. At high switching

frequencies, the Si IGBT-based converter with split inductors, though with split inductor losses, may have a higher efficiency than that without split inductors. However, compared with SiC MOSFETs and SiC JFETs, Si IGBTs have a relatively slow switching speed with large switching losses making it inferior in high-switching-frequency applications, which has been indicated by numerous papers [1], [2]. Besides, the EMI issue and the crosstalk effect in Si IGBT-based converters are not as serious as those in the converters with fast-switching SiC devices, thus the benefits of the split output converter cannot be fully exploited with Si IGBTs. In addition, extra split inductors are required in the split output converter, it is therefore not recommended to apply Si IGBTs to the split output converter.

As with SiC MOSFETs, the ultra-fast switching SiC JFETs can also bring issues, such as the spurious gate voltage with potential shoot-through failure, the high turn-on losses due to the large output capacitance, and the EMI problem caused by high *dv*/*dt* and *di*/*dt* [27]. The advantage and disadvantage of the split output converter with SiC JFETs can be similar to that with SiC MOSFETs. As analyzed in this paper based on SiC MOSFETs, the split inductors of the split output converter with SiC JFETs should also be able to suppress the spurious gate voltage avoiding the shoot-through failure, buffer the charging current of the output capacitance with reduced turn-on losses, and reduce the *dv*/*dt* of the output voltage leading to the EMI mitigation. Meanwhile, the issues caused by the split inductors, e.g. the current freewheeling problem, would also exist in the split output converter with SiC JFETs. The SiC JFET-based converter with optimally-designed split inductors may have a higher efficiency than that without split inductors at high switching frequencies. In addition, the normally-off SiC JFET without body diode essentially need an extra freewheeling diode [28], making it suitable for the split output converter which also needs extra diodes to build the converter. The split output converter with SiC JFETs would be a valuable area of future work.

VIII. Conclusions

A detailed investigation into the split output converter based on SiC MOSFETs and SiC Schottky diodes has been carried out both experimentally and analytically. The split output converter has both advantages and disadvantages. The crosstalk suppression capability of the split output converter has been proved by the proposed mathematical model and experimental results. The switching performance is improved with the lower turn-on current overshoot, the suppressed low-frequency current ringing during the turn-on transient, and the reduced current and voltage distortions at the turn-off transient. The reduced turn-on energy is higher than the increased turn-off energy leading to reduced total switching losses. The EMI mitigation in the split output converter has been verified by the DFT analysis on the output voltages. Meanwhile, the split output converter has issues such as the current freewheeling problem, the current pulses and voltage spikes of split inductors, and the disappeared synchronous rectification, which have been analyzed based on the experimental waveforms.

Due to the reduced switching losses, the split output converter can have lower power device losses at high switching frequencies compared to the standard two-level converter, even though the current freewheeling problem and the disappeared synchronous rectification can increase the conduction losses. However, the experimental results in continuous operating mode based on the designed circuit show that, the split inductor losses caused by the current pulses and voltage spikes can outweigh the reduced power device losses, impairing the efficiency of the split output converter. Further studies need to be carried out to optimize the efficiency of the split output converter to maximize its potential benefits in high-switching-frequency applications.

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