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Performance of differential pair circuits designed with line tunnel FET devices at different temperatures

M D V Martino[1,5], J A Martino[1], P G D Agopian[1,2], R Rooyackers[3], E Simoen[3], N Collaert[3] and C Claeys[4]

[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[2] Sao Paulo State University (UNESP), Campus Sao Joao da Boa Vista, Brazil
[3] Imec, Leuven, Belgium
[4] E.E. Department, KU Leuven, Leuven, Belgium

E-mail: mdvmartino@gmail.com

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Abstract

This work studies differential pair circuits designed with Line tunnel field effect transistors (TFETs), comparing their suitability with conventional Point TFETs. Differential voltage gain (A_d), compliance voltage and sensitivity to channel length mismatch are analyzed experimentally for different temperatures. The first part highlights individual characteristics of Line TFETs, focusing on behaviors that affect analog circuits. In comparison to Point TFETs, Line TFETs present higher drive current, better transconductance and worse output conductance. In the second part, differential pairs are studied at room temperature for different dimensions and bias conditions. Line TFETs present the highest A_d, while Point TFET decrease the susceptibility to channel length mismatch. In the last part, the temperature impact is investigated. Based on the activation energy, the impact of band-to-band tunneling and trap-assisted tunneling is discussed for different bias conditions. A general equation is proposed, including the technology and the susceptibility to temperature and dimensions. It was observed that Line TFETs are a good option to design differential pairs with higher A_d and ON-state current than Point TFETs.

Keywords: differential pair, analog performance, FinFET, Line TFET, Point TFET

(Some figures may appear in colour only in the online journal)

Introduction

At this point in time, where technological nodes reach the nanoscale domain, short channel effects, leakage currents and other undesirable behaviors become major roadblocks [1, 2]. Considering that the supply voltage and power dissipation cannot be scaled in the same ratio [3, 4], low power applications require new device concepts, such as tunnel field effect transistors (TFETs) [5, 6].

The basic TFET structure is a gate-controlled p-i-n diode, in which the dominant transport mechanism is band-to-band tunneling (BTBT), instead of drift-diffusion. This way, it is theoretically possible to obtain a sub-60 mV/decade sub-threshold swing (SS) at room temperature [7–9]. On the other hand, measurements of point tunneling devices revealed that the magnitude of trap-assisted tunneling (TAT) in the OFF-state region may be a critical issue to reach the expected SS values [10, 11].

In this context, Line Tunnel FET structures have been proposed in order to avoid SS degradation and to enhance the drive current [12, 13]. These devices are characterized by a source/gate overlap, so that the direction of tunneling and the gate electric field become aligned [14, 15]. While the Point TFETs ON-state current is unaffected by the channel length,

[5] Author to whom any correspondence should be addressed.

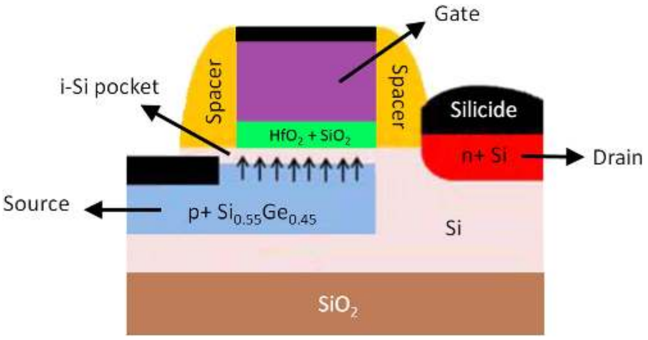

Figure 1. Line Tunnel FET structure.

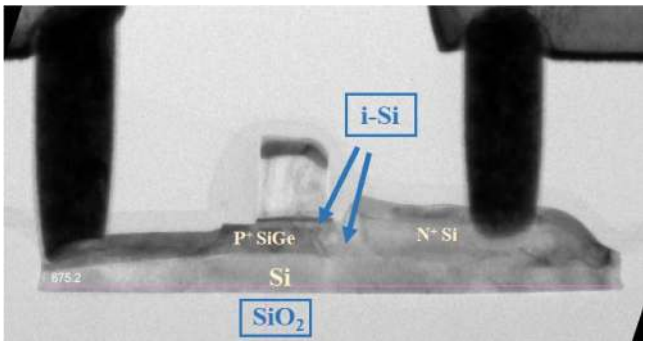

Figure 2. TEM image of a Line Tunnel FET structure.

this design proposed for Line TFETs makes its current to vary proportionally not only to the channel width but also to the channel length [16, 17].

Due to the promising advantages of individual TFETs, basic circuits have also been analyzed in recent papers [18, 19]. For instance, digital configurations such as multiplexers and inverters have been studied, mainly by simulations [20, 21], with a couple of papers presenting experimental data as well [22, 23]. Simulation approaches have also been used to investigate some basic analog applications [24–27].

Bearing interesting digital and analog applications in mind, this paper presents the experimental performance of Line Tunnel FET devices in a widely used circuit, namely a differential pair. The results are analyzed for different dimensions, bias conditions and temperatures. Preliminary results at room temperature have been published in [28] and other structures, such as Point TFETs, have been studied in [29, 30]. This way, it was possible to compare the results for these different technologies, with conclusions on the suitability of each of them in differential pair circuits.

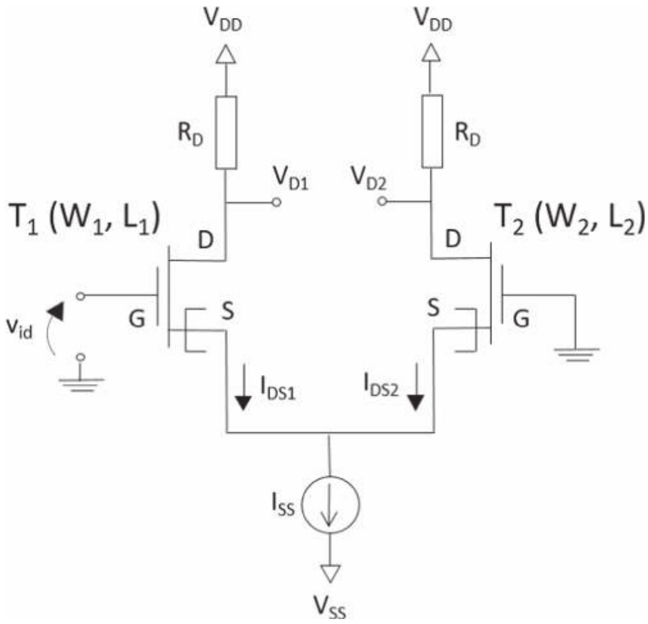

Figure 3. Differential pair circuit.

Device characteristics

The experimental results mentioned in this paper refer to transistors fabricated on 300 mm silicon-on-insulator wafers at imec/Belgium. The devices present a Si/SiGe heterojunction, known to provide enhanced performance, due to the lower bandgap at the source [31]. Line-nTFETs have been used, with a thin intrinsic silicon pocket layer on top of a p-type $Si_{0.55}Ge_{0.45}$ source, which extends under the gate. Source and drain regions are separated by an undoped Si channel.

The gate stack is composed of interfacial SiO_2 (1 nm), HfO_2 (1.8 nm) and TiN (2 nm), followed by deposition of p-doped amorphous silicon. In terms of channel mask dimensions, selected devices present a width of 70, 100 and 130 nm, and a length of 70 and 130 nm, respectively. Figure 1 shows a schematic structure of a Line Tunnel FET device while figure 2 gives a TEM image of a processed device. More details can be found in [31].

The Line TFET working principle is based on an increasing gate bias resulting in a potential well in the pocket conduction band. When the lowest sub-band in the pocket conduction band aligns with the source valence band, tunneling is triggered. Then, the positively biased drain collects the electrons, leading to a current with its magnitude increasing for wider and longer channels. This channel length dependence is different from the inverse proportionality observed for e.g. FinFETs and the non-dependence obtained for Point TFETs [5, 16, 17].

Methodology

The differential pair circuit is represented in figure 3. A differential input voltage (v_{id}) is applied on the T_1 gate, while the T_2 gate is grounded. The output V_{D1} is used to determine the differential voltage gain (A_d), defined as the ratio $A_d = |V_{D1}|/|\Delta v_{id}|$.

The analyses have been performed for different bias conditions, with $1.3\ V \leqslant |V_{SS}| \leqslant 1.5\ V$ and $-0.4\ V \leqslant v_{id} \leqslant +0.4\ V$. V_{DD} has been connected to ground. The susceptibility of the circuit to the transistors dimensions has been explored as well, with different values of channel width (70, 100 and 150 nm) and length (70 and 130 nm). Measurements have been taken for temperatures ranging from 25 °C to 175 °C.

Results and analysis

First of all, individual characterizations have been performed for each Line TFET at room and high temperatures. Figures 4

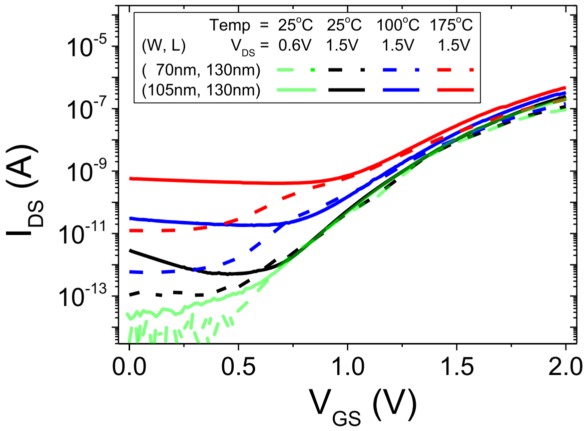

Figure 4. Drain current as a function of V_{GS} for Line TFETs with different dimensions, V_{DS} values and temperatures.

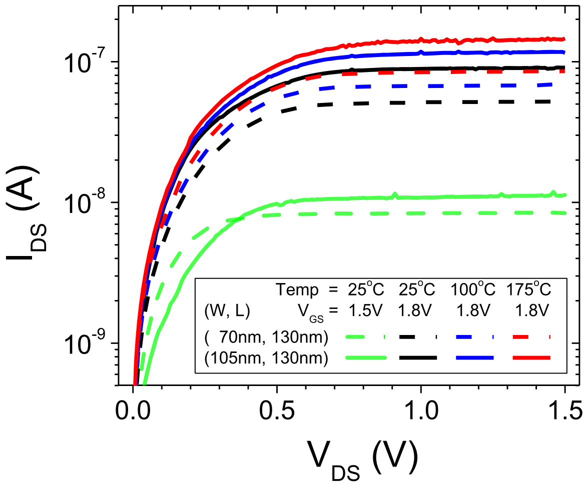

Figure 5. Drain current as a function of V_{DS} for Line TFETs with different dimensions, V_{GS} values and temperatures.

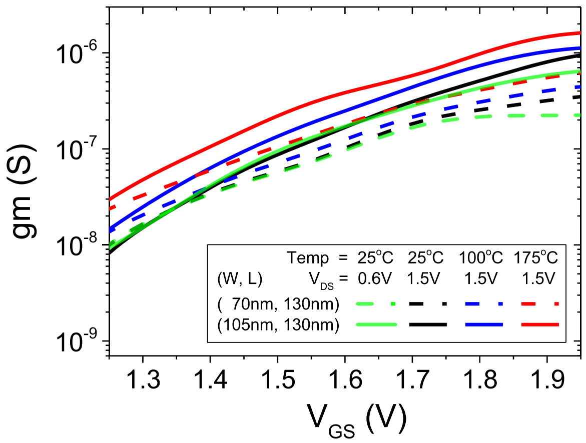

Figure 6. Transconductance as a function of V_{GS} for Line TFETs with different dimensions, V_{DS} values and temperatures.

and 5 show the input and output characteristic curves, respectively, revealing the impact of devices dimensions, bias condition and temperature. Meanwhile, figure 6 exhibits the transconductance as a function of the gate voltage and

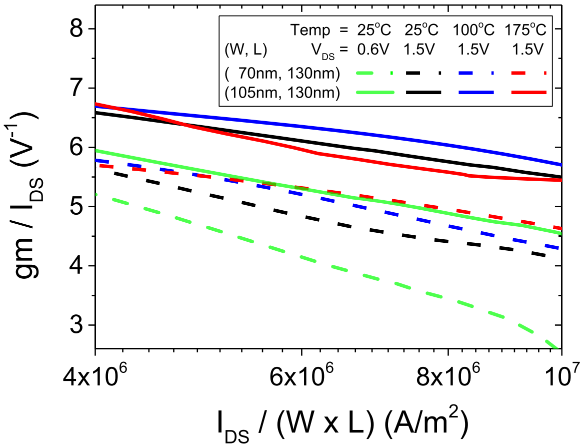

Figure 7. Transistor efficiency as a function of normalized drain current for Line TFETs with different dimensions, V_{DS} values and temperatures.

figure 7 illustrates the transistor efficiency as a function of the normalized drain current. Both of them are represented for the same bias and temperature conditions as figure 4, highlighting the on-state region.

Based on the previously explained Line TFET working principle, it is known that both I_{DS} and gm are directly proportional to the channel area. This is the reason for the normalization method applied for the plots in figure 7. A different channel length dependence is expected for FinFETs, in which the current decreases for longer channels due to the drift/diffusion mechanism, and for Point TFETs, which are not susceptible to the channel length due to the local tunneling perpendicular to the gate electric field.

This channel length dependence is summed up by equation (1), published and explained in [32]. The introduced parameter m refers to the different drain current susceptibility to the effective values of channel length (L_{ef}), leading to different behaviors of differential pairs designed with each technology.

$$I_{DS} \propto \frac{W_{ef}}{L_{ef}^{m}}, \qquad (1)$$

where: $m_{\text{Line TFET}} = -1$; $m_{\text{Point TFET}} = 0$.

It is worth mentioning that analogous input and output characteristic curves for Point TFET devices are reported in [33, 34]. Therefore, it is possible to compare relevant parameters, such as I_{DS}, gm, g_D and r_0. For instance, a Line TFET presents much higher on-state current when compared to a Point TFET, with an expected difference of up to 3 orders of magnitude for similar bias condition and channel dimensions. In terms of transconductance, the order of magnitude observed for Line TFETs in figure 6 (gm $\sim 10^{-7}$ S) is better than the lower values obtained for Point TFETs. On the other hand, regarding the output conductance and resistance, Line TFETs typical values can be extracted from figure 5 ($g_D \sim 10^{-9}$ S, $r_0 \sim 10^{9}\,\Omega$), which are worse than the ones observed for Point TFETs. Such parameters will also lead to differences in the behavior of basic circuits built with each of these technologies. This way, this individual comparison will be recapped in order to justify the differences observed in

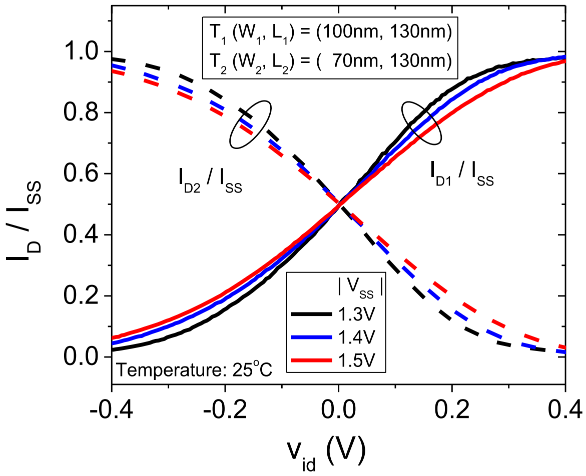

Figure 8. Normalized drain current as a function of differential input voltage for Line TFETs with different bias conditions values.

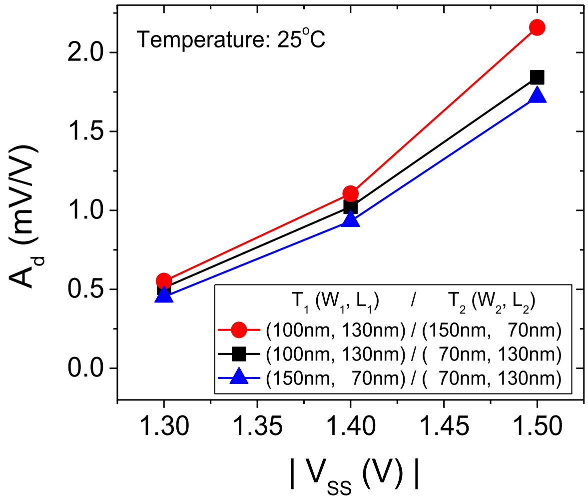

Figure 9. Differential voltage gain as a function of V_{ss} for Line TFET pairs with different dimensions.

relevant differential pairs parameters, such as the differential voltage gain (table 1).

Analysis of differential pairs at room temperature

After the analyses of individual devices, three differential pair circuits have been measured for different bias conditions. Figure 8 shows the normalized drain currents, I_{D1}/I_{SS} and I_{D2}/I_{SS}, as a function of v_{id}. It is possible to notice an increase in the overdrive voltage for higher values of I_{SS} (and V_{SS}), due to the raise in the gate-source voltage. This leads to a wider linear region, and a resulting higher compliance voltage, similarly to the trend observed for Point TFETs. The compliance voltage for Line TFETs and Point TFETs are close to each other [29]. The slope observed in figure 8 and the absolute values of drain current, showed in figure 4, can be used to extract the differential voltage gain for each condition. This way, since higher values of V_{SS} cause a significant increase in I_{SS} and a slight decrease in the normalized current slope, the overall value of A_d increases with V_{SS}.

Figure 9 sums up the bias impact on three different configurations of basic pair circuits. There is a similar trend of A_d susceptibility to V_{SS}, but the absolute values are higher for circuits designed with transistors with larger channel areas. Even with similar normalized current slopes, the difference once more follows the expected increase with I_{DS} for transistors with larger channel areas. This way, a similar procedure could lead to a comparison of A_d for Line TFETs and Point TFETs. In a general equation, the differential voltage gain may be expressed by two components: one represents the base magnitude value from the technology and bias condition (fitting parameter p), while the other comes from the drain current susceptibility to the channel dimensions (equation (1)).

$$A_d = p(\text{technology, bias}) \times f\left(\frac{W_{ef1}}{L_{ef1}^m}, \frac{W_{ef2}}{L_{ef2}^m}\right), \qquad (2)$$

where: $m_{\text{Line TFET}} = -1$; $m_{\text{Point TFET}} = 0$.

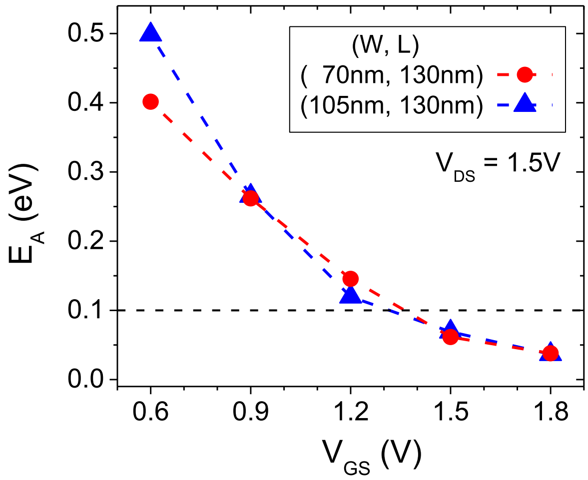

Figure 10. Activation energy as a function of V_{GS} for Line TFETs with different values of channel length and width.

Table 1. Features presented by differential pairs designed with Point TFET and Line TFET devices.

	Point TFET	Line TFET
High differential voltage gain		✓
High on-state current		✓
Low susceptibility to channel length mismatch	✓	
Low susceptibility to the temperature	✓	✓

Analysis of differential pairs at high temperature

The analysis of differential pair circuits at room temperature has been followed by the study of temperature impact, making use of previously obtained individual characteristics and including the activation energy in order to investigate the prevailing transport mechanism for different bias conditions. The activation energy values for the same devices represented in figures 4–6 are exhibited in figure 10.

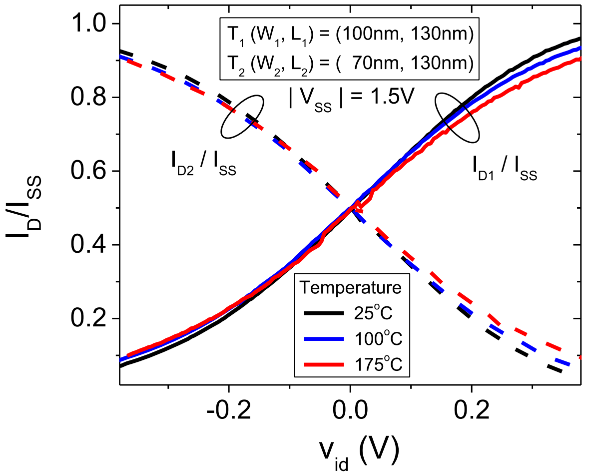

Figure 11. Normalized drain current as a function of differential input voltage for Line TFETs at different temperatures.

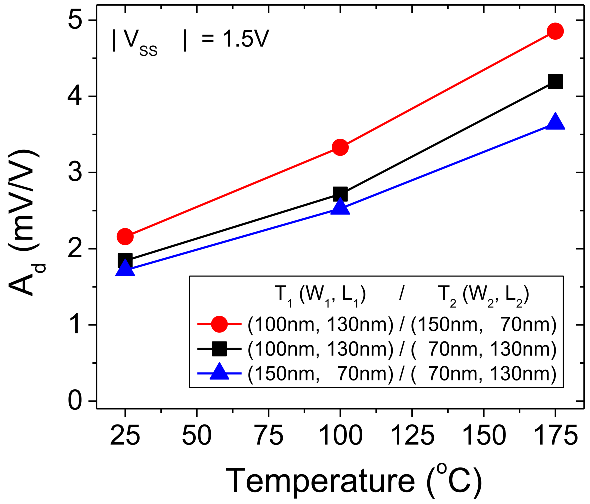

Figure 12. Differential voltage gain as a function of temperature for Line TFET pairs with different dimensions.

When the activation energy gets lower than 0.1 eV, the prevailing mechanism is BTBT, while TAT dominates otherwise [35]. This means that, when $|I_{SS}|$ is set so that $|V_{SS}| = 1.5$ V for $v_{id} = 0$ V, and then v_{id} ranges from -0.4 to $+0.4$ V, there will be a transition in the prevailing transport mechanism.

Figure 11 shows the normalized drain currents as a function of v_{id} for the same pair studied in figure 8, but now including data for three different temperatures. It is possible to notice a slight decrease in the slope for higher temperatures. On the other hand, since this difference is much smaller than the increase in I_{SS} observed (figure 4) for 100 °C and 175 °C, the overall differential voltage gain increases with temperature. This global impact of the temperature on A_d is illustrated in figure 12, including the same pairs previously studied at room temperature (figure 9).

Considering that the differential voltage gain is calculated based on the slope for $v_{id} = 0$ V and $|V_{SS}| = 1.5$ V, it is important to remember that it refers to the condition for which T_1 and T_2 are dominated by BTBT. Therefore, the A_d dependence on the temperature basically comes from the band gap (E_g) narrowing for higher temperatures, mathematically shown in equation (3) [36]. For the temperature range discussed in this work, there is a roughly linear dependence.

$$I_{BTBT} \propto e^{(-k.E_g{}^{3/2})}. \tag{3}$$

It is interesting to remember that the positive trend of A_d with temperature observed in figure 12, as a consequence of tunneling enhancement, is a very relevant difference when compared to conventional MOS devices, in which the negative trend is due to mobility degradation (and decreasing gm) under higher temperatures. For instance, a previous comparative study [30] showed a steep decrease by more than 50% in A_d for a differential pair with FinFETs exposed to the same temperature variation studied in this paper, in a way that the lower susceptibility to the temperature may be considered a very relevant advantage of TFET devices.

Therefore, a fitting parameter q, dependent on the activation energy of T_1 and T_2 impact at the operation temperature, could be included in equation (2). In this way, the general equation (4) takes into consideration also the temperature impact and its consequent dominant transport mechanism.

$$A_d = p(\text{technology, bias}) \times q(E_{A1}, E_{A2}) \times f\left(\frac{W_{ef1}}{L_{ef1}^m}, \frac{W_{ef2}}{L_{ef2}^m}\right), \tag{4}$$

where: $m_{\text{Line TFET}} = -1$; $m_{\text{Point TFET}} = 0$.

Finally, it is possible to make a comparison of differential pairs designed with different technologies in terms of differential voltage gain, on-state current, susceptibility to channel length mismatch and susceptibility to the temperature.

It is worth remembering that differential voltage gain (A_d) of a differential pair is directly proportional to its differential pair transistor transconductance (gm) and to the output resistance (R_O) resulting from the parallel association of output transistor resistance r_0 and load resistance R_D ($R_O = r_0 // R_D$). The individual parameters analysis based on figures 4–7 (Line TFETs) and on [33, 34] (Point TFETs) can be used to compare the resulting differential voltage gain for each technology. Since typical values of r_0 are much higher than R_D, the difference in A_d will derive basically from the contrast in gm. In other words, for differential pairs designed with the same external resistance, Line TFET higher values of gm always lead to a circuit with higher differential voltage gain.

Meanwhile, differential pairs designed with Line TFETs tend to present higher on-state currents, but Point TFETs are important for applications in which channel length mismatch is an issue. Both Point TFET and Line TFET can take advantage of the lower temperature dependence of BTBT and provide a less susceptible circuit in this point of view. Table 1 summarizes the features of each technology in terms of important parameters for differential pairs.

Therefore, Line TFET technology is a very good option for applications requiring high differential voltage gain and low susceptibility to temperature variation, since it can take advantage of a relatively high on-state current, which is a known disadvantage of Point TFET devices, and the suitable transport mechanism, typical of tunneling devices.

Conclusions

This work studied the performance of differential pairs designed with Line TFETs, based on experimental data obtained at room and high temperature. The suitability of this technology in comparison to Point TFET was discussed, including besides temperature, also dimensions and bias influence.

Line TFETs present the best values of drive current and gm, while Point TFET are the most suitable in term of g_D. These behaviors impact the differential pair designed with each kind of device. Combining the normalized current slope with the drive current magnitude, it was extracted that Line TFETs yield the highest differential voltage gain.

The analysis of the temperature impact points out that there was a transition in the dominant transport mechanism for the input differential voltage range, varying from TAT to BTBT. In order to extract the differential voltage gain as a function of temperature, both transistors in the differential pair have been biased such that BTBT was the prevailing mechanism. Since this mechanism causes a slight increase in the on-state current for higher temperatures, the effect on the circuit was an increase in the differential voltage gain for higher temperatures, in contrast to the A_d degradation observed for conventional MOS circuits. A global generic equation for the differential voltage gain as a function of technology, devices dimensions and temperature parameters has been proposed.

Taking all the results into consideration, it was possible to sum up the advantages and disadvantages of designing differential pair circuits with each of the studied technologies. If low susceptibility to channel length mismatch is a strong requirement, Point TFET would be the best option, but if the application requires a higher differential voltage gain, Line TFET devices would lead to the best overall performance. Therefore, it was possible to experimentally investigate Line TFET technology application in differential pairs at room and high temperature.

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ORCID iDs

M D V Martino https://orcid.org/0000-0003-2018-5092
P G D Agopian https://orcid.org/0000-0002-0886-7798

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