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PERFORMANCE OF DIGITAL INTEGRATED CIRCUIT TECHNOLOGIES AT VERY HIGH TEMPERATURES†

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Abstract

Results of detailed investigations of the performance and reliability of digital bipolar and CMOS integrated circuits over the 25 to 340°C range are reported. Included in these results are both parametric variation information and analysis of the functional failure mechanisms. Although most of the work was done using commercially available circuits (TTL and CMOS) and test chips from commercially compatible processes, some results of experimental simulations of dielectrically isolated CMOS are also discussed. In general, it was found that commercial Schottky clamped TTL, and dielectrically isolated, low power Schottky-clamped TTL, functioned to junction temperatures in excess of 325°C. Standard gold doped TTL functioned only to 250°C, while commercial, isolated I^2L functioned to the range 250°C 275°C. Commercial junction isolated CMOS, buffered and unbuffered, functioned to the range 280°C 310°C+, depending on the manufacturer. Experimental simulations of simple dielectrically isolated CMOS integrated circuits, fabricated with heavier doping levels than normal, functioned to temperatures in excess of 340°C. High temperature life testing of experimental, silicone-encapsulated simple TTL and CMOS integrated circuits have shown no obvious life limiting problems to date. No barrier to reliable functionality of TTL bipolar or CMOS integrated circuits at temperatures in excess of 300°C has been found.

Introduction

Requirements exist for active electronic components which function reliably at ambient temperatures in excess of 300°C. Component demand is currently for instrumentation used in logging of geothermal wells and in controlling jet engines in military aircraft; other areas such as nuclear reactor instrumentation are awakening to their need. For the geothermal well logging applications, reliable operation of systems at ambient temperatures near 325°C for periods exceeding 100 hours are required. By comparison, available oil well instrumentation systems are rarely rated for operation above 180°C ambient. Currently, jet aircraft engine control and monitoring systems are required to operate over the ambient range from -55°C to +260°C, with higher temperatures expected in experimental engines.

Initial results of research into the high-temperature capabilities of discrete silicon devices and commercially available digital integrated circuit (IC) technologies indicate feasibility of useful operation of economical digital ICs at ambient temperatures up to at least 300°C.[1-3] Complexity limits and reliability factors have not yet been firmly established, however. This paper discusses partial results which proceeded from a larger investigation of the high-temperature characteristics and capabilities of commercial, mainstream-compatible integrated circuit technologies. In the investigation, both CMOS and bipolar technologies were examined up to maximum temperatures well in excess of 300°C, with devices from several manufacturers being used for each generic category. Both TTL (standard and Schottky-clamped, dielectrically isolated and junction isolated) and I^2L (substrate-fed and standard) technologies were included in the bipolar technology category. For all of the bipolar generic types, the variation of the base emitter voltage with temperature causes a severe skewing of the gate transfer characteristics.

The performance characteristics of a wide range of simple, commercially available CMOS IC types, both buffered and unbuffered, were investigated. In addition, experimental simulations of the performance of simple dielectrically-isolated CMOS ICs were performed using specially fabricated hybrid devices. Both static and dynamic characteristics were investigated over the temperature range from 25°C to the maximum temperature of functionality. In all cases covered in this discussion, temperatures mentioned are junction temperatures since parameter measurement was performed dynamically, with little junction temperature rise above ambient. However, self-heating was found to not change the parameters significantly for ambient temperatures below 300°C.

The impetus for the experiments simulating dielectrically isolated CMOS came from the fact that investigations of the behavior of both dc and dynamic parameters of many commercial device types showed that acceptable performance is obtainable from monolithic bulk CMOS ICs at temperatures up to near 300°C, and that the largest obstacle to functionality at higher temperatures is the large supply leakage current. Experimental evidence and modelling of bulk CMOS devices indicate that most of this leakage current is attributable to the input/output protection circuitry and to the p-well-to-substrate junction leakage rather than to the individual active devices that constitute the basic logic gate. In order to investigate the utility of CMOS circuits at temperatures approaching 350°C, an experiment was conducted. By using thick film hybrid techniques, discrete transistors were interconnected to form logic gates which simulate those constructed with dielectric isolation. These circuits exhibit acceptable electrical characteristics at temperatures considerably higher than the junction-isolated types.

High Temperature Bipolar IC Performance

Investigation of high-temperature performance characteristics of TTL ICs focused on simple logic gates (2-input and 4-input NANDs) fabricated using standard junction isolation (J.I.) techniques and fabricated using both dielectric isolation (D.I.) and photocurrent compensation. Both gold-doped and Schottky-clamped technologies were involved in the investigation. Results were obtained from only one circuit type fabricated using photocurrent compensation and D.I. technologies (similar to the 54LS00 referred to subsequently as the "military" TTL circuit). Note that the work was intended to elucidate

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functional failure mechanisms and general parametric behavior rather than to define and determine detailed use-condition high temperature parameters of large populations. Devices from several manufacturers were used in the investigations, and both dc and dynamic characteristics were examined over the ambient range, 25°C, to slightly above 300°C where possible. The units referred to as commercial were off-the-shelf ceramic-encapsulated units.

Usable dc and ac characteristics were observed beyond 300°C ambient for both commercial and military Schottky-clamped TTL. Figures 1 and 2 show examples of typical unloaded transfer characteristics observed over the range 25°C to 325°C for a commercial 54S20-type 4-input NAND TTL gate and for a 54LS00-type 2-input NAND TTL gate. Clearly usable transfer characteristics are evident in the figures at least up to 300°C, although noise margin is something of a problem for the output low case. Although the data of Figure 1 applies directly only to devices from a particular manufacturer, characteristics of 54S20-type ICs from other manufacturers were essentially identical to those of Figure 1 in all important respects. In fact, except for lower maximum temperature limits and scaling of the behavior of some parameters, standard gold-doped TTL high-temperature performance characteristics were very similar to those shown in Figures 1 and 2 and other Schottky-clamped parameters discussed in subsequent sections. Most importantly, the high-temperature functional failure modes of commercial standard TTL, Schottky-clamped TTL, and military Schottky-clamped low-power TTL were identical, and the inferred failure mechanisms are the same for all of these types. Thus the following detailed discussions will concentrate on the military 54LS00-type IC with only passing reference to parameters of other TTL types.

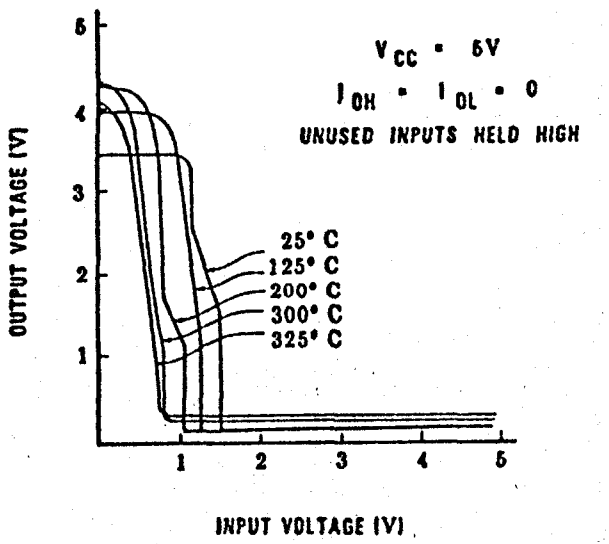

Figure 1. Voltage Transfer Characteristic of Commercial 4-Input 54S20-Type TTL NAND Gate, Various Temperatures

The functional failure mode in all cases (standard and Schottky-clamped TTL) was low V_{OH} (output High voltage). The beginnings of a trend to decreasing V_{OH} with increasing temperature can be seen in Figures 1 and 2 for 325°C. Analysis of transfer characteristic data along with data such as power supply current showed that the decrease in V_{OH} was caused by collector-base junction leakage current from the phase splitter transistor flowing through the phase splitter collector resistor. Up to temperatures very close to the maximum temperature of functionality, leakage current due to isolation junctions in the commercial de- did not contribute substantially to parameter degradation. The high temperature functional failure mechanism can be inferred by examining data such as that shown in Figures 3 and 4, which exhibit the behavior of power supply current for the output High state (I_{CCH}) and the behavior of output High voltage versus output High-sourcing current for the IC type of Figure 2. This data must also be correlated with the high temperature behavior of input Low current I_{IL}. If these intercomparisons are performed for the 54LS00-type IC or for any of the other TTL types mentioned earlier, it becomes clear that the observed reduction in V_{OH} cannot be due to output pulldown (due to leakage current into the base terminal, for example) by the current sinking transistor in any of the IC output stages. The high temperature output High-current sourcing capability of all the TTL types is so large that if sufficient current were sunk by the output current sinking transistor to cause the observed decrease in V_{OH}, the current would appear as a distinguishable additional component in the I_{CCH} versus T characteristic at high temperature. Most of the increase in I_{CCH} evident in Figure 3 at high temperatures can be accounted for by increase in I_{IL} at zero input voltage. This current increase originates in the collector-base junction of the phase splitter transistor and is diverted out the input terminal, appearing as an additional component of I_{IL} rather than flowing into the base terminal of the current sink transistor. The current does, however, flow through the collector resistor of the phase splitter circuit; the voltage drop caused by this leakage current thus results in a decrease in V_{OH}, since for moderate output (and power supply) currents V_{OH} follows the voltage drop across this collector resistor after being shifted down in voltage by one or two V_{BE} drops. Junction leakage current levels and resistor values combine in this way to give an upper temperature limit of functionality slightly in excess of 325°C for commercial Schottky-clamped TTL and military Schottky-clamped low power TTL. One exception to this was a military circuit which was something of a hybrid (in circuit design) between standard TTL and low power Schottky TTL; unique aspects of the circuit design limited the upper temperature of functionality to approximately 270°C for this circuit type.[3] Higher leakage current density levels, due to generation-recombination effects and relatively high circuit resistance levels, caused the upper functionality temperature limit of commercial standard (gold doped) TTL to be approximately 250°C.

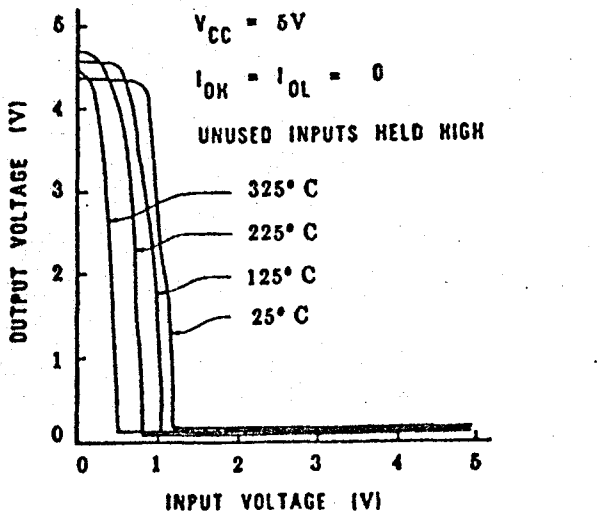

Figure 2. Voltage Transfer Characteristic of Military 2-Input 54LS00-Type TTL NAND Gate, Various Temperatures

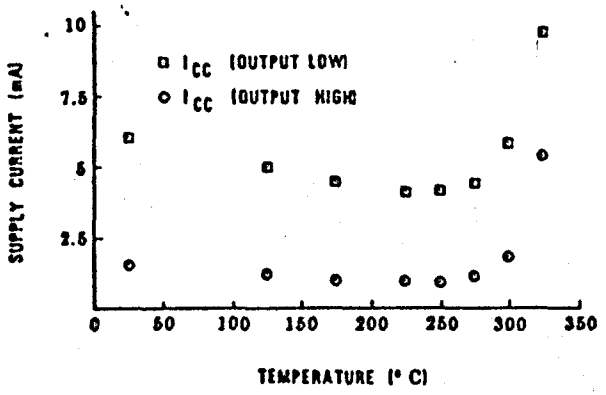

Figure 3. Power Supply Currents for Output High (I_{CCH}) and Output Low (I_{CCL}), Military 2-Input 54LS00-Type TTL NAND Gate, Versus Temperature

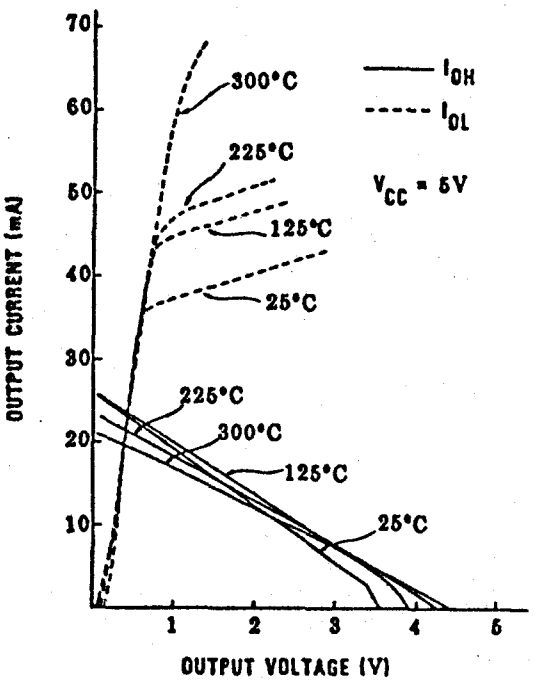

Figure 4. Current Sourcing and Sinking Versus Output Voltage, Military 2-Input 54LS00-Type TTL NAND Gate, Various Temperatures

From the behavior of I_{CCH} and the power supply current for output Low (I_{CCL}) at high temperature, shown in Figure 3, it is clear from this standpoint that operation at least to the neighborhood of 300°C is feasible. The high-temperature output drive capability shown in Figure 4 must be compared to high temperature I_{IL} and input High-current (I_{IH}) levels in order to determine whether fanout greater than unity is possible at high temperature. Figure 5 shows typical input I-V characteristics at various temperatures for the (military) circuit type of Figure 2. Comparison of Figures 4 and 5 lead to the conclusion that fanout greater than unity exists above 300°C for this circuit type. Standard and Schottky-clamped commercial TTL showed higher values of I_{IL} and I_{IH} (e.g., $I_{IH} \simeq 0.5 - 1$ ma at 300°C for commercial 54S20-type ICs). They also showed much higher output drive capabilities, and exhibit fanout capability greater than unity up to a temperature very close to the maximum temperature of functionality. The reduction in current sourcing capability evident in Figure 4 can be inferred to be due to increase in circuit resistance values with increasing temperature.[4] The increase in current sinking capability shown in Figure 4 can be inferred to be due to an increase with temperature in current sink transistor h_{FE}.[3]

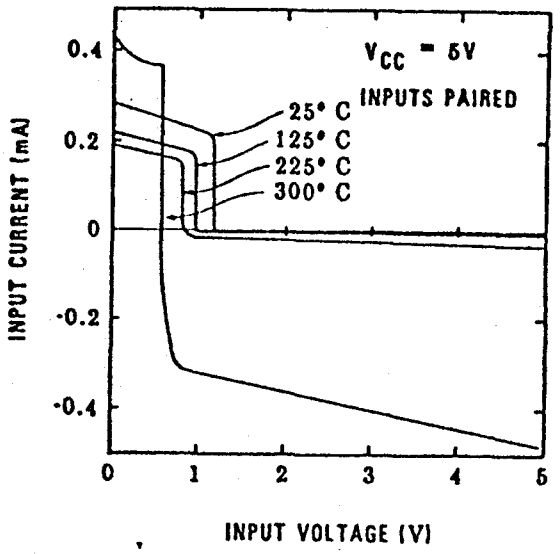

Figure 5. Input I-V Characteristics, Military 54LS00-Type TTL NAND Gate, Various Temperatures

The decrease in I_{IL} shown in Figure 5, with increasing temperature up to the neighborhood of 250°C, is understandable based on the behavior of the resistance of diffused resistors with temperature. The increase in I_{IL} for very low-input voltage, such as exhibited by the 300°C curve in Figure 5, is apparently due to collector-base junction leakage current flowing from the phase splitter transistor as discussed earlier. This phenomenon increases I_{IL} at high temperature, which is not desirable, but also tends to prevent h_{FE} multiplication of the leakage current by the phase splitter transistor, thereby extending the high-temperature performance range. The origin of the I_{IH} currents is in the clamp diode reverse leakage current; magnitudes of I_{IH} at high temperature were very similar for both Schottky-clamped and standard TTL. The magnitudes of I_{IH} were determined to be correlated with clamp diode area by comparison of the layout of the ICs under discussion here with the layout of a circuit reported earlier[3] which showed very low values of I_{IH}.

The behavior of propagation delays (t_{PHL}, output High to output Low delay time, and t_{PLH}, output Low to output High delay time) with temperature is shown in Figure 6 for the military 54LS00-type TTL NAND. The output load circuit used for these dynamic measurements was a standard 4 diode-load capacitance circuit such as that commonly specified by all manufacturers. The diodes were maintained at 25°C, and the load capacitance was 25 pF. Delay times were measured between 1.5 V levels at the output (even though the relevance of this voltage level is in question for high-temperature applications) for the sake of standardization and in the absence of a clearly better technique. The general characteristics of the behavior of propagation delays with temperature shown in Figure 6 were identical to the characteristics of other Schottky-clamped types investigated, although the 54S20-type ICs showed much smaller values of t_{PLH} and t_{PHL}. Standard TTL, on the other hand, showed a monotonic increase of t_{PLH} with temperature starting at 25°C, and, of course, did not function above 250°C. In view of the high-temperature $I_{OL} - V_{OL}$ characteristics shown in Figure 4, the insensitivity of t_{PHL} to temperature was

expected. However, the sensitivity of t_{PLH} to temperature, above 250°C, was unexpected and cannot be explained totally by the reduction of current sourcing capability shown in the characteristics of Figure 4. However, the drastic increase of t_{PLH} above 250°C can be explained by partial failure of the Schottky clamping of the current sink transistor collector-base junction due to a reduction in the forward biased voltage of the collector-base junction with temperature at a rate faster than that of a Schottky diode forward biased voltage drop. Crude calculations indicate that this mechanism can occur in the neighborhood of 250°C. The result would be, of course, the gradual onset, starting at some high temperature, of charge storage in the current sink transistor, strongly increasing t_{PLH} with increasing temperature. The lack of similar increase in t_{PHL}, due perhaps to charge storage in one of the current sourcing transistors, can be explained as being due to the fact that for high V_{OH}, for the load circuit used, the current sourcing transistors are not overdriven. They are in the linear active operating mode, assuming that dc leakage current in the current sink transistor is small, and thus charge storage phenomena would not affect t_{PHL} for low repetition rate measurements.

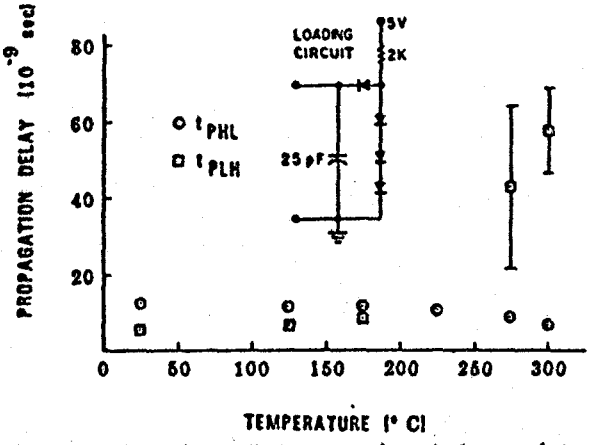

Figure 6. Behavior of Propagation Delays with Temperature, Military 54LS00-Type NAND Gate

High-temperature characteristics of substrate fed Integrated Injection Logic (I^2) and standard isolated I^2 were also investigated as an alternative to TTL. The two technologies showed similar characteristics over the temperature range, with standard I^2 being slightly superior in terms of high-temperature performance. Figure 7 shows behavior of standard I^2L gate delay versus gate power for a range of temperatures up to near the maximum temperature of functionality for this I^2L type (275°C). This data was obtained using a five-stage ring oscillator. The increasing deviation of the characteristic curves away from P • T_d (power • delay time) = constant (at low power) with increasing temperature is taken to be due primarily to increasing junction leakage in the gate transistors. Increase of the gate "speed" with increasing temperature is due to the decrease of the gate logic swing, which is caused by a decrease in V_{BE} with increasing temperature. This decrease in logic swing with temperature, which can be seen in Figure 8 for both substrate-fed I^2L and standard I^2L, eventually leads to functional failure at approximately 250°C and 275°C, respectively, when combined with the effects of OFF transistor leakage currents. The decrease in output amplitude for standard I^2L is seen from Figure 8 to follow closely the (normal) 2 mV/°C decrease in V_{BE} observed repeatedly for silicon junctions, up to a temperature at which the leakage current in the OFF device becomes appreciable. For substrate-fed I^2L the decrease in output voltage depends on the difference in the rate of decrease with temperature of a silicon V_{BE} and a Schottky diode forward voltage, and thus the output voltage does not follow the simple 2 mV/°C V_{BE} decrease.

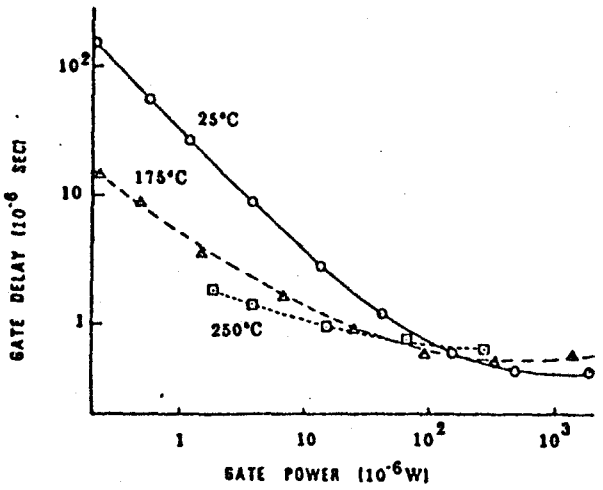

Figure 7. Standard I^2L Gate Power - Delay Characteristics, Various Temperatures

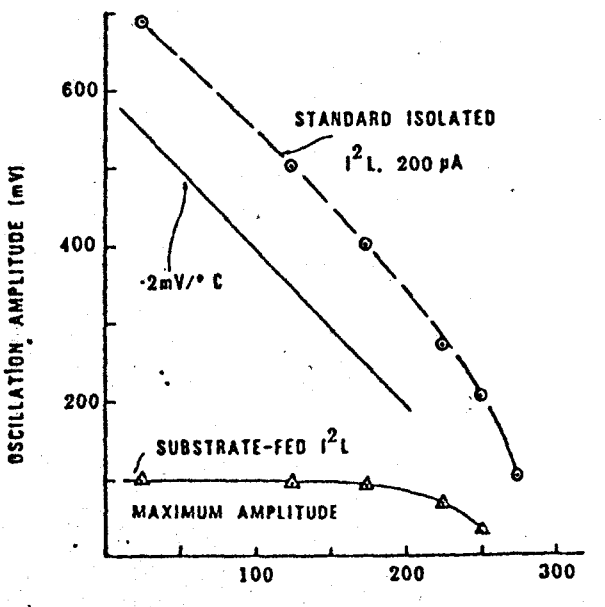

Figure 8. Ring Oscillator Output Voltage Amplitude, Standard I^2L and Substrate - Fed I^2L, Versus Temperature

CMOS High Temperature Characteristics

Investigations of commercial CMOS high-temperature properties were conducted primarily using 4012-type dual 4-input NAND gates fabricated by three major manufacturers, although the behavior of experimental devices was also examined. Both buffered and unbuffered circuits were used in the investigation. Quite acceptable static and dynamic characteristics were observed in circuits from all three manufacturers up to 270°C. Above this temperature, supply leakage current, due primarily to diode leakage in the p-well/substrate junction, eventually limited the functionality of all circuits. Unloaded transfer characteristics of a typical (unbuffered) CD4012 circuit in the normal operating temperature range and at high temperature are shown in Figures 9 and 10. The rise in V_{OL} at high temperatures exhibited in these

figures is characteristic of all CMOS NAND gates investigated, and is apparently caused by the inability of the n-channel transistors to properly sink the aggregate of the leakage currents at high temperature. Figure 11 shows typical behavior of the transfer characteristic for the buffered CMOS NAND gates investigated and also exhibits the rise in V_{OL} at high temperature. In fact, high V_{OL} was at least a part of the functional failure mode observed for all CMOS NAND gates, both commercial and experimental, at high temperature. Upper temperature limits to functionality of commercial types, based strictly on transfer characteristics, ranged from 280°C (unbuffered CD4012A) to 310°C buffered 4-input NAND) with all units of a particular type exhibiting limits very close to the mean limit temperature for that type.

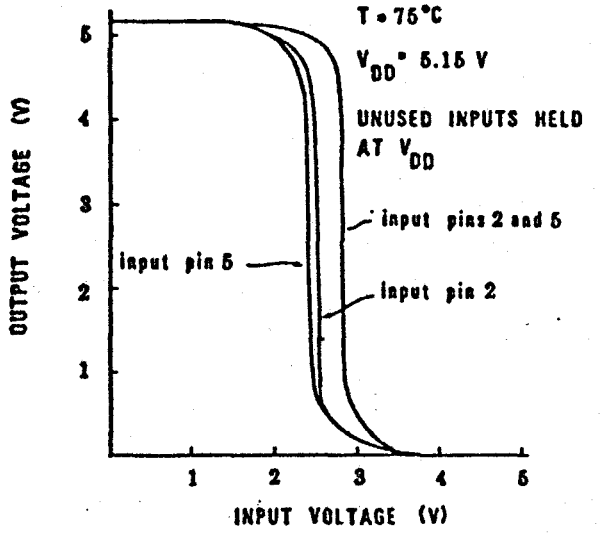

Figure 9. Voltage Transfer Characteristics of Unbuffered CD4012-Type CMOS 4-Input NAND Gate, 75°C

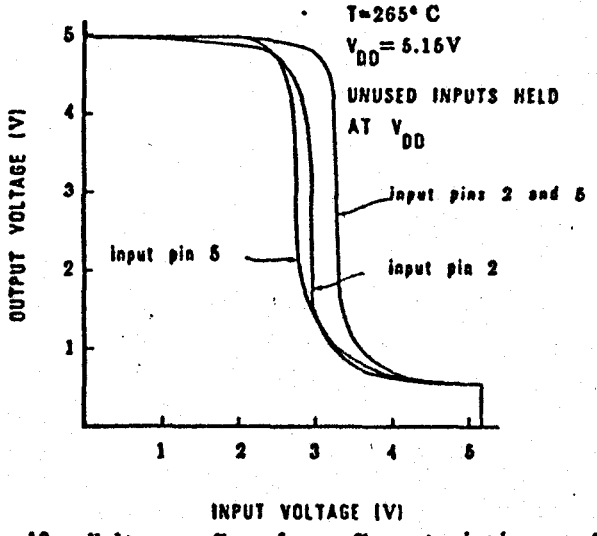

Figure 10. Voltage Transfer Characteristics of Unbuffered CD4012-Type CMOS 4-Input NAND Gate, 265°C

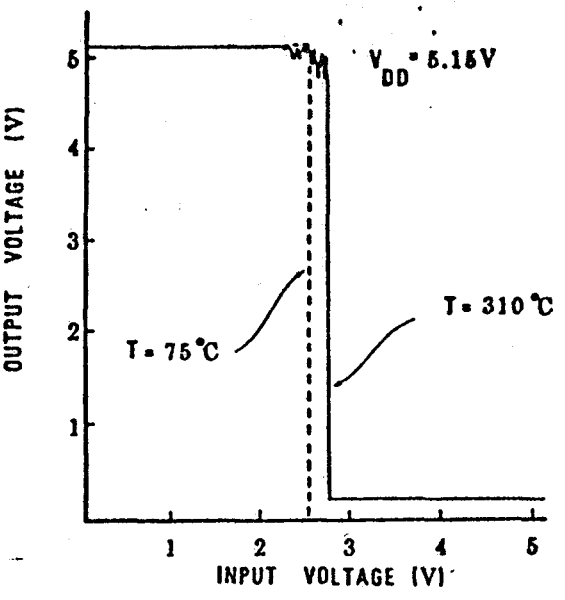

Figure 11. Voltage Transfer Characteristics of Buffered CMOS 4-Input NAND Gate

Leakage current due to the input and output protection circuitry was found to constitute a non-negligible fraction (~25 percent) of the total supply leakage current at high temperatures, but did not cause functional failure at high temperature. Table 1 shows an allocation of supply leakage current among the various sources. Note that this phenomenon (protection circuit leakage current) is not a fundamental characteristic of CMOS technology, and some simple modifications to the protection circuitry may control this leakage current component. The behavior of typical input current characteristics and supply leakage current characteristics with increasing temperature are shown in Figure 12 for V_{DD} = 5 V. Data shown in this figure was obtained from a buffered CMOS NAND circuit (F4012BDM) but is very similar in magnitude and temperature dependence to data obtained from other CMOS NAND types. The supply leakage current data shown is for all inputs High, which is the condition for maximum supply leakage for all CMOS NAND circuits investigated. I_{CCL} and I_{CCH} in the figures refer respectively to input current with the input at V_{SS} and V_{DD}. Two aspects of the data are worthy of comment. First, the behavior with temperature of all three currents is of the form $\exp(-E_A/kT)$ at least from 100°C to beyond 300°C, with E_A equal to or greater than 1 eV. This is a strong indication that the mechanism which gives rise to the leakage currents is diode leakage, which should have a temperature dependence of the form $I \sim T^{2.5} \exp(-1.21/kT)$, or $I \sim \exp(-1.31/kT)$, in the high-temperature regime. The data shown comes very close to this ideal behavior. Physical models also assign diode leakage as the source of the currents. Second, the magnitudes of both supply leakage current and the input currents are relatively low up to the neighborhood of 300°C, even though they are increased by many orders of magnitude over room temperature values. This is especially so of the input currents, and in this respect CMOS circuitry differs considerably from TTL circuitry. The limited current sourcing and sinking capability of CMOS, coupled with the decrease in these capabilities with increasing temperature means that input current demands must be kept low in order to maintain functionality.

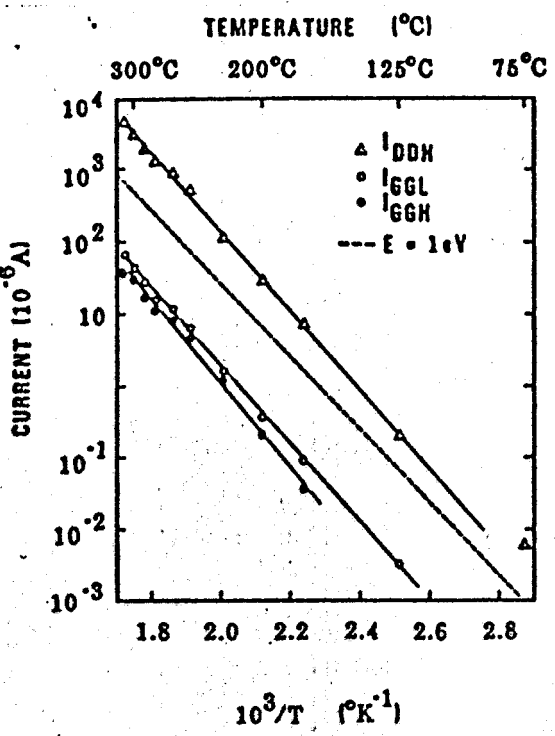

Figure 12. Input and Supply Leakage Currents Versus $10^3/T$, Typical Buffered CMOS 4-Input NAND Gate

The temperature dependence of CMOS output current affects the propagation delays at high temperature. Figure 13 shows edge "speeds" and propagation delays for a typical commercial unbuffered CMOS 4-input NAND gate. The behavior of propagation delays and rise and fall times of other CMOS NAND gates was very similar to the behavior of t_{PHL} and t_F shown in Figure 13 and and could in all cases be modeled by a decrease in current sinking capabilities of the gates due to reductions in carrier mobility and threshold voltages. The behavior of t_{PLH} and t_R shown in the figure was typical of CMOS NAND gates fabricated by one manufacturer, but was not typical of gates fabricated by other manufacturers, which showed monotonic increases in t_{PLH} and t_R with temperature (similar to the behavior of t_{PHL} and t_F). The behavior of t_{PLH} and t_R shown in Figure 13 was, however, correlated with a strong increase in output short-circuit current for High output on this gate type, while the monotonic increase of t_{PLH} and t_R for other gate types was correlated with a (more normal) continued decrease in current sourcing ability. The source of the anomalous increase in current sourcing capability for the gate type of Figure 13 is still being investigated.

Figure 13. Response Times for Typical Unbuffered CD4012A 4-Input CMOS NAND Gate Versus Temperature

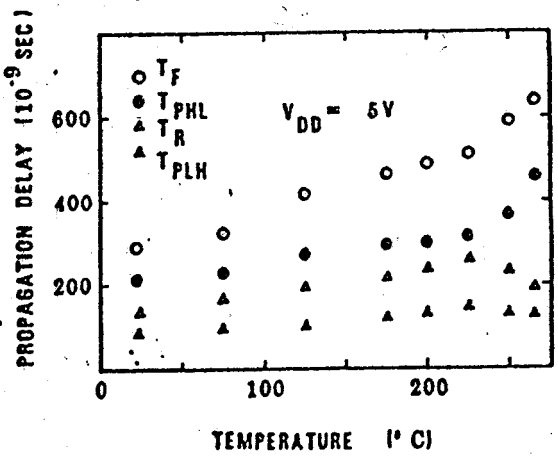

Table 1.
CMOS Supply Leakage Components, Commercial CMOS 4-Input NAND Gate

Current (10^{-6}A)	Temperature (°C)			
	75	200	250	265
Input Protection Circuit	9.6×10^{-5}	.471	8.8	19.2
P-Channel Drain-Substrate		.235	5.2	8.1
N-Channel P-Well-Substrate	3.5×10^{-5}	1.45	23.4	44
I_{DD} (All Inputs High)	6.28×10^{-4}	17.3	299	570
I_{DD} (Input 1A Low)	1.1×10^{-3}	15.8	270	525
I_{DD} (Input 1B Low)	1.0×10^{-3}	11.4	200	393

In an effort to demonstrate the potential of a high-temperature dielectrically isolated (D.I.) CMOS technology, several experimental devices were constructed. To simulate a D.I. process, n- and p-channel MOSFETs on separate chips were interconnected using thick film hybrid techniques to form a 2-input CMOS NAND gate. The construction and electrical characteristics of these high-temperature MOS transistors have previously been reported.[2,5] This arrangement eliminates the p-well-to-substrate leakage currents which were found to be so troublesome in junction isolated ICs. To reduce the circuit leakage currents even further, the gates were constructed without input protection networks.

Figures 14 through 20 show the transfer and supply current characteristics of one commercial and two experimental CMOS 2-input NAND gates at various temperatures. All gates used the same basic circuit configuration and none utilized output buffering. Figures 14 and 15 show the characteristics of an RCA 4011 circuit. This particular device is unusable at temperatures above 280°C because of high V_{OL}.

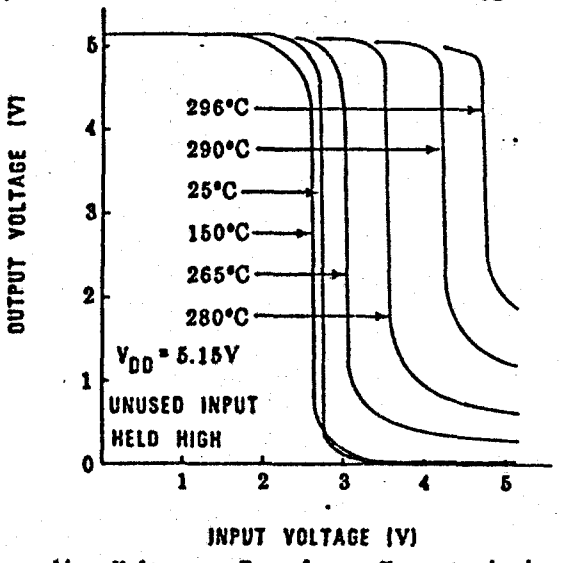

Figure 14. Voltage Transfer Characteristics of Unbuffered RCA 4011 CMOS 2-Input NAND Gate

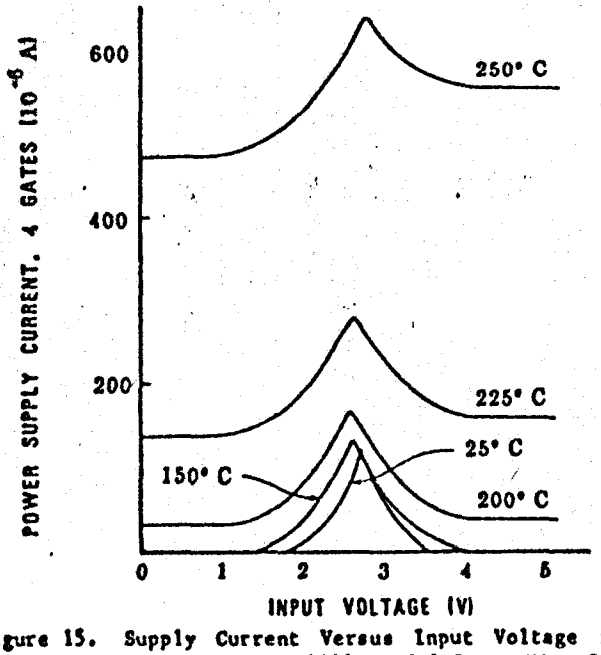

Figure 15. Supply Current Versus Input Voltage for Unbuffered RCA 4011 CMOS 2-Input NAND Gate

Figures 16 and 17 show the characteristics of one experimental gate. In this case the doping levels are approximately equal to those in the commercial 4011, but the transistors are larger. It can be seen that the elimination of the p-well/substrate junction and input protection diodes has greatly reduced the supply current at high temperatures. The leakage currents in the experimental circuits are primarily drain/substrate leakage currents. (Note that Figure 15 shows current for four gates, while Figure 17 deals with only one.) If the transistors used in the experimental circuit were scaled down to match those in the RCA devices, the leakage currents could be reduced by at least another factor or two.

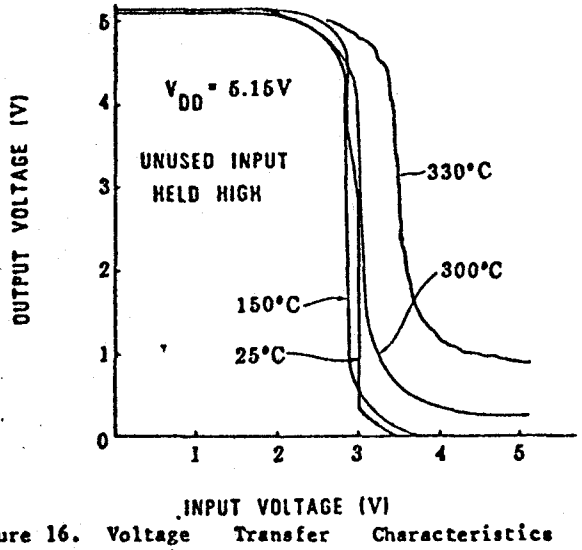

Figure 16. Voltage Transfer Characteristics of Experimental CMOS 2-Input NAND Gate

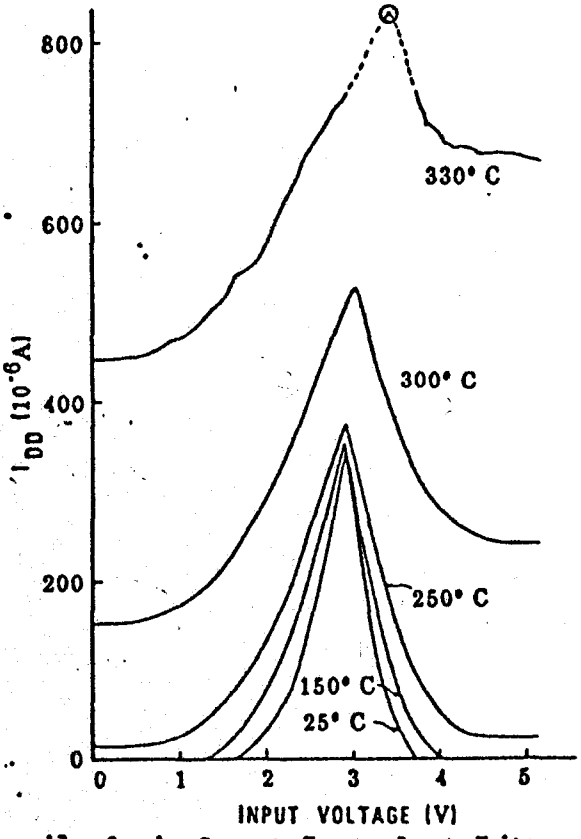

Figure 17. Supply Current Versus Input Voltage for Experimental CMOS 2-Input NAND Gate

More heavily doped, high-threshold MOSFETs were used to construct another experimental NAND gate which displayed excellent characteristics to 300°C and good characteristics to 340°C (Figures 18 and 19). These transistors are of the same geometry as those used in Figures 16 and 17, but the increased doping

levels served to reduce drain/substrate leakage and to increase threshold voltage. At room temperature $V_{T,N} \simeq 3$ and $V_{T,P} \simeq -2$, giving rise to the sharp transfer characteristic. The high doping levels also enabled enhancement mode operation at temperatures well above 300°C—a necessity in CMOS circuits if low-current drain is desired. Output buffering, using two high-temperature CMOS inverters, could extend the maximum usable temperature of this circuit to as high as 360°C. GaP or GaAs diodes could be used to give reliable, low-leakage input protection.

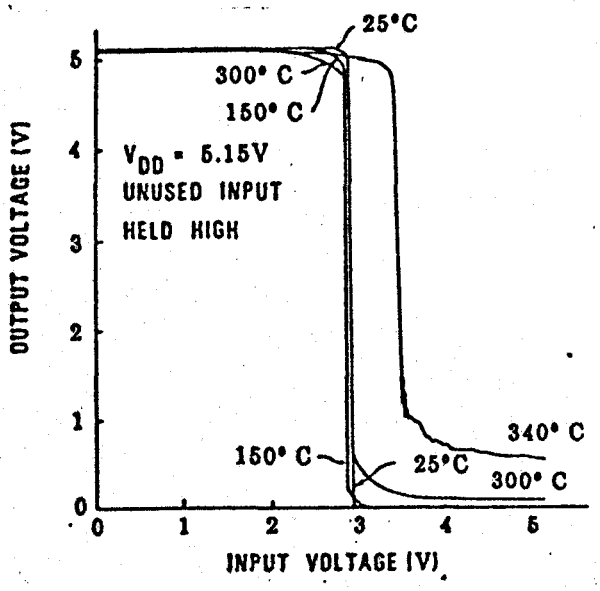

Figure 18. Voltage Transfer Characteristics of Experimental CMOS 2-Input NAND Gate

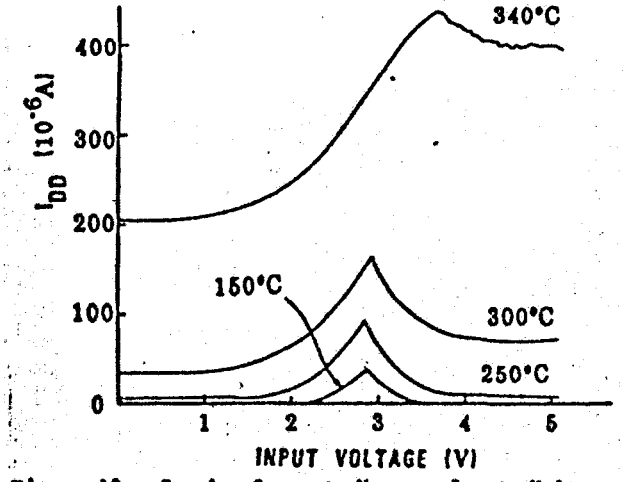

Figure 19. Supply Current Versus Input Voltage for Experimental CMOS 2-Input NAND Gate

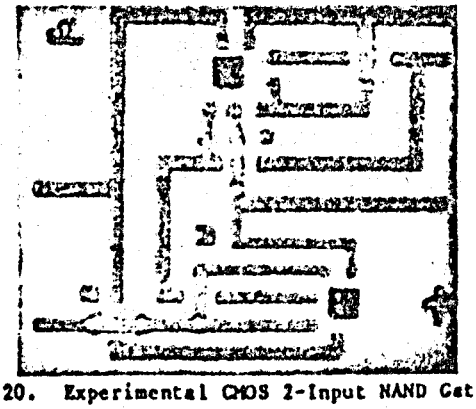

Figure 20. Experimental CMOS 2-Input NAND Gate

An alternative to normal J.I. or D.I. CMOS is Silicon-On-Sapphire (SOS) CMOS. CMOS ICs fabricated using this technology would not have p-well-to-substrate junctions; and the high-V_{OL} failure mode, at least due to leakage of these junctions might be prevented. Imperfections in the silicon film do give rise to the possibility of other high-temperature functional failure modes due to transistor leakage. Investigations into the high temperature properties of SOS transistors have begun, and these will be extended to the properties of SOS CMOS ICs as appropriate. Figure 21 shows the behavior of I_D for $V_{GS} = 0$ (I_{DSS}) for typical edgeless and normal p-channel and n-channel SOS MOSFETs. The activation energy exhibited by the I_{DSS} data is quite low compared to that normally exhibited by bulk discrete and IC MOSFETs. For bulk devices of room-temperature threshold voltage, V_T, comparable to the devices of Figure 21 (1 to 2 V), I_{DSS} at high temperatures is primarily composed of drain-substrate leakage current. However, the channel current component of I_{DSS} cannot be totally neglected at high temperature. This channel current can have a large inversion-layer component if the low-threshold transistors are operating in the depletion mode at high temperatures. Because of back gate effects and other unique aspects of SOS technology, the behavior of V_T versus temperature for SOS MOSFETs is, in principle, more complicated than that of bulk devices. Comparison of the behavior of p-channel and n-channel I_{DSS} in Figure 21 shows that either "subthreshold" channel currents are negligible, or the subthreshold currents are identical for the two different device polarities. This last possibility seems unlikely. Thus the I_{DSS} currents must be primarily due to junction leakage effects. The values of I_{DSS} shown in Figure 21 are remarkably low; based on information available now, SOS CMOS appears to have real promise as a high-temperature technology.

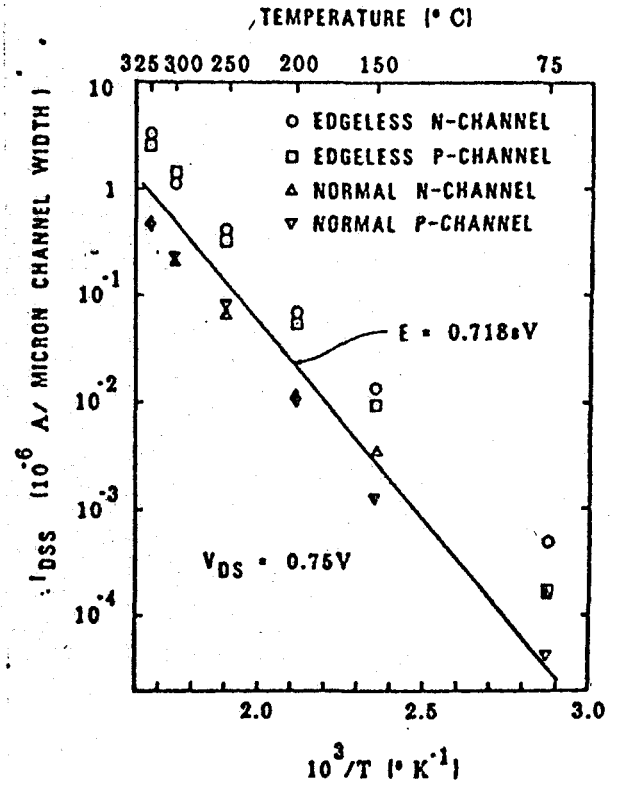

Figure 21. Typical Behavior of I_{DSS} with Temperature for Four Silicon-On-Sapphire MOSFET Types

High Temperature Reliability

In order to obtain information on high-temperature parameter stability and possible major failure modes of bipolar and CMOS ICs, operating life tests were performed for times ranging up to 4,000 hours. The units used in the life tests were not standard commercial technology ICs. They were silicone-encapsulated, copper beam-tape bonded devices fabricated using a chip technology similar to the beam lead-sealed junction technology, including the use of trimetal PtSi-Ti-Pt-Au metallization. Ambient test temperatures were chosen to be somewhat under the maximum operating temperatures of the device types. Ambient temperatures and device types were 225°C, TTL type 5420; 265°C, Schottky-clamped TTL type 54S20; and 265°C, CMOS type CD4012A.

The operating tests from which the data was obtained involved 14 units of each type for the CMOS and standard TTL types, and eight units for the Schottky TTL type, of which one-half had inputs held High 90 percent of the time and Low 10 percent of the time, and one-half had inputs held High 10 percent of the time and Low 90 percent of the time. The input pulse repetition rate was 1 Hz. Power supply voltage was 5 V in all cases, and parameter measurements were performed only at high temperature.

The life test behavior of two critical parameters is shown in Tables 2 and 3 for the two TTL IC types. More complete parameter data for typical life-tested TTL units is shown in Tables 4 and 5. Of the total 22 TTL units subjected to life testing (14--5420, 8--54S20) only one 54S20 gate showed true functional failure, i.e., inability to execute a 4-input NAND truth table. This failure occurred between 500 hours and 2,000 hours of test. The sister gate, in the same package, functioned with little parameter change after 2,000 test hours. Taken in total, the data in Tables 2 through 5 exhibit acceptable parameter stability for most applications, out to the termination of the life tests. One puzzling factor was the decrease of I_{IH} during the life test, shown in Table 2. The mechanism for this decrease has not yet been identified.

The behavior of selected parameters of the CD4012-type CMOS NAND gates versus time on life test is shown in Table 6. The CMOS life test population showed two different types of behavior. Eleven units showed little or no change in parameters during the tests, while four units showed abrupt increases in input current and other parameters. The data of Table 6 was taken from the "stable" 11 units. Table 7 shows the behavior of parameters of one of the four unstable units during the life test; a strong increase in I_{CCH} is evident at the 200-hour parameter measurement point, and a subsequent increase in I_{OHS} is clear at the 2,000 hour measurement point. The source of these increases has not been identified. The devices did, however, function after the parameter changes shown and showed very little change in gate-threshold voltage V_{TH}. Results are at the least promising in terms of reliable high-temperature functionality. It is possible that damage to the input protect circuitry ("zapping") during parameter measurement was responsible for the changes in input current requirements observed.

Table 2. Behavior of Lot Mean $I_{IH}(V_I = 2.4\ V)$ and $V_{OL}(I_{OL} = 2\ mA)$ for 54S20 TTL Gates, 265°C Ambient Life Test

	TIME (hr)	
Parameter	100	2,000
I_{IH}(mA)	0.283	0.165
V_{OL}(mV)	114	130

Table 3. Behavior of Lot Mean $I_{IH}(V_I = 2.4\ V)$ and $V_{OL}(I_{OL} = 1\ mA)$ for 5420 TTL Gates, 225°C Ambient Life Test

	TIME (hr)			
Parameter	50	200	1,000	2,000
I_{IH}(mA)	0.298	0.336	0.310	0.311
V_{OL}(mV)	100	102	101	103

Table 4. Typical Results of 265°C Life Test on 54S20-Type TTL NAND Gates.

	TIME (hr)	
Parameter	100	2,000
I_{CCH}(mA)	6.67	6.67
I_{CCL}(mA)	4.00	4.13
V_{OL}*(mV)	115	130
V_{OH}**(V)	4.09	4.08
I_{OS}(mA)	31.9	29.3
I_{IL}(mA)	0.680	0.972
I_{IH}(mA)	0.268	0.202

*V_I = 2.4 V, **V_I = 0.4 V

Table 5. Typical Results of 225°C Life Test on 5420-Type TTL NAND Gates.

		TIME (hr)					
Parameter		0	50	500	1,000	1,500	2,000
I_{CCH}(mA)		5.65	5.67	5.75	5.74	5.74	5.71
I_{CCL}(mA)		4.00	3.96	4.06	4.05	4.05	4.04
V_{OL}*(mV)		91	121	123	123	123	118
V_{OH}**(V)		3.78	3.81	3.78	3.73	3.66	3.64
I_{OS}(mA)		19.6	19.5	17.3	17.7	19.0	19.2
I_{IH}(mA)	Input A	0.318	—	0.307	—	0.305	—
	Input B	—	0.321	—	0.337	—	0.339
I_{IL}(mA)	Input A	0.881	—	0.885	—	0.883	—
	Input B	—	0.918	—	0.915	—	0.910

*V_I = 2.4 V, **V_I = 0.4 V

Table 6. Behavior of Mean, Highest, and Lowest Values of Selected Parameters, CD4012-Type CMOS NAND Gates, 265°C Ambient Life Test. Data Excludes Four Units Exhibiting High I_{GGH} and I_{OHS}.

	TIME (hr)						
Parameter	50	100	200	400	1,000	2,000	4,000
I_{DDL}(mA)							
high	1.261	1.256	1.251	1.245	1.255	1.243	1.100
mean	1.046	1.045	1.042	1.034	1.046	0.936	0.910
low	0.779	0.773	0.767	0.753	0.772	0.762	0.682
I_{DDH}(mA)							
high	1.082	1.071	1.086	1.057	1.069	1.053	0.925
mean	0.876	0.873	0.891	0.864	0.877	0.786	0.749
low	0.643	0.638	0.652	0.621	0.640	0.631	0.555
I_{GGH}(μA)							
high	5.91	5.97	6.08	6.08	7.76	21.0	12.18
mean	4.54	4.61	4.69	4.69	4.95	5.72	4.62
low	2.95	2.99	3.07	3.07	3.19	3.16	2.75
I_{GGL}(μA)							
high	18.2	18.2	19.2	19.0	19.9	43.0	18.5
mean	14.4	14.4	14.9	14.8	15.5	16.0	12.2
low	10.3	10.3	10.7	10.6	10.6	10.8	8.7

Table 7. Behavior of Selected Parameters of a CD4012-type CMOS NAND Gate Versus Time on 265°C Operating Life Test. Unit Shown was One of Four (Out of Fifteen) Which Showed Significant Parameter Change.

	TIME (hr)						
Parameter	50	100	200	400	1,000	2,000	4,000
I_{DDL}(mA) (per package)	1.147	1.132	1.787	1.861	1.812	1.794	1.580
I_{GGH}(μA)	5.14	1.16	317	317	331	339	320
I_{GGL}(μA)	17.8	17.9	20.5	20.4	20.8	20.5	15.8
I_{OHS}(mA)	5.001	4.986	4.101	4.079	4.262	58.0	55.0
I_{OLS}(mA)	1.560	1.534	2.197	2.150	2.144	2.20	2.1
I_{OL}(V)	.176	.176	.195	.197	.199	.198	.148
V_{DD}-V_{OH}(V)	.0084	.0082	.297	.296	.305	.312	.303
V_{TH}(V)	2.94	2.93	2.70	2.68	2.71	2.73	2.67

Conclusions

While standard gold-doped TTL functioned only to 250°C, it was found that Schottky-clamped TTL is functional at temperatures above 325°C. At high temperatures, however, the noise margin may become extremely small. In all cases the functional failure mode was low V_{OH}, caused by collector-base leakage current from the phase-splitter transistor flowing through the phase splitter collector resistor.

Unbuffered commercial J.I. CMOS functioned to 280°C, buffered J.I. CMOS functioned to 310+°C and experimental, simulated D.I. CMOS functioned to temperatures in excess of 340°C. In the NAND gates studied, the functional failure mode was high V_{OL}, a condition caused by the inability of the n-channel transistors to properly sink the junction leakage currents.

The investigations demonstrate conclusively that potentially useful performance characteristics can be obtained from some silicon integrated circuits at temperatures well in excess of 300°C. Based on this work and further work on performance-limiting mechanisms, useful characteristics of specially designed and constructed silicon ICs at temperatures in excess of 325°C are expected. Questions of reliability are not totally resolved at this point, but no insurmountable barriers to reliable high-temperature operation have been found.

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