Open access • Journal Article • DOI:10.1109/23.289280

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Published on: 01 Apr 1991 - IEEE Transactions on Nuclear Science (IEEE)

Topics: Test bench and Effective number of bits

Performance of Flash ADCs in the 100 MHz Range
I. Test Bench and Preliminary Results

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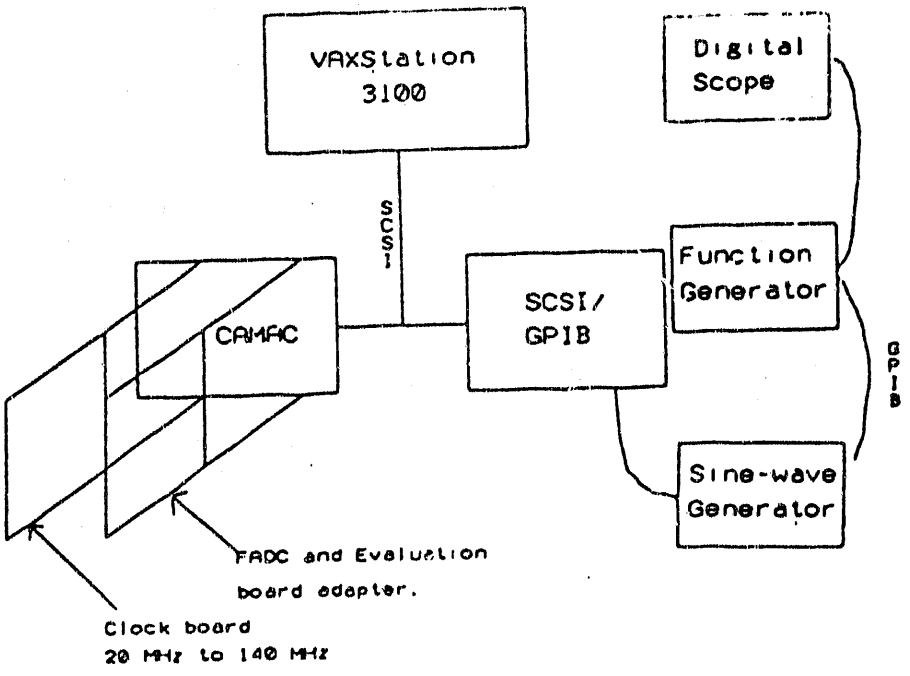

Figure 1 -- Test Bench Block Diagram

Abstract

We describe a systematic study of the performance of commercially available Flash ADCs in the 100 Megasample per second range, which might be suitable for use at the Superconducting Super Collider. Performance characteristics are measured using a CAMAC based test bench which is described. Among the FADC performance characteristics reported are linearity, differential linearity and the effective number of bits. This paper is the first in a series of reports to be presented within the next year as our tests continue.

INTRODUCTION

As presently designed, beams at the Superconducting Super Collider will collide once every 16 nsec. Thus it may be necessary to collect data at a comparable rate, i.e. 62.5 MHz. At the very least, trigger information will need to be gathered at this rate. In conjunction with the design of a compensating scintillator plate calorimeter, we have begun an investigation of devices capable of digitizing the analog signals produced by a detector at such rates. In particular, we report on commercially available Flash A/D converters in the 100 Megasample per second range. All of the devices we report on here use 8-bits to specify the digital value. However, it should be noted that for a given application dynamic ranges greater than 255:1 can be achieved using non-linear conversion curves.

In order to perform these investigations, we have developed a CAMAC-based test bench along with the appropriate software. Our testing procedure follows the guidelines given in IEEE Std 1057, "IEEE Trial-use Standard for Digitizing Waveform Recorders."

In the following sections we describe the test bench hardware and software and present preliminary results on three commercially available FADCs, the Analog Devices AD9002, the Sony CX20116 and the Sony CXA1176.

TEST BENCH DESCRIPTION

A. Hardware

A block diagram of our test bench hardware configuration is shown in figure 1. A VAXstation 3100 [1] running VMS controls and monitors the test bench. Communication between the computer and the test bench is via the SCSI port. A SCSI to CAMAC crate controller [2] provides communication with a single CAMAC crate containing two special purpose CAMAC boards. The bus converter [3] allows GPIB communication with a function generator [4], synthesized signal generator [5] and a digital oscilloscope [6]. The function and signal generators provide input signals to the FADC units.

A special clock generator board built for this test bench provides trigger and clock signals to the FADC unit. Ten discrete values of the clock signal provided to the FADC are available in the range 20 -140 MHz. Extension to lower values is possible. This allows us to test devices with dynamic ranges wider than those currently available at high sampling frequencies. Both TTL and ECL signals are available from this board.

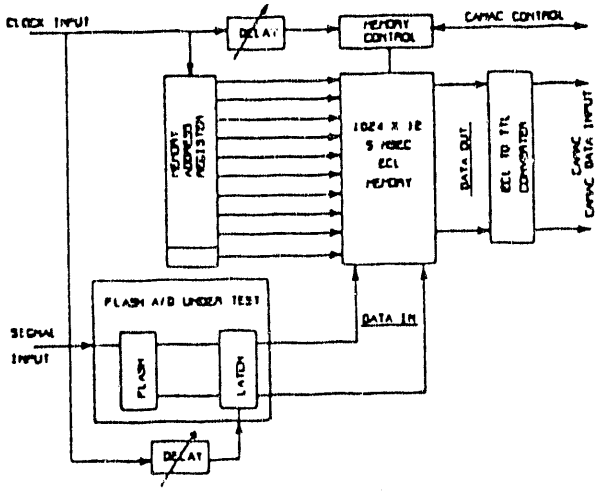

Figure 2 -- Evaluation Board Adapter

The second special board is designed to house an FADC evaluation unit. In some cases these are available from the chip manufacturers and in others we must design our own. This board also contains 1 kilobyte of fast 12 bit memory to store the FADC output prior to reading via CAMAC. A block diagram of this board is given in Figure 2.

B. Software

The test bench software consists of a set of program modules which perform the individual tests. The user interface uses the DEC screen management utility (SMG), permitting access with any standard DEC-supported terminals. Graphic routines are based on the GKS standard and support interactive printing of graphics output on a Postscript printer and interactive storage to GKS metafiles.

Software access to the bus devices attached to the GPIB bus is via a set of routines based on a standard library supplied with the IOtech SCSI/GPIB interface.

Readout and control of the CAMAC is done using routines which emulate a subset of the standard NIM/ESONE CAMAC library.

For a typical test, the user will have one window listing the options available, another listing parameters and the test results, and a third window to display graphical output. Information messages and alarms are displayed on top of these windows.

TEST PROCEDURES

As mentioned above, our tests are based on the IEEE trial standard Std 1057 and we refer the reader to that document for details. In what follows we give a brief description of these tests.

A. Gain and Offset

The gain and offset for a FADC can be measured independently by comparing the output signal to the input signal. We adjust the gain, a multiplicative factor applied to the input signal, and the offset, an additional additive factor applied to the input, so as to minimize the mean squared deviation between the two signals. For an ideal device the gain is 1.000 and there is no offset. A static determination of these quantities is made using a series of programmable dc levels. A dynamic determination is made by using about four cycles of a single sine wave input whose peak-to-peak amplitude covers the input range of the FADC under test.

B. Linearity

The differential and integral nonlinearity also are determined using the programmable dc-level inputs. The differential non-linearity is the normalized difference in the gain corrected measured range of input signals which yield a given output code and the expected, or "ideal", value of this range. The normalization is to the "ideal" value, or "code bin width". The same quantity is also determined using a triangular wave input asynchronous to the clock signal so that all input values are sampled. A perfect FADC has a differential non-linearity of 0.

The integral nonlinearity is computed as the maximum difference between the "ideal" and measured code transitions, after correcting for gain and offset, as a percentage of the full scale output value. We use the dc-level inputs to determine this quantity and a related quantity, the maximum static error. The maximum static

error does not correct for gain and offset in comparing the transition levels and is not reported below.

C. Signal-to-noise and Effective Number of Bits

The sine wave data used to make a dynamic determination of the gain and offset also are used to determine other characteristics of the FADC. The rms noise is obtained from comparing the best fit of the sine wave to the measured data points. The signal-to-noise ratio is the rms signal (peak amplitude/$\sqrt{2}$) divided by the rms noise. The peak error is the largest term contributing to the rms noise divided by three times the sample standard deviation.

The effective number of bits also is determined from this data. This quantity is defined as the number of digitized bits less the $\log_2$ (actual rms error/the "ideal" quantization error) The actual rms error is determined for a given sine wave after gain and offset corrections are applied, The "ideal" quantization error assumes the rms error of a uniform distribution (bin width/$\sqrt{12}$). For an ideal device the number of digitized bits and the effective number of bits are identical.

PRELIMINARY RESULTS

In Table 1, we show the performance characteristics for the three devices mentioned previously. These preliminary results were taken at the one sampling frequency listed for each of the devices.

Flash ADC	AD9002	CXA1176	CX20116
Manufacturer	Analog Devices	Sony	Sony
Advertised Maximum Rate (MSPS)	125	300	110
Clock Rate for Measurements(MHz)	30.0	80.0	20.0
Gain			
Static	0.995	0.994	0.996
Dynamic	0.983	0.989	0.995
Differential Non-Linearity			
Sine Wave	0.300	1.000	0.800
Triangle Wave	0.297	not measured	0.559
Integral Non-Linearity	0.576	0.638	0.333
Signal-to-Noise Ratio	168.1	156.0	202.5
Effective Number of Bits	7.271	6.988	7.405

Table 1 -- Preliminary Results

FUTURE TESTS

In the future we will use multiple sine wave inputs to investigate time base errors and report on the aperture uncertainty and fixed errors in the settling time. Parameters such as analog input bandwidth, settling times, random noise, the word error rates, slew rates, and absolute overvoltage recovery will be given.

We will also present a more thorough summary of results as a function of sampling frequency for a large set of commercially available FADCs. As new devices under development are made available to us, we will test these as well.

Acknowledgement.

This work was supported in part by a Research Development and Exploratory Fund grant by the director of the Ames Laboratory and by the U. S. Department of Energy under contract numbers W-7405-ENG-82-KA and W-7405-ENG-82-KS. Reference to a company or to product names does not imply approval or recommendation of the product by Iowa State University or the U. S. Department of Energy to the exclusion of others that may be suitable.

Notes and References

[1] DEC, SMG, VAXstation, and VMS are licensed trademarks of the Digital Equipment Corporation, Cambridge, Mass.

[2] Jorway Model 73 SCSI Bus Crate Controller.
Jorway Corporation, Westbury, New York.

[3] IOtech SCSI 488/D Bus Controller.
IOtech Inc., Cleveland, Ohio.

[4] Hewlett-Packard Model HP3314A Function Generator.
Hewlett-Packard Corp., Everett, Washington.

[5] Hewlett-Packard Model HP8656B Synthesized Signal Generator.
Hewlett-Packard, Ltd., West Lothian, Scotland.

[6] LeCroy Research Systems Model 9400.
LeCroy Research Systems, Chestnut Ridge, New York.

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