Performance of the ABCN-25 readout chip for the ATLAS Inner Detector Upgrade

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Abstract

We present the test results of the ABCN-25 front end chip implemented in CMOS 0.25 μm technology and optimised for the short, 2.5 cm, silicon strips intended to be used in the upgrade of the ATLAS Inner Detector. We have obtained the full functionality of the readout part, the expected performance of the analogue front-end and the operation of the power control circuits. The performance is evaluated in view of the minimization of the power consumption, as the upgrade detector may contain up to 70 million of channels. System tests with different power distribution schemes proposed for the future tracker detectors are possible with this chip. The ABCN-25 ASIC is now serving as the prototype readout chip in the developments of the modules and staves for the upgrade of the ATLAS Inner Detector.

I. INTRODUCTION

A primary challenge of tracking detectors being developed for the SLHC environment is the high occupancy, which affects directly the granularity of sensors and the number of electronic channels, to be about 10 times higher compared to the present SCT detector. As a result, power consumption in the readout ASICs is one of the most critical issues on top of usual requirements concerning noise and radiation resistance. These requirements have to be considered taking into account present and expected trends in development of industrial CMOS processes. In order to address all these aspects an R&D proposal has been initiated to develop a new ASIC for the ATLAS Silicon Tracker Upgrade [1].

The ABCN-25 ASIC has been designed as a prototype test vehicle for the development of the stave/module readout concepts of the ATLAS tracker upgrade for the SLHC. It has been fabricated in the 0.25 μm CMOS technology from IBM. Reasons for developing the present prototype in the 0.25 μm technology were partially economical. Furthermore we were able to reuse well-known functional blocks, like the memory elements, the bandgap reference or the elements of DAC circuits and complete the design in a relatively short time.

The first critical aspect of the future electronics in the detector concerns the delivery of the power to the nearly 70 million of readout channels, transmission and service devices, which have to be located inside the detector. The constraint is twofold, as it concerns the minimization of the power, and also the reduction in the current. The power dissipated should be limited to less than 70 kW, for the overall silicon strip detector, to comply with the estimated capacity of the cooling system. The supply current has a direct impact on the necessary amount of metallic conductor cross-section to deliver the current, and this amount is actually limited by the available cables existing in the present detector. Various schemes for power distribution, like serial powering of modules or DC-DC step-down converters on the detector, are under investigation in the frame of another R&D project [2]. The ABCN-25 ASIC incorporates two shunt regulator circuits to exercise the serial powering system of the detector modules, as well as a low drop voltage regulator for the front-end supply voltage.

The second critical aspect concerns the readout architecture: the large amount of data generated by modules, will be transmitted off the detector through 4.8 Gb/s optical links [3]. The concentration of data from different modules towards the high throughput optical device requires a readout structure involving a per-module controller and a complex data concentrator/multiplexer at the end of the stave [4].

II. ABCN-25 CHIP MEASUREMENTS

The ABCN-25 architecture follows the concept of binary readout of silicon strip detectors as implemented in ABCD3T ASIC [5]. It comprises 128 channels of preamplifier, shaper and comparator circuits with two memory banks, one used as a pipeline for the trigger latency and another one used as a derandomizing buffer. The front-end has been optimised for 2.5 to 5 pF detector capacitance (2.5 cm long silicon strip detector) and it is compatible with either detector signal polarity. The shaper is designed for 25 ns peaking time providing double pulse resolution of 75 ns.

The chips have been mounted on different boards and prototype hybrids [6], and tested through 2 test systems: one, called the SCT-DAQ, is the custom designed hardware and software developed for the tests of the SCT detector modules actually installed in the detector, the other one, called NI-DAQ, allows performing equivalent tests but is a new solution based on a VXI-NI crate, commercial data acquisition board and the LabVIEW software [7].

A. Front-End

The design specifications of the analogue front-end is summarized in Table 1. There are two parameters, which drive the design of the front-end, namely the ENC be below 750 el. rms and the power dissipation be below 0.7 mW per channel.

Let us note that after heavy radiation damage in the SLHC environment the expected signal from the silicon strip detectors is about a half of that available in the present SCT detectors. Therefore the ENC is required be significantly lower, below 750 el. rms, compared to 1500 el. rms in the present detector.

Main Analogue FE Specs	
Gain at the discriminator input:	100 mV/fC for the nominal bias currents and the nominal process parameters
Effective gain extracted from the response curve:	90 mV/fC for the nominal bias currents and the nominal process parameters
Linearity:	better than 3% in the range 0 – ±6 fC
Time walk	<15 ns 1.25 –10 fC @ 1 fC threshold
Noise:	<= 750 electrons rms for irradiated module
Max Parasitic Leakage Current:	200 nA DC per channel with < 10% change in gain at 1 fC
Power	700 μW (optimised for short strips)

Table 1: Main specifications for the ABCN-25 front-end.

The noise figures of the front-end have been measured on a test board with a specific "clean" printed circuit board layout in front of the channel input pads to minimize the tracks parasitic capacitance and remove any crosstalk from digital signals or power lines. Small SMD type capacitors can be added on 2 channels to perform the measurement of the noise versus the input capacitance. The measurement results are summarized in Figure 1: the measurements were made on two different chips, one set (J) reporting values from zero external capacitance to 5.6 pF, with different bias currents of the input transistor. For the other set (M) the capacitance at the input has been extended up to 15.8 pF. For short strips the expected strip capacitance should not exceed 2.5 pF. For long strips it should be in the range of 10 pF. The measurement at 2.3 pF shows a noise of ~580 electron rms at nominal bias current of 140 μA. At high bias current (198 μA) the noise for 10.8 pF is at ~1100 electron rms. This measurements demonstrate that, although the design has been optimised for the short strips it provides also satisfactory performance for long strips by increasing the bias current in the input transistor and so in expense of additional power dissipation.

The black dots in Figure 1 correspond to noise measurements made with the chips mounted on one of the first hybrid prototypes equipped with 20 ABCN-25 chips and connected to detector strips of 1 cm, 2.5 cm, 5 cm and 7.5 cm. They show a higher noise than with discrete capacitance, for strips length higher than 2.5cm. The noise deviation above the 2.5cm strip length should be reviewed when more advanced versions of the hybrids will be tested.
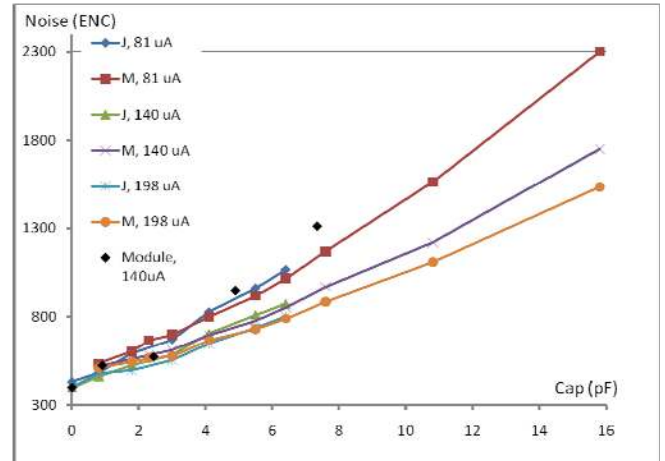

Figure 1: Measured noise figures of the ABCN-25 readout chip. Two sets of measurements (M and J), with different bias currents in the input transistor are shown.

For comparison, the noise figures from simulation with close conditions to the test (bias, temperature) are plotted in Figure 2. The expected noise at 3 pF capacitance is just below 600 el. rms for drain current in the input transistor of 140 μA, matching well with the above measurements. We have obtained 580 el. rms for 2.3 pF test capacitance, to which a parasitic value of 0.5-0.8 pF should be added, due to stray capacitances on the printed circuit board.
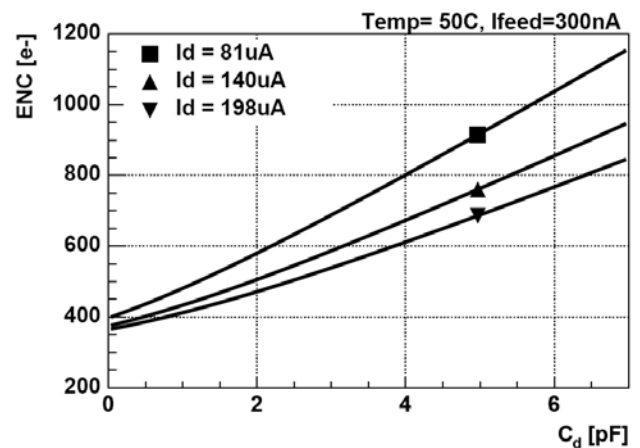

Figure 2: Simulated noise figures for the front-end.

The gain has been measured by performing threshold scans for three different values of the input charge, namely 1.5, 2.0 and 2.5 fC. The input charge is applied simultaneously to ¼ of the channels, through a charge injection circuit present on the ABCN-25 front-end. The measurements are repeated 4 times to scan all channels. The plots in Figures 3 shows the excellent uniformity across the channels, with an average value of 97 mV and a deviation of less than 1%.
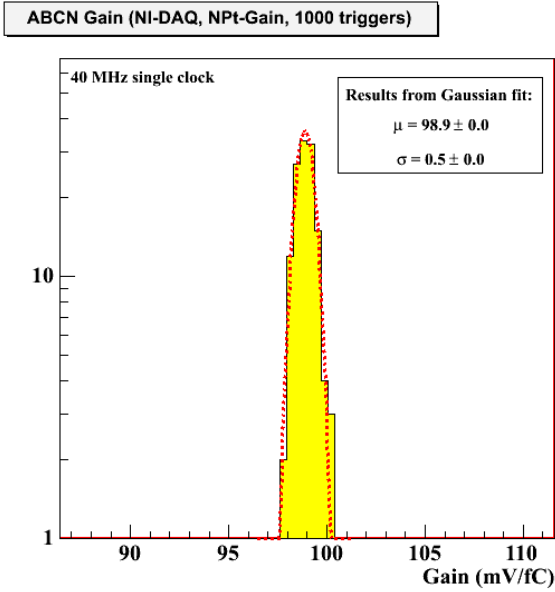
Figure 3: Gain histogram over one ABCN-25 chip.

The linearity is estimated from the threshold scan measurements at charges up to 10 fC. The plot on Figure 4 shows the maximum deviations from a linear fit for 128 channels. The measurements include the factors of non-linearity of the front-end preamplifier and shaping stages as well as the dependence of the minimum discriminator overdrive on the threshold level.
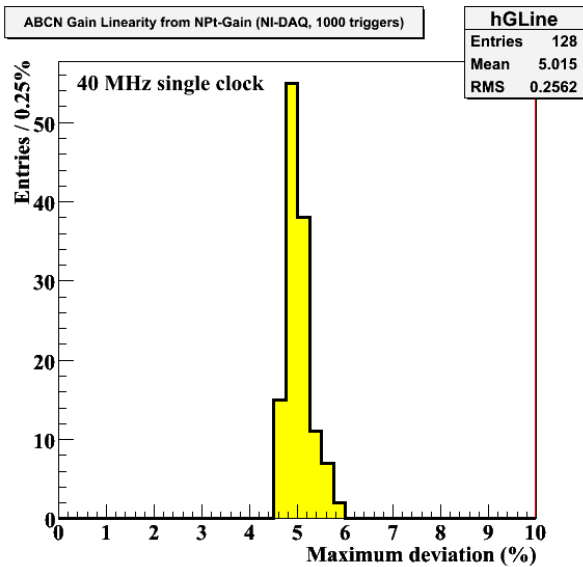

Figure 4: Linearity measurement, maximum deviation from a linear fit from 1.5 fC to 10 fC for 128 channels of the same chip.

The time walk is measured from the signal detection efficiency versus the injection pulse delay scans, related to a clock reference, for signal charges of 1.25 fC to 10 fC and a threshold fixed at 1.0 fC. The plot in Figure 5 presents the result as the position of the leading edge of the discriminator output versus the fixed clock reference. The measured time walk is within 15 ns for the nominal conditions.
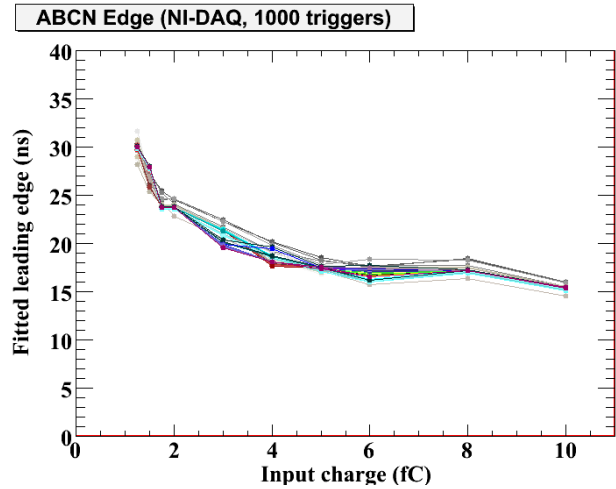

Figure 5: Time walk measurements on the 128 channels of ABCN-25 chip.
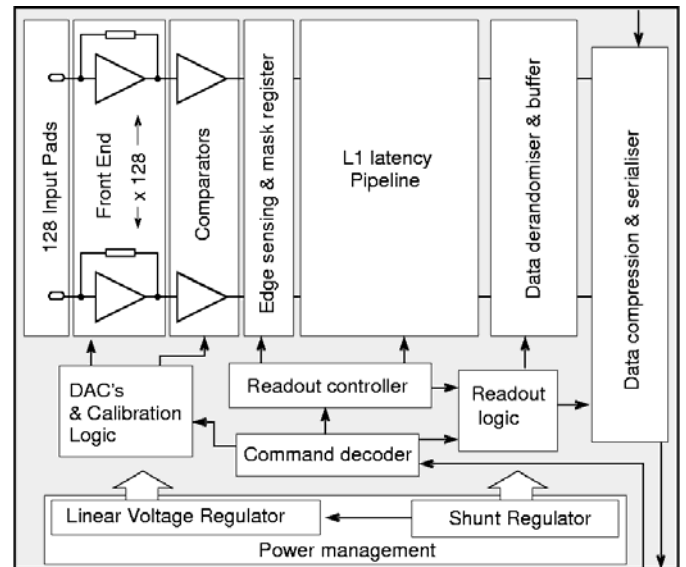
B. Digital

Figure 6: ABCN-25 functional block diagram.

Beyond the front-end part, the ABCN-25 contains the logic functions to perform the processing of the binary data obtained after the discriminators outputs. The block diagram of the ABCN-25 ASIC including the logical function is shown in Figure 6. The pipeline is made of a 128×256 addressable static RAM, storing the data for 6.4 μs. After a L1 signal is received, the data corresponding to 3 bunch crossings (BC) is transferred to the local data derandomizer. It is made of one 128×128 addressable static RAM, allowing to store up to 43 L1 events. The most complex part of the logic is the data compression module. This function scans in a few clock cycles the hit information contained in one event (including data from 3 BC) of the derandomizer and generates the 7 bit channel number and the 3 bit data for each channel which matches a preselectable data pattern. The 10 bits per each valid hit are buffered and are available for transmission.

The data transmission is initiated by either the L1 signal (master mode) or the reception of a token signal (slave mode). The mechanism is such that when a token is received, the ABCN-25 transmits its data to one adjacent ABCN-25 chip and then issues a token. In this way the data from the same event are appended by passing from a chip to the next one (up to 20 in case of the "short" strips hybrids) up to the last chip in the data chain, set in the "master" mode. This last chip analyses the data flow, generates a header and terminates the transmission of the event. There are multiple logical mechanisms involved, which make this part of the circuit rather costly in term of the number of gates and consequently the power. One feature for example is that the data flow mechanism can be fully reversed, to have a redundant possibility of sending data.

The current consumption versus supply voltage of the ABCN-25 digital part is plotted in Figure 7. It should be noted that below 1.7 V the current supplying the chip is not anymore coming from the power source, but rather from the I/O ports. The chip is functional for power supply voltage as low as 1.3 V. The static current in the digital part is 48 mA at 2.5 V. This current is about 30 mA higher than the expected value. Further investigations are needed and will be perform to identify the sources of this excess of current. The switching current (the one scaling with the frequency) is 92 mA at 2.5 V and clock frequency of 40 MHz.
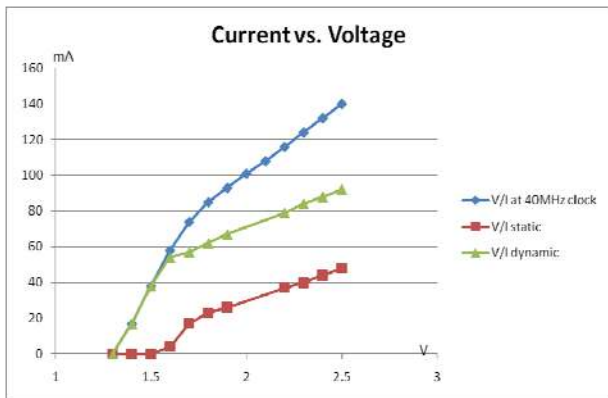

Figure 7: ABCN-25 digital current versus voltage supply.

During the design phase, control bits were added to activate or deactivate the clocking on some functional blocks of the chip, to measure the dynamic current related to these functions. The dynamic currents taken by the different functions, measured by controlling these bits are shown in Table 2.

PIPE-STOP interrupts the clock of the main pipeline block, made of the 128×256 RAM cells, the R/W addressing circuit, and the Built-in Self Test circuit. REG_STOP affects the correcting mechanism of the triple redundant registers. There are 8 such registers in this circuit, built in such a way that one bit corruption due to a Single-Event-Upset (SEU) is detected and corrected. This functionality requires continuous running of the local clock. The REG_STOP bit interrupts this clock and consequently the SEU correction mechanism is not

active. The CD_STOP interrupts the clock on the command decoder circuitry, which executes the non critical commands, like the R/W operation of the biasing registers. The column "Readout clock STOP" of Table 2 indicates the possibility to not apply the clock to the data serializer (this clock may run at either 40 or 80 MHz in normal condition).

Mode	I digital	Reduction	%
Normal	92 mA		
PIPE-STOP	72 mA	20 mA	22%
REG_STOP	87 mA	5 mA	5.5%
CD_STOP	87 mA	5 mA	5.5%
Readout clock STOP	87 mA	5 mA	5.5%
All STOPS	57 mA	35 mA	38.5%

Table 2: Digital supply current measurement for various digital functions deactivated.

The last column resumes the current left if all the STOPS are applied. The remaining dynamic current (57 mA, 61.5% of the total current) is taken by the derandomizer, the large compression logic circuitry, and the readout controller. These measurements show that a significant amount of the dynamic current is taken by the data compression and readout logic parts. In this realization, these two parts are not designed with specific SEU error detection and/or correction mechanisms. Implementing the SEU detection and correction in this functional blocks in the future will increase further the amount of current. A careful optimisation, possibly simplification, of the readout mechanism should be considered to limit the power consumption in the digital parts.

III. SHUNT REGULATORS

Serial powering of detector modules is one of the possible option to the power distribution problem, however, it introduces new aspects that have to be addressed in the front-end ASIC. The scheme requires that each module, comprising 20 to 40 ABCN ASICs, depending on the module design, have to be powered through a shunt regulator. The shunt regulator can be either an external device, one per hybrid, or can be a distributed structure, i.e. each ASIC contains a shunt regulator, which are then connected in parallel on the hybrid.

The ABCN design comprises two prototypes of distributed shunt regulator circuits, which can be used alternatively. One circuit is a full shunt regulator. Another circuit comprises only shunt transistors, with gate control inputs, which are foreseen to be driven by an external voltage control loop, common for all ASICs connected in parallel on the hybrid.

A. *Internal Distributed Shunt Device*

The conceptual schematic diagram of the developed shunt regulator suitable for connecting several shunt regulators in parallel on the hybrid is shown in Figure 8. The circuit monitors the current flowing through the shunt transistor and compares with 6 preset reference currents. If the shunt current exceeds a given reference current the reference voltage and so the output voltage of the regulator is adjusted. In this mechanism the output voltages of several shunt regulators connected in parallel are adjusted to a common level.
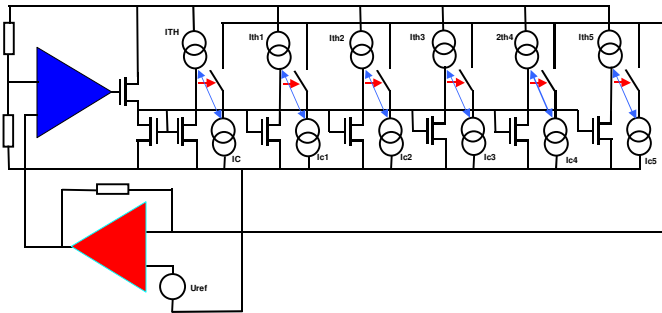
Figure 8: Conceptual schematic diagram of the shunt regulator with auxiliary correction amplifier.

The effectiveness of this circuit has been verified on a dedicated test board on which 4 ABCN-25 chips are powered, activated and transmitting data. Current monitors are added in the power distribution lines to measure the current of each ABCN-25 individually, whereas the power source is set in the current source mode.
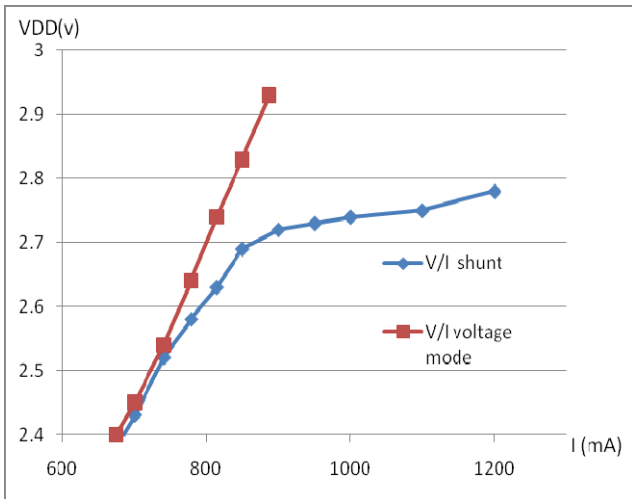

Figure 9: Voltage versus current on the 4 ABCN-25 test board. Squares : V versus I with the power supply set as a voltage source. Diamonds: V versus I with the internal shunt enabled, and the power supply as a current source.

In Figure 9, the voltage shunt operation with the 4 internal shunt devices in parallel is demonstrated, with the test board equipped with 4 ABCN-25. The voltage is limited below 2.8 V when the current on the board is forced well above the nominal current of 800 mA at 2.7 V.
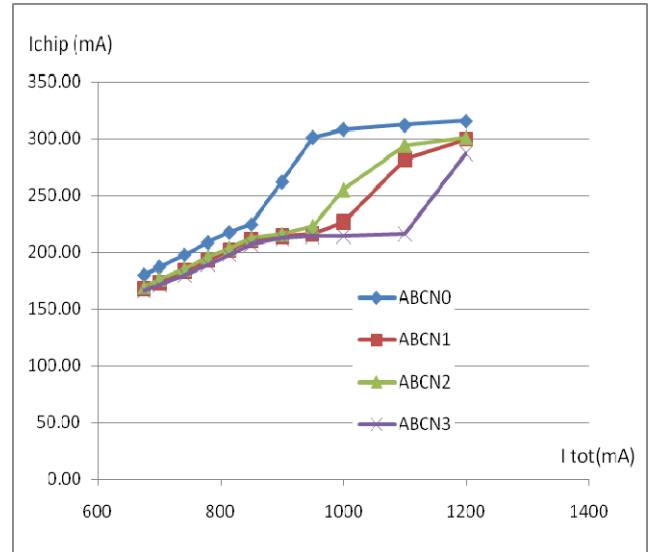

Figure 10: Current distribution per ABCN-25 chip versus total current, internal shunt enabled.

The additional current is derived through the shunt elements, as shown on Figure 10. The currents per each ABCN-25 are showing the expected behaviour: looking to the chip ABCN0, the current in the shunt device is increasing according to the source current, then it gets limited to approximately 80 mA. When increasing the source current, the excess current is passing through the shunt devices of ABCN2 and ABCN1, up to the same limit of around 80 mA, finally it gets through the shunt device of ABCN3.

B. *Shunt Device with external control*

The schematic diagram of the distributed shunt devices with an external feedback control is shown in Figure 11. The external shunt control line drives in parallel the shunt elements distributed in chips.
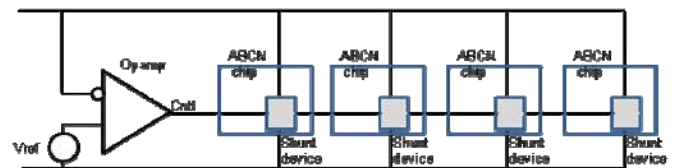

Figure 11: Conceptual schematic diagram of the shunt regulator with auxiliary correction amplifier.

In Figure 12, the voltage shunt operation with the 4 shunt devices in parallel is shown, with the test board equipped with 4 ABCN-25. The voltage is limited slightly below 2.5 V when the current on the board is forced above the nominal current of 700 mA at 2.45 V.

The additional current is derived through the shunt elements, as shown on Figure 13. The current in excess is reasonably distributed across each ABCN-25 shunt device. As expected, the degenerated current mirror circuit controlling the gate of the large shunt transistor helps to limit the difference of current, which may result from different transistor

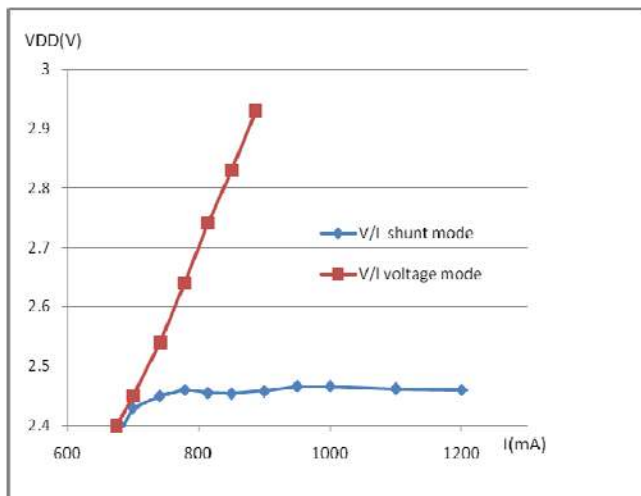parameters. It avoids that one chip takes the majority of the excess current.

Figure 12: Voltage versus current on the 4 ABCN-25 test board. Squares : V versus I with the power supply set as a voltage source. Diamonds : V versus I with the distributed shunt enabled, and the power supply set as a current source.
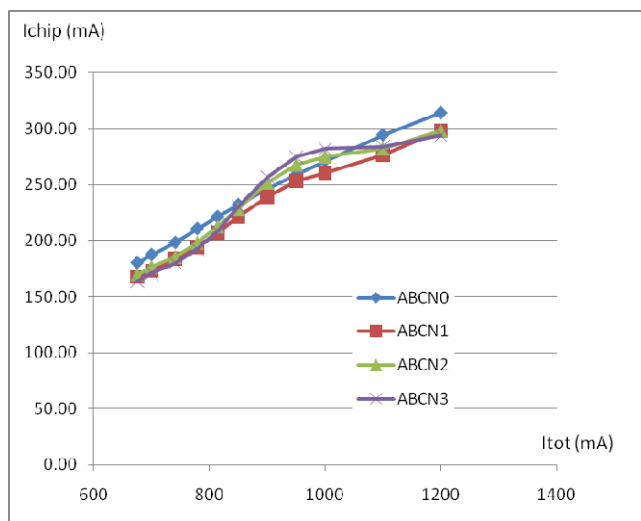

Figure 13: Current distribution per ABCN-25 chip versus total current, distributed shunt enabled.

IV. PERSPECTIVE FOR THE ABCN CIRCUIT IN 130 NM PROCESS

The ABCN-25 power measurements demonstrate that, with this readout architecture, the digital power dominates the analogue power, by a factor of approximately 3 to 4. A number of parameters contribute this large factor, which can be reviewed in the case of transferring the same functionality to a 130 nm technology.

Because the digital power supplies the on-chip LDO voltage regulator delivering the 2.2 V required by the analogue front-end, the supply voltage for the digital part is fixed at 2.5 V. With this arrangement it is not possible to operate the

ABCN-25 chip at lower voltage supply in the prototype hybrids, to take advantage of the resulting reduction in the power consumption of the digital part (the dynamic power scales with the power of 2 of the voltage).

With a 130 nm technology, the voltage applied to the digital part could be as low as 1 V or 0.9 V (observing that our speed requirement of 40 to 160 MHz for the readout is far away from the limits imposed by the technology). Simulations have shown that a factor 6 in power reduction is possible, cumulating the effects of voltage reduction and standard layout techniques, which were not applicable in the 250 nm technology because of radiation dose tolerance. The estimates show that reduction of digital supply current down to 56 mA (56 mW power) is possible. The analogue front-end will require still 1.2 V voltage source supply. The consequence of such choices (1.0 V or below for digital, 1.2 V for analogue) has to be considered in the framework of the discussions on the power distribution to the ASICs.

V. ACKNOWLEDGEMENTS

VI. REFERENCES

[1] F. Anghinolfi, W. Dabrowski, Proposal to develop ABC-Next, a readout ASIC for the S-ATLAS Silicon Tracker Module Design. https://edms.cern.ch/document/722486/1

[2] M. Weber, Research and Development of Power Distribution Schemes for the ATLAS Silicon Tracker Upgrade. https://edms.cern.ch/document/828970/1

[3] P. Moreira, The GBT project, in these proceedings.

[4] P. Farthouat, A. Grillo, Read-out Electronics for the ATLAS upgraded tracker. https://edms.cern.ch/document/781398/1

[5] F. Campabadal et al., Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracker. Nucl. Instr. and Meth. A. 2005,vol. 552, pp. 292–328.

[6] A. Greenall, Prototype flex hybrid and module designs for the ATLAS Inner Detector Upgrade utilising the ABCN-25 readout chip and Hamamatsu large area Silicon sensors

[7] M. Dwuznik, S. Gonzalez Sevilla, Replacing full custom DAQ test system by COTS DAQ components on example of ATLAS SCT readout, in these proceedings.