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SUPPLEMENTS

Performance of the Binary Silicon System for ATLAS

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We report on the results from a beam test of a binary silicon strip system proposed for ATLAS. The data were collected during the H8 beam test at CERN in 1995 and at a beam test at KEK in 1996. The binary modules tested had been assembled from silicon micro-strip detectors of different layout and from front-end electronics chips of different architecture. The efficiency, noise occupancy, and position resolution were determined as a function of the threshold setting for various bias voltages and angles of incidence. Interstrip effects were also evaluated using a high resolution telescope. The performance of a prototype detector module irradiated to a fluence of 1.2×10^{14}p/cm^2 is also characterized.

1. Introduction

We are proposing to simplify the readout of silicon detectors in the Semiconductor Tracking Detector (SCT) [1] of ATLAS [2] by using a binary readout [3], which records only the addresses of strips with pulse height exceeding a preset threshold value. Thus the pulse height is not directly available during data taking. It has been shown [4,5] that the distribution of pulse heights can be recovered by varying the threshold and measuring the counting rate, which is the integral of the pulse height spectrum. Likewise, the noise

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can be determined from threshold scans without beams. It is important to note that the primary parameters of interest for a tracking device are not the signal and noise, but the single channel efficiency and position resolution, and the noise occupancy.

Basic requirements on a binary silicon system for ATLAS include the ability to operate at the LHC bunch crossing rate of 40 MHz, the ability to sustain estimated total fluences of 10^{14}p/cm^2, and a point resolution of about 20 microns. These requirements translate to maximum noise occupancies of approximately 10^{-3} per channel and a high efficiency (>99%).

In the following, we report on the results from the 1995 ATLAS beam test [6,7] in the H8 beamline in the CERN North Area. We also report on the results of a beam test [8] carried out at KEK in 1996. Previous beam tests at KEK [5] have shown low noise occupancy at the nominal threshold of 1 fC and good efficiency, even at higher thresholds. In the H8 beamtest, the use of a beam telescope with a resolution of a few microns allowed the investigation of the efficiency at a fine scale as a function of the interstrip distance.

2. Beam Test Setup

During the 1995 H8 beam test, several silicon micro-strip modules with binary readout were tested. Fig. 1 shows the schematic of the setup during the September run: the x-y beam telescopes bracketed the binary modules, and allowed the determination of the location of tracks in the modules to within 2-3 microns in the horizontal and the vertical directions. Two of the binary modules, called UCSC and DDR2, were held fixed, while the central one, called ATT3, was mounted on a rotary stage and could be rotated about an axis parallel to the strips. The distance between the x-y hodoscope planes was about 80cm and the distance between the binary modules was about 5cm. The setup at KEK was similar, with the exception that the beam telescope consisted of anchored binary modules.

Table 1 lists the detector modules used in the CERN and KEK beam tests. All modules are so-called "r-ϕ" modules, where the detector strips

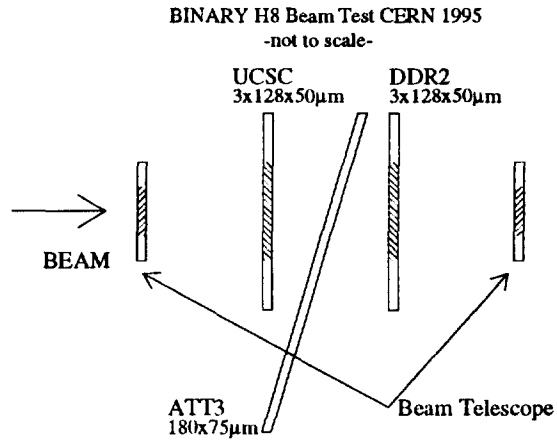

Figure 1. Schematic of the beam test setup.

are directly bonded to the front-end electronics (FEE). In addition, the hybrid, which carries the FEE and the data and control signals, is mounted across the detector strips in the approximate center of the 12cm silicon detector module.

The modules combined SSC-style and more recently developed LHC-style detectors with different FEE. Two bipolar amplifier-comparator chips ("LBIC" and "CAFE") with peaking time of close to 20ns were used. The LBIC [9] was developed for AC-coupled SSC detectors, while the CAFE [10] chip was designed for operation with finite input current for use with ATLAS DC-coupled detectors. Two CMOS digital pipelines were used, the CDP128 [11], a clock-driven binary pipeline, and the DDR2 [12], a data-driven binary pipeline with data compression and data transmission protocol similar to the ATLAS protocol.

The silicon detectors tested were AC-coupled double-sided detectors [13] with 50μm pitch developed in Japan for the SSC and DC-coupled ATLAS-type 75μm pitch detectors [14] fabricated at LBNL. Both Kapton flex-circuit and ceramic hybrids were used.

The readout, newly developed for this test, is based on Digital Signal Processors (DSP's) utilizing a 40 MHz clock and designed to allow a data

Table 1
Binary micro-strip detector modules under test.

Module	Hybrid	Provider	side,bulk,coupling	Chip	Test
UCSC	Kapton	Hamamatsu	n-on-n AC	LBIC	H8-95
DDR2	Kapton	Hamamatsu	p-on-n AC	LBIC	H8-95
ATT3	Ceramic	LBL	n-on-p DC	CAFE	H8-95
ATT2	Ceramic	LBL	p-on-n DC	CAFE	KEK-96
ATT4	Ceramic	Hamamatsu	n-on-n AC	CAFE	KEK-96
UCSC2	Kapton	Hamamatsu	n-on-n AC	LBIC	KEK-96

rate of several kHz.

In addition to rotation scans, two parameters were varied to map out the detector performance: the detector bias voltage ($V_{\rm bias}$) and the threshold voltage of the on-chip comparators ($Q_{\rm thr}$). The results from the threshold scans were used to determine the pulse height spectrum. The data at different rotation angles helped us to understand the effects of finite track crossing angles.

3. Noise Occupancy

The noise occupancy was measured as a function of the threshold voltage to determine the *rms* noise. This was done before and after the run using the full DAQ. Channels which were obviously noisy were removed from the data. The occupancy per channel as a function of $Q^2_{\rm thr}$ is shown in Fig. 2. Since neither of the pipelines are edge-sensing and since the comparator chips have different output widths, the occupancy data have been corrected for the number of effective time slices sensed by the pipeline.

The occupancies are approximate Gaussian functions of the threshold voltage. The slope is a measure of the noise variance. We observe the expected dependence of the noise on the strip length (12cm vs 6cm). Extrapolating the noise occupancies to $Q_{\rm thr}$=1 fC gives a noise occupancy of $0.8 \times 10^{-4}(\sigma_{\rm n} \approx 1640e^-)$ for the ATT3 module and $1.5 \times 10^{-4}(\sigma_{\rm n} \approx 1706e^-)$ for the UCSC module. After the H8 test, it was discovered that the CAFE chips were operated at a non-optimal power setting. Subsequent measurements at the KEK testbeam revealed a noise occupancy (at the nominal $Q_{\rm thr}$=1 fC) of $< 10^{-5}$.

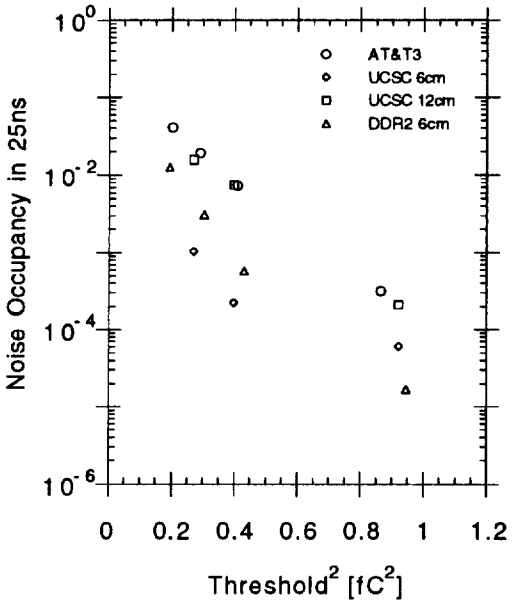

Figure 2. The average single-strip occupancy as a function of $Q^2_{\rm thr}$.

4. Data Analysis

After aligning each module with the tracking program, only events with one "good" track were analyzed. Good tracks were defined as tracks with a χ^2 probability P_{χ^2} >1% which intercept the fiducial region of a detector module.

Clusters were formed by joining adjacent hit strips up to ±2 strips away from the expected track impact point. The cluster position was assigned to the geometric center of the cluster. Events with clusters close to known noisy or dead

strips were rejected. The surviving events were then used in the efficiency and resolution measurements.

5. Results

5.1. Efficiency vs. Interstrip Position

The efficiency for the p-side detector read out with the DDR2 chip is shown in Fig. 3 as a function of the interstrip position. The interstrip position is calculated as the crossing point of a track in the detector in one unit of strip pitch. It is defined such that the strip-to-strip boundary is centered at 0.5.

As expected, as $Q_{\rm thr}$ is increased, the efficiency starts to degrade at the strip edges. This is due to a reduction in the effective pulse height due to charge sharing between strips. Nevertheless, at the nominal operating threshold ($Q_{\rm thr}$=1 fC), the efficiency is well over 99% at the strip edge. The overall efficiency is also > 99% at a $Q_{\rm thr}$ 40% higher than nominal. It is 50% close to 3.5 fC, the median of the binary Landau distribution. Fig. 4

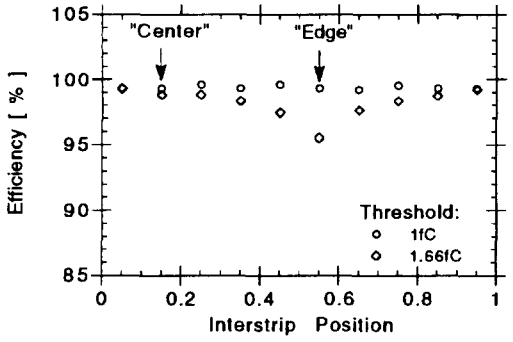

Figure 3. The efficiency as a function of the track intercept across a strip, in units of strip pitch. The strip-strip boundary is at 0.5 pitch units.

shows the *rms* resolution at $Q_{\rm thr}$=1 fC for multi-hit clusters and for all clusters in the DDR2 module. An improvement in the resolution due to charge sharing is evident, but the usefulness of charge sharing in a binary system is limited to the edge of the strips, where tracks tend to form multi-hit clusters.

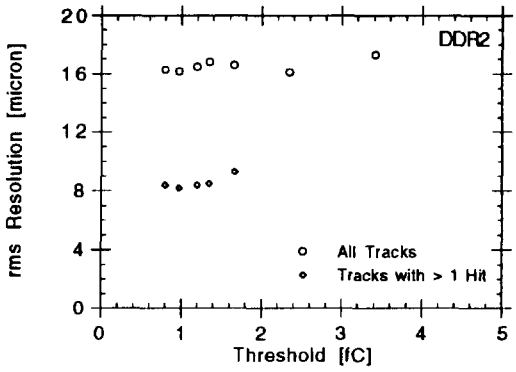

Figure 4. The position resolution vs. $Q_{\rm thr}$ for multi-hit clusters and for all clusters.

5.2. Efficiency and Resolution vs. $V_{\rm bias}$

Since n-on-n detectors deplete from the backside, the collection of charge might be less efficient at lower bias voltages than at higher ones. The UCSC module depletes at about 70V. This module was operated at a $V_{\rm bias}$ of 100V and 200V. The efficiency was found to be close to 100% around the nominal $Q_{\rm thr}$ of 1 fC and to have a median of 3.5 fC, confirming earlier testbeam results [4,5].

Fig. 5 compares the efficiencies at the edge of the strips at the two bias voltages . The strip edges are expected to be more sensitive to the increase in charge collection efficiencies due to higher $V_{\rm bias}$. In fact, the data are virtually identical at the nominal threshold of 1 fC and it is only at 1.7 fC that there is a noticeable effect.

5.3. Dependence on Rotation Angle

The data of the ATT3 module were taken at constant $V_{\rm bias}$ but at varying rotation angle. The n-on-p detector has a depletion voltage ($V_{\rm depl}$) of about 140V, and was operated at close to 80V due to limitations in one of the power supplies. With the junction on the n side, this mode of operation corresponds to an inverted n-on-n detector operated at partial depletion, which is an option

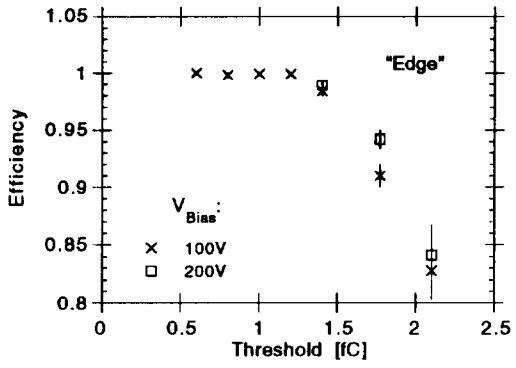

Figure 5. The efficiency as a function of Q_{thr} for tracks crossing between the strip edges.

for the ATLAS SCT in case of unexpectedly high radiation levels.

Fig. 6 shows the *rms* resolution and the hit multiplicity for three rotation angles at Q_{thr}=1 fC. Due to increased charge sharing, the mean pulse height, i.e. the Q_{thr} value at the median of the efficiency curve, decreases as the rotation angle increases. This, in turn, increases the charge multiplicity and improves the resolution. However, the efficiency is well above 99% for thresholds below 1.2 fC and for all rotation angles.

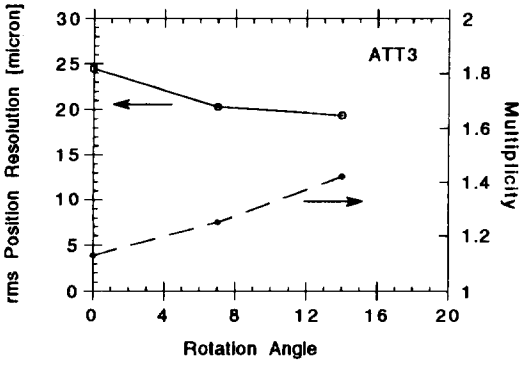

Figure 6. The position resolution and the hit multiplicity as a function of the track angle of incidence (in degrees).

5.4. Irradiation Studies

One of the modules tested during the KEK testbeam in 1996 (ATT4 module) had been irradiated to a fluence of 1.2×10^{14}protons/cm^2 (at 12 GeV). Unfortunately, some of the post-irradiation history of the module included unwanted warm-up periods resulting in a full depletion voltage higher than planned ($\approx$ 280V). Fig. 7 shows the noise occupancy vs. efficiency curves for the irradiated modules at V_{bias}= V_{depl} and at V_{bias}=55%V_{depl}. At approximately full-depletion voltage and Q_{thr}=1 fC, the efficiency is over 99% and the noise occupancy is slightly above 10^{-4}. At approximately half of full-depletion voltage, the efficiency drops only to 96%.

Fig. 8 shows the mean pulse height (MPH) as a function of the bias voltage for the irradiated and the non-irradiated modules. It is interesting to note that, even though there is a noticeable degradation in the MPH for the irradiated module, the MPH is safely above the nominal operating threshold of 1 fC. This may provide a reasonable safety margin (or "headroom"), in terms of efficiency and noise, in order to operate in the LHC environment.

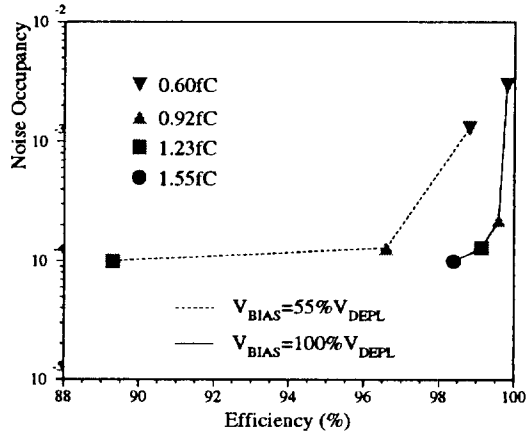

Figure 7. Noise occupancy vs. efficiency for the irradiated ATT4 module.

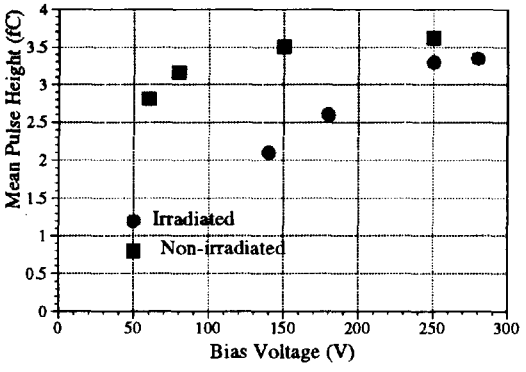

Figure 8. The MPH as a function of V_{bias}.

6. Discussion and Conclusion

Beam tests performed with various detector modules using a binary readout show that such a system may provide reasonable performance in the LHC environment. The KEK and CERN beam tests presented here included studies of efficiency, noise occupancy, incidence angle, and interstrip effects on various detector modules and using different architectures. At the nominal operating threshold of 1 fC, good efficiency was found for tracks inclined up to 14 degrees. The efficiency of n-side on n-bulk detectors was found to have a marginal dependence on V_{bias} once the detector is depleted. Furthermore, an irradiated n-on-n detector, operating at about and well below its depletion voltage had just a moderate degradation in performance.

From these data, it can be concluded that a realistic silicon strip binary system could have a headroom of 20-50% in Q_{thr} for an efficiency $>$ 99% and a noise occupancy of $\approx 10^{-4}$.

The ATLAS binary beamtest program, for the past two years, has been focused in proving the feasibility of such a system in the LHC environment. Now the focus has shifted [15] to providing the final performance parameters in preparation for a final technology choice within the ATLAS Collaboration.

7. Acknowledgents

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