Performance Optimization of Broadwell-Y Shaped Transistor using Artificial Neural Network and Moth-Flame Optimization Technique

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ABSTRACT:
FinFETs are the emerging 3D-transistor structures due to strong electrostatic control of active channel by gate from more than one side which was not possible in conventional transistor. FinFET structures with rectangular and trapezoidal shape have been excessively analyzed in literature. The main purpose of this work is to present a FinFET structure with such a compact fin shape that the gate has high controllability over it; and thus reduced short channel effects in comparison to existing structures. Here, FinFET with Broadwell-Y shape, proposed by Intel has been designed and its short channel effects were analysed. Simulations of the designed FinFET have been performed in Technology Computer Aided Design (TCAD) tool. Performance of broadwell-Y shaped FinFET was compared with the existing rectangular and trapezoidal structures for the same input design parameters and it was noticed that Broadwell-Y shaped FinFET outperformed the last two structures in terms of short channel effects. Then the performance of the designed device was optimized using Moth Flame Optimization (MFO) after the network was trained through Artificial Neural Network (ANN). Results obtained from MATLAB were in close agreement with those obtained from TCAD simulations. Output parameters like leakage current (I_{OFF}) of 2.407e-12A, On-Off current ratio (I_{ON}/I_{OFF}) of 4.5e06, Subthreshold Swing (*SS*) of 65.4mV/dec and Drain Induced Barrier Lowering (*DIBL*) of 37.9mV/V were obtained after optimization. Short channel effects are improved for 20nm gate length as SS is close to ideal value 60mV/dec and DIBL is below 100mV/V which makes this designed structure a good option for applications at nanoscale.

KEYWORDS: FinFET, Moth-Flame Optimization (MFO), Artificial Neural Network (ANN), Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Leakage current, TCAD, MATLAB, Fin height, Gate length.

1. INTRODUCTION

To increase the density of transistors and minimize the area requirements over the integrated chip, downscaling of conventional transistors is essential [1]. Reducing the gate length in MOSFETs influences the performance in adverse way as short channel effects (SCEs) become dominant [2]. These SCEs are required to be reduced in order to enhance device performance. Variations in the design and material properties of basic MOS transistor were suggested by researchers to improve its performance in analog and digital circuits for lower technology nodes [3-18]. Dual-gate MOS transistors built on insulator substrate were the successors to the existing single gate devices. These devices were capable of controlling drain current in an effective way and hence, lessening SCEs [3-5].

Then, device with single gate but covering the channel from three sides was created to avoid misalignment of multi-gates with respect to each other. This self-aligned device, named as FinFET was advantageous in terms of reduction of SCEs like Threshold voltage (V_{th}) - roll off, DIBL and SS etc. below 32nm technology node and also fabrication was easy using conventional process technologies [6]. Process parameters like fin width, fin height, gate length, gate oxide thickness, gate work function, source/drain and fin doping etc. decide FinFET performance [7-10]. FinFET with rectangular fin shape

is shown in Figure 1. Fin width has to be kept below 2/3 of gate length for reduced SCEs. Earlier used SiO_2 gate dielectric was replaced by high-k materials like HfO_2 and ZrO_2 because of the fact that high-k dielectrics allow for increased gate capacitance and simultaneously decreased gate tunneling leakage current, thereby improving device performance whereas low-k oxides have 100 times more leakage current and comparatively reduced gate capacitance [11]. Dopant atoms increase the mobility of charge carriers, but excessive channel doping can cause random dopant fluctuations (RDF) in the structure and shifts the threshold voltage [12].

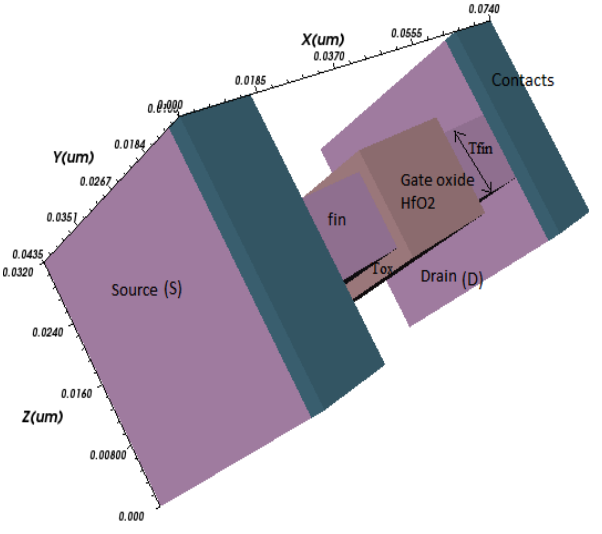
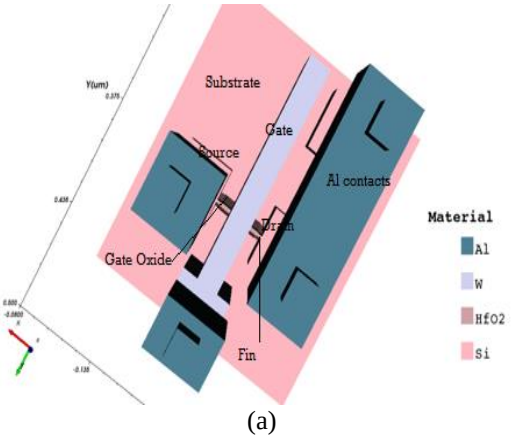


Fig. 1. Rectangular FinFET [13].

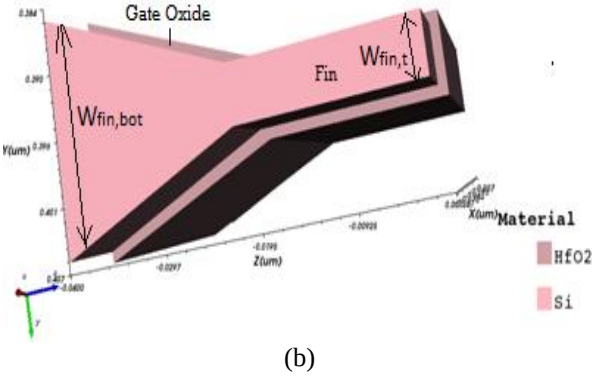
After the rectangular FinFET structures were fabricated, Intel noticed from SEM view that rectangular transistors are actually tapered in shape i.e. have non-vertical sidewalls [14]. Lot of research has been done on these tapered i.e. trapezoidal transistor structures. Improvement in performance and reduction in SCEs was investigated. Top fin width was dependent on fin inclination angle [15-17]. Further, broadwell-Y shaped transistors were suggested by Intel over trapezoidal transistors because of sub-optimal output of latter [18]. FinFET technology is being adopted by the leading semiconductor companies like Intel, IBM, TSMC and Global Foundries for their latest processors because of its numerous advantages. Therefore, obtaining an optimum performance becomes imperative for FinFETs [14], [19-21]. For optimized performance, a number of swarm based algorithms have been discussed in the literature like Particle Swarm Optimization (PSO), Artificial Bee Colony (ABC), Bat Algorithm (BA), Firefly Algorithm (FA), Cuckoo Search (CS) algorithm etc. [22-26]. These algorithms have been applied in various engineering fields [27-31]. One such algorithm has been applied in this work; Moth-Flame Optimization (MFO). It was proposed by Mirjalili in 2015 where moths take the guidance from moonlight to fly in the straight line path. In actual, these fancy insects get distracted from their straight line path and follow spiral path as they try to make fixed angle with artificial lights. The best positions obtained by moths called flame is updated for each moth after every iteration and moths sort themselves to fly around the best flame, thus never lose their best positions obtained so far and update their fitness values. The unique feature of MFO is that the adaptive convergence towards flame causes fast exploitation about the flames and assigning separate flame to every individual moth avoids trapping in local minima. Thus, MFO is able to balance both exploration and exploitation properties very well [32]. This specific feature of MFO will help achieving accurate results for the proposed design. Therefore, the performance of designed broadwell-Y shaped transistor has been optimized using MFO. The proposed FinFET structure has been studied at 20nm gate length as device performance at 20nm and below is affected by quantum mechanical effects and scattering effects. Thus, the analysis of such device becomes important from research point of view. Section II illustrates simulation setup and methodology for the designed structure. Section III presents the MFO optimization approach. Last section of this paper concludes the proposed work.

2. SIMULATION SETUP AND METHODOLOGY

The 3D design of broadwell-Y shaped transistor has been created on bulk silicon substrate in TCAD tool. For 20nm gate length of transistor, thickness of HfO_2 used as gate dielectric is 1nm. Fin height (H_{fin}) and width (W_{fin}) are 20nm and 10nm respectively. Doping concentration for channel, source/drain and substrate is 10^{18}, 10^{20} and $2x10^{15}$ cm^{-3} respectively. Tungsten material used for gate avoids poly-depletion effects [33]. Material composition for fin, source and drain is silicon. Aluminium contacts are attached to source, drain and gate to apply electrodes. Designed broadwell-Y shaped transistor and fin shape has been shown in Figure 2(a) and (b). Also, rectangular and trapezoidal FinFETs were designed with the same input process parameters. Designed devices were simulated for gate to source voltage V_{gs} = 0 - 1V and drain to source voltage V_{ds} = 0.05V. Lombardi model for the inclusion of various scattering effects which influence carrier mobility has been used [34-35].



(a)



(b)

Fig. 2. (a) Designed transistor structure showing gate, source and drain regions (b) Broadwell-Y fin shape.

Density gradient quantum correction model has been applied for carrier transport at nanoscale in order to include quantum mechanical effects. An extra term of quantum potential has been added to determine the charge carrier concentration which is defined in (1)(2)(3)(4):

$$\Phi_n = -2\beta_n\left(\frac{\nabla^2(\sqrt{n})}{\sqrt{n}}\right); \beta_n = \frac{(h/2\pi)^2}{12.e.m_e^*} \quad (1)$$

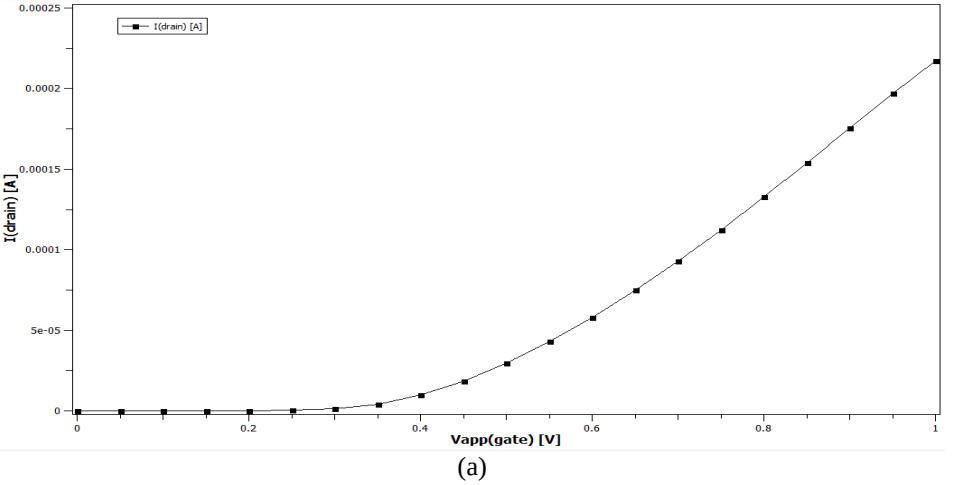
$$\Phi_p = -2\beta_p\left(\frac{\nabla^2(\sqrt{p})}{\sqrt{p}}\right); \beta_p = \frac{(h/2\pi)^2}{12.e.m_h^*} \quad (2)$$

$$n = N_c F_{\frac{1}{2}}\left(\frac{E_F - E_{c,eff} - \varphi_n}{KT_o}\right) \quad (3)$$

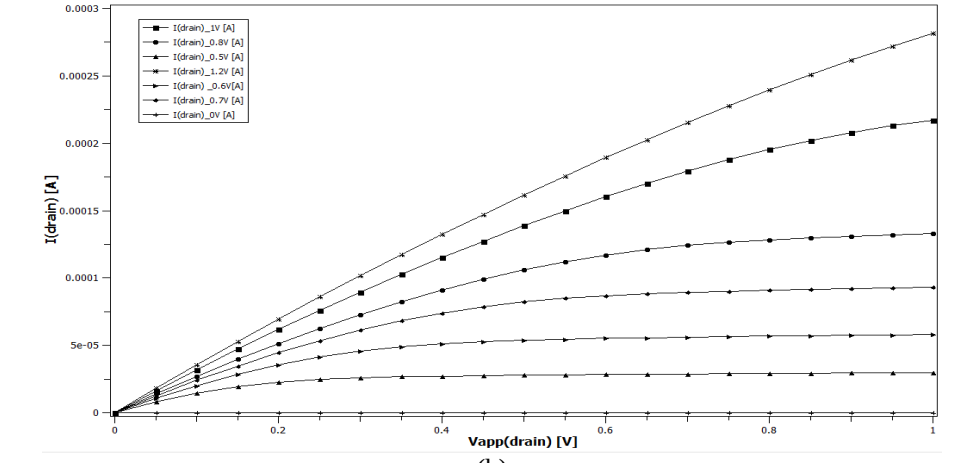
$$p = N_v F_{\frac{1}{2}}\left(\frac{E_{v,eff} + \varphi_p - E_F}{KT_o}\right) \quad (4)$$

where β_n and β_p are electron and hole density gradient coefficients, h is Planck's constant, T_o is temperature, E_F, $E_{c,eff}$, $E_{v,eff}$ represent fermi level, conduction band (CB) edge, valence band (VB) edge respectively. m_e^* and m_h^* are effective mass terms for e^- and hole, K is Boltzmann's constant, n and p define charge carrier density, N_c and N_v are effective density of states in CB and VB respectively [36-37]. Transfer characteristics corresponding to V_{ds} = 1V, drain characteristics for V_{gs} ranging from 0 to 1.2V and transconductance curve are shown in Figure 3(a-c). Equation (5) gives the relation between transconductance (g_m) and drain current (I_d).

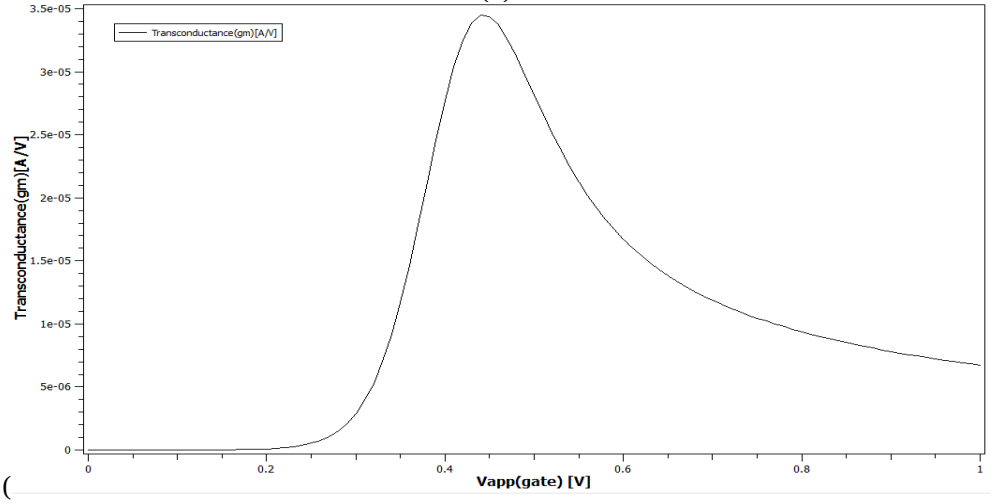
$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \text{ for constant } V_{ds} \quad (5)$$



(a)



(b)



(c)

Fig. 3. (a) Transfer characteristics, (b) drain characteristics of designed broadwell-Y shaped transistor (c) Transconductance curve w.r.t. gate-source voltage at V_{ds} of 0.05V.

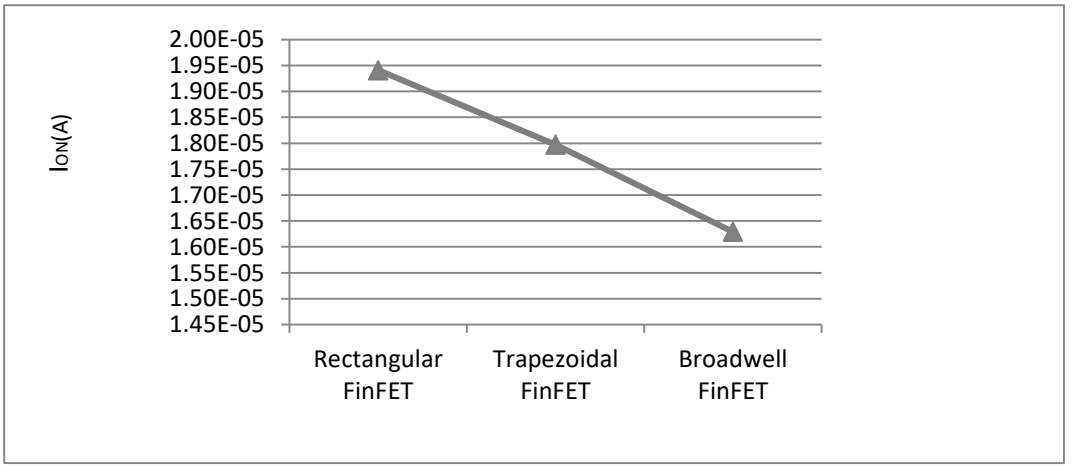


Fig. 4. I_{ON} for designed rectangular, trapezoidal and broadwell-Y shaped FinFETs.

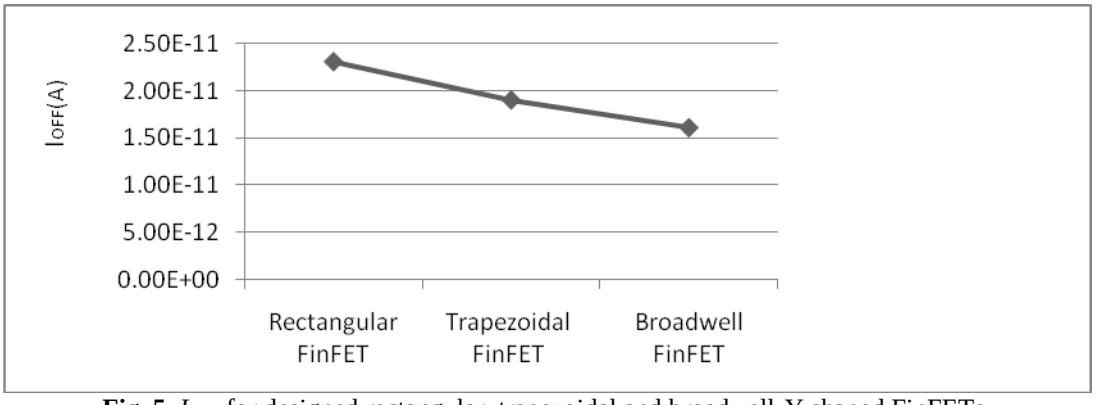


Fig. 5. I_{OFF} for designed rectangular, trapezoidal and broadwell-Y shaped FinFETs.

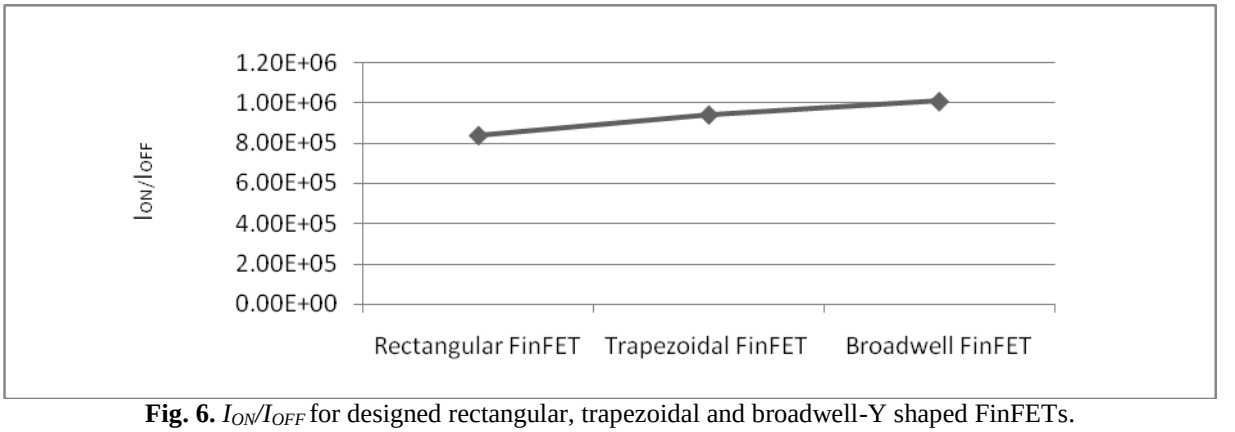


Fig. 6. I_{ON}/I_{OFF} for designed rectangular, trapezoidal and broadwell-Y shaped FinFETs.

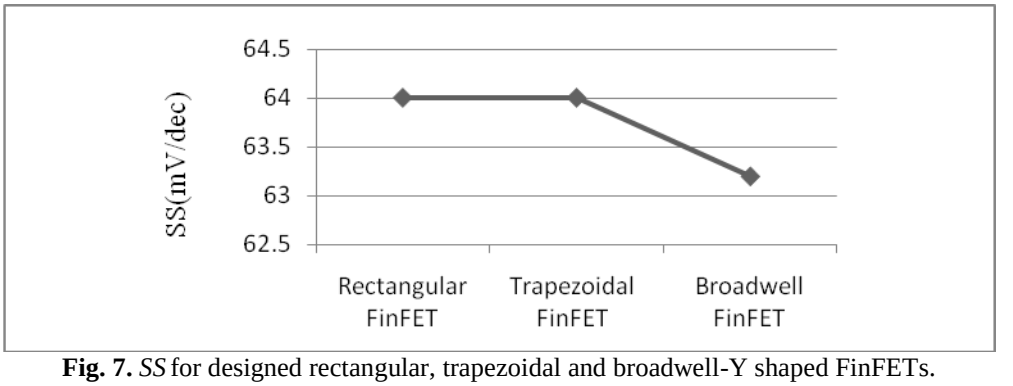


Fig. 7. *SS* for designed rectangular, trapezoidal and broadwell-Y shaped FinFETs.

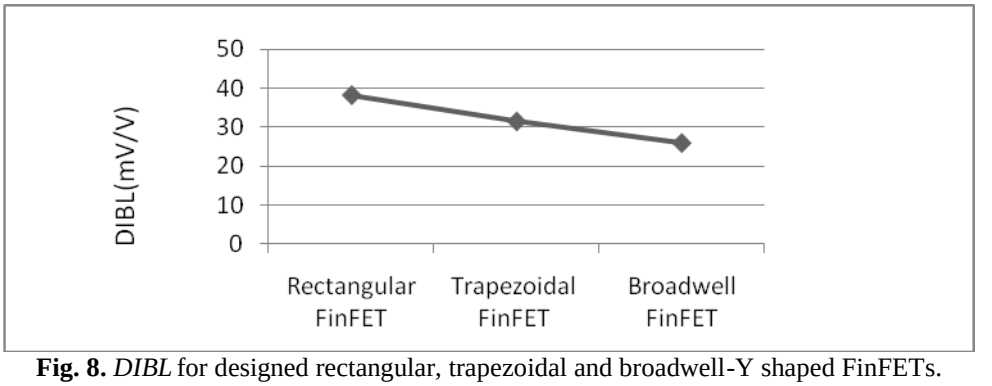


Fig. 8. *DIBL* for designed rectangular, trapezoidal and broadwell-Y shaped FinFETs.

On-current (I_{ON}), off/leakage current (I_{OFF}), on/off ratio (I_{ON}/I_{OFF}), Subthreshold Swing *(SS*) and Drain Induced Barrier Lowering (*DIBL*) are the parameters which have been evaluated to analyse the performance of designed device and compared with those of existing rectangular and trapezoidal structures as shown in Figures 4 to 8. At V_{gs} = 1V and 0V, I_{ON} and I_{OFF} are noticed respectively. SS is computed for decade change in drain current as given in (6)

$$SS = \frac{dV_{gs}}{d\log_{10} I_d} \tag{6}$$

DIBL is estimated at V_{ds} = 0.02V and 1V for I_d = W_{eff}/L_g x 10^{-7}A where W_{eff} is effective channel width = $2*H_{fin}$ + W_{fin}. This I_d value is $2.5x10^{-7}$A obtained using (7) and (8) [15].

$$W_{fin} = W_{fin,t} + \frac{\alpha}{\alpha+1}\left(W_{fin,bot} - W_{fin,t}\right) \tag{7}$$

$$\alpha = \frac{2W_{fin,bot} + W_{fin,t}}{2W_{fin,t} + W_{fin,bot}} \tag{8}$$

Where $W_{fin,t}$, $W_{fin,bot}$ represent the thickness of fin at the top and bottom respectively.

After comparing three designed structures, it was observed that I_{OFF}, I_{ON}/I_{OFF}, *SS* and *DIBL* are improved for Broadwell-Y shaped FinFET at the expense of reduced I_{ON}. Performance improvement of trapezoidal over rectangular FinFETs in terms of leakage current, on/off current ratio and DIBL is due to less top fin width of former and overall lesser area than the latter [15]. Also, the advantages of broadwell-Y shape over trapezoidal fin shaped FinFETs is due to the structure of fins as claimed by Intel in the reports [18]. Performance of broadwell-Y shaped FinFET was further optimized using MFO. Training the network through ANN is the first step towards the optimization process. For this purpose, four output parameters I_{ON}, I_{OFF}, *SS* and *DIBL* have been evaluated for a set of 56 samples of two input parameters [W_{fin}, T_{ox}]. This dataset is further given as input to artificial neural network (ANN) to get trained output. This is because ANN maps very well the multi-dimensional problems for given (i) dataset of inputs and corresponding targets, (ii) sufficient neurons in the hidden and output layer [38]. Training network used is 'feedforward' with learning rate of 0.03 and performance goal of 1e-05. Trained net file is further fed to optimization technique.

3. OPTIMIZATION RESULTS

MFO technique deals with the convergence of results imitating the concept of moths whose positions are updated after they are guided by moonlight for straight line movement. In MATLAB, MFO is supplied with the trained output network obtained from ANN and the fitness function defined in (9). Number of search agents and maximum numbers of generations in the algorithm are 20 and 50 respectively. Lower and upper bounds for inputs [W_{fin},T_{ox}] are [5,0.5] and [16,2] respectively.

Minimizing the fitness function (*ff*) corresponds to reduction in SCEs: *SS*, *DIBL*, I_{OFF} and increment in I_{ON}.

$$ff = SS + DIBL - I_{ON}*10^{5} + I_{OFF}*10^{12} \tag{9}$$

Procedural flow of MFO is:

- Random population of moths (search agents moving around search space) is created and corresponding fitness values are evaluated according to their position.
- Position of each moth is updated with respect to the flame (best position of moths obtained so far) given as:

$$F(moth_i, flame_j) = d_i.e^{ct}.\cos(2\pi t) + flame_j \tag{10}$$

$$d_i = \left| flame_j - moth_i \right| \tag{11}$$

  Where *'F'* is spiral function, 'd_i' is distance between *ith* moth and *jth* flame, '*c'* is constant indicating the shape of log spiral, '*t*' is random number lying in the range of [-1,1].
- According to (10) and (11), movement of moths around various flame positions leads to high exploration rate, but exploitation rate is decreased. Solution to this limitation was given by decreasing the number of flames '*flame_count'* with the increase in iteration '*iter*' given in (12):

$$flame\_count = round(Y - iter*(Y-1)/T) \tag{12}$$

'Y' is maximum no. of flames and '*T'* is total no. of iterations [32].

Two more optimization algorithms: Genetic Algorithm (GA) and Particle Swarm optimization (PSO) were used to optimize the performance of designed device i.e. minimize '*ff*'. Same population size and number of iterations of 20 and 50 respectively are used so as to compare the efficiency of three optimization approaches. In GA, on the basis of Darwin's concept of "survival of the fittest", selection, crossover and mutation are applied to the fit population [39]. In MATLAB, Selection function used is stochastic uniform, crossover function and probability is scattered and 0.8 respectively and mutation function is constraint dependent.

PSO results in optimized solutions after the velocity as well as position (local and global) of particles are updated as per (13), (14) [40]:

$$vel_{t+1} = w * vel_t + c_1 * rand * (loc\_pos_t - curr\_pos_t) + ... \\ c_2 * rand * (glob\_pos_t - curr\_pos_t) \quad (13)$$

$$curr\_pos_{t+1} = vel_{t+1} + curr\_pos_t \quad (14)$$

Parameters of PSO are (i) inertia weight, '*w*' set between [0.2, 0.8], (ii) cognitive factors; c_1, c_2 as 2. vel_{t+1}, vel_t is particle velocity at time '*t+1*' and '*t*'. loc_pos_t, $curr\_pos_t$ and $glob\_pos_t$ gives local best, current best and global best position of particles respectively at time '*t*'.

Optimum value of fitness function obtained from GA, PSO and MFO was 101.5692 corresponding to best value of input parameters [5.0542, 0.6843]. Convergence of fitness function is shown in Figure 9. It was observed that MFO resulted in faster converged performance than GA and PSO for the same optimum fitness value of 101.5692. For optimum input parameters obtained from optimization approach, broadwell-Y shaped structure was designed in TCAD and the output parameters obtained from simulated device were in close agreement with those obtained from MATLAB as shown in Table I with the tolerance of approximate less than 7%.

4. CONCLUSION

In this paper, broadwell-Y shaped transistor has been designed at 20nm gate length, 20nm fin height and 10nm fin thickness and simulated in TCAD tool considering the effects of scattering on mobility. Also, quantum mechanical effects were included in classical drift-diffusion model. Performance of designed transistor was optimized through ANN-MFO technique. Fin thickness and gate oxide thickness were the input parameters while training the neural network. On current, off state current and short channel effects have been analyzed. It was observed that MFO proved its effectiveness in solving the proposed optimization problem within very less time and with the deviation of approximately 7% from the simulation results obtained from TCAD. Leakage current and on-off current ratio is of the order of 10^{-12} A and 10^6 respectively and DIBL is less than 40mV/V, which is reasonably improved value. Ideally DIBL should be less than 100mV/V for reduced SCEs. Thus, the designed device is much suited for the applications where compact area, low power and low leakage are essential and device has to be operated at Nano-scale.

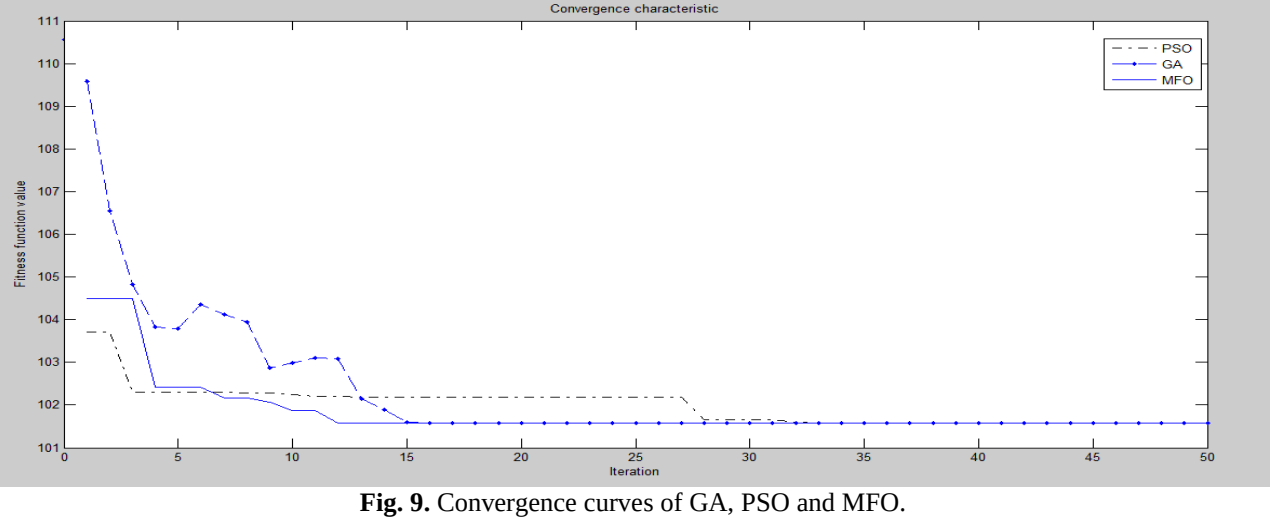


Fig. 9. Convergence curves of GA, PSO and MFO.

Table 1. Comparison of results obtained from MATLAB and TCAD simulations.

Output Parameters	MATLAB Results of ANN-GA, ANN-PSO and ANN-MFO	TCAD Simulation Results	% Error
I_{ON} (A)	1.0921e-05	1.083e-05	0.833%
I_{OFF} (A)	2.3051e-12	2.407e-12	4.42%
I_{ON}/I_{OFF}	4.738e06	4.5e06	5.02%
SS (mV/dec)	64.7699	65.4	0.97%
DIBL (mV/V)	35.5863	37.9	6.5%
Fitness Function	101.5692	104.624	3%

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