JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.14, NO.5, OCTOBER, 2014 http://dx.doi.org/10.5573/JSTS.2014.14.5.525

Performance Optimization Study of FinFETs Considering Parasitic Capacitance and Resistance

TaeYoon An, KyeongKeun Choe, Kee-Won Kwon, and SoYoung Kim

***Abstract*—Recently, the first generation of mass production of FinFET-based microprocessors has begun, and scaling of FinFET transistors is ongoing. Traditional capacitance and resistance models cannot be applied to nonplanar-gate transistors like FinFETs. Although scaling of nanoscale FinFETs may alleviate electrostatic limitations, parasitic capacitances and resistances increase owing to the increasing proximity of the source/drain (S/D) region and metal contact. In this paper, we develop analytical models of parasitic components of FinFETs that employ the raised source/drain structure and metal contact. The accuracy of the proposed model is verified with the results of a 3-D field solver, Raphael. We also investigate the effects of layout changes on the parasitic components and the current-gain cutoff frequency (f_T). The optimal FinFET layout design for RF performance is predicted using the proposed analytical models. The proposed analytical model can be implemented as a compact model for accurate circuit simulations.**

***Index Terms*—Cutoff frequency, fin field-effect transistors (FinFETs), fringe capacitance, number of gate fingers, number of fins, parasitic resistance, radio frequency (RF).**

Manuscript received May. 7, 2014; accepted Jul. 28, 2014
A part of this work was presented in Korean Conference on Semiconductors, Seoul in Korea, Feb. 2014.
Department of Semiconductor Systems Engineering, College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea
E-mail : ksyoung@skku.edu

I. INTRODUCTION

As traditional planar MOSFETs continue to be scaled down, the control of short-channel effects becomes increasingly difficult in planar-bulk architecture. Fin field-effect transistors (FinFETs) have been developed as an alternative device structure for technologies below the 22 nm node [1]. Advantages of FinFETs over conventional planar MOSFETs are high immunity to short-channel effects, drain-induced barrier lowering, high gate controllability, and reduction of leakage current [2-4]. Although FinFETs are potentially advantageous for further scaling, parasitic components present an important obstacle: fringing capacitances increase with scaling due to the increasing proximity of the source/drain selective epitaxial growth (SEG) region [5] and of the massive contact with a short length of interconnect to the gate [6], and series resistance also increases as the width of the fins is narrowed [7, 8]. These parasitics degrade circuit-level performance metrics such as digital circuit delay and analog/RF performance [6]. Recently, Wu et al. published a detailed analysis of geometry-dependent gate-capacitive and gate-resistive parasitics, conducted with the goal of reducing both the gate fringe capacitance and gate parasitic resistance for n-fin FinFETs [9]; however, the reference model employed in this work did not consider the use of the raised source and drain (RSD) structure and metal contact. Lacord et al. have analyzed capacitance models in FinFETs, taking into account the specific technology of RSD structure and metal contact [10]. Dixit et al. [7] developed a parasitic source/drain resistance model based on analysis of components of the series resistance in double-gate FinFETs and argued that the contact

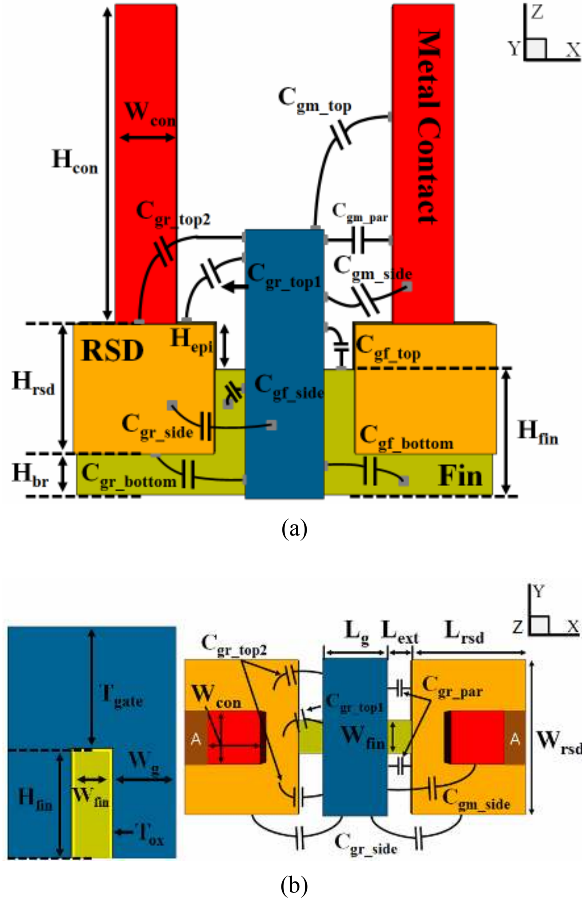


Fig. 1. Two-dimensional view of FinFET with RSD and metal contact structure (a) 2-D side view, (b) 2-D gate cross-sectional view and top view.

Table 1. Geometric parameters of FinFET.

Parameter	Description	[nm]
L_g	Gate Length	25
T_{gate}	Gate Top Side Height	43.2
W_g	Gate Wing Length	22.64
T_{ox}	Oxide Thickness	1.1
L_{ext}	Fin Extension	9.94
H_{fin}	Fin Height	39.36
W_{fin}	Fin Width	12.99
L_{rsd}	RSD Length	44.63
H_{fin}	RSD Height	40.26
W_{rsd}	RSD Width	40.26
H_{epi}	EPI Height	14.72
H_{con}	Contact Height	100.6
W_{con}	Contact Width	19.55
H_{br}	Bottom Fin Height	13.82

resistance is the dominant component. However, their approach was limited to only one contact surface. Tekleab et al. [8] provide further understanding of the parasitic resistance in double-gate FinFETs considering contact position. The contact resistance is modeled by generalizing the one-dimensional transmission line model (TLM) [11] to 2-D and 3-D; both these works used boundary conditions for modeling series resistance in 3-D structures. Such a model cannot reflect changes of fin height or RSD depth because TLM is only accurate when the current path in the junction is shallow. The radio-frequency (RF) performance of FinFETs has been investigated considering the parasitic series resistance and capacitance by widely varying its geometrical parameters [12, 13].

In this paper, we present an analytical fringe capacitance and parasitic resistance model of FinFETs that employ the RSD structure and metal contact. The proposed model significantly improves the estimation of parasitic components. The outer fringe capacitance model is divided into cross coupling capacitance components and each component is derived using conformal mapping [14, 15] and a non-dimensionalization technique [16]. The source/drain parasitic resistance model incorporates the contribution of contact and spreading resistance considering three-dimensional current flow, and each component is derived by using parallel connection of divided parts and field integration rather than by using TLM. The accuracy of the developed model is verified with a 2D and 3D field solver, Raphael [17]. The FinFET structure that is used to run 3D field solver for extracting parasitic components is shown in Fig. 1. We excluded the intrinsic capacitance and inner fringe capacitance with dielectric constant of the oxide close to 0 in order to extract the outer fringe capacitance among the parasitic components. In extracting resistance, we simulate only the half side of the structure shown in Fig. 8. The voltage is applied between the contact and the cross section just before the channel to extract only the source/drain resistance. By doing this, we can exclude channel resistance. We then present a detailed analysis of geometry-dependent three-dimensional parasitics to show how changes to geometrical parameters and layout, such as changing the number of gate fingers, affect the circuit performance metrics of current-gain cutoff frequency (f_T).

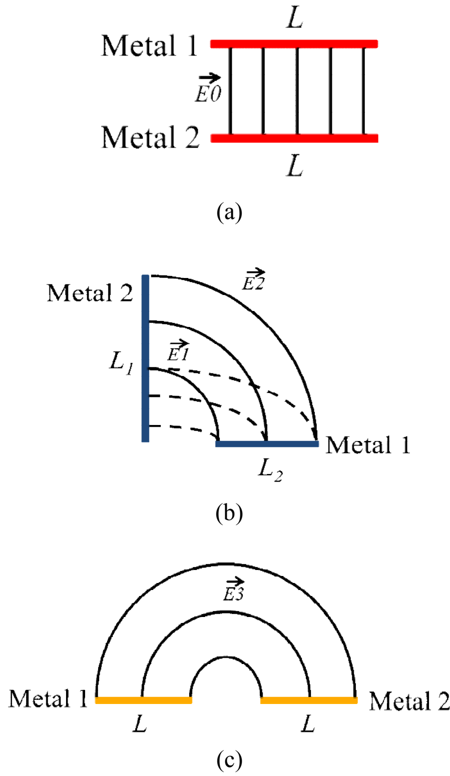


Fig. 2. Geometry-dependent capacitance components and their corresponding empirical models (a) parallel case, (b) perpendicular case, (c) coplanar case

II. Analytical Approach for Modeling Parasitic Capacitance and Resistance

1. Fringe Capacitance Modeling

A. Derivation of the Proposed Model

Fig. 1 shows a 2-D cross-sectional view of the FinFET employing the RSD structure and metal contact. Geometric parameters are assigned for each 3-dimensional structure; the x, y and z axes respectively represent the length, width and, height of each geometric block. The dimensions applied in this work are summarized in Table 1 on sub-22 nm process FinFETs [18]. Extra coefficients are defined to simplify expressions: $A = L_{ext} + L_{rsd}$, $B = 0.5(L_{rsd} - W_{con})$, $C = 0.5(F_{pitch} - W_{con})$, $D = H_{con} - (H_g - H_{epi} - H_{fin})$, $E = H_{con} - D$, $F = H_g - H_{br} - H_{rsd}$.

Fig. 1 illustrates the complicated geometric structure of a FinFET and its electric coupling between various potential nodes such as metal contact, RSD, fin, and gate through the outer fringe capacitances. The total outer gate fringe capacitance from these interlacing nodes comprises three parts contributed by the main potential nodes: gate to fin, gate to RSD, and gate to metal contact node.

The C_{gm} is composed of three cross-coupled fringe capacitance components (C_{gm_top}, C_{gm_side}, and C_{gm_par}) and represents the fringe capacitance between the gate and the metal contact node. C_{gr} consists of five cross-coupled fringe capacitance components ($C_{gr_top1\&2}$, C_{gr_side}, C_{gr_bottom}, and C_{gr_par}) and represents the fringe capacitance between the gate and the RSD node. In the analysis, each component is coupled with gate metal to the top, side and bottom planes of the RSD. The gate-to-fin fringe capacitance is modeled as a C_{gf}. C_{gf} consists of C_{gf_side}, C_{gf_top}, and C_{gf_bottom}, which are cross coupling fringe capacitances. C_{gf} is electric coupled capacitance from the gate metal node to the top, side, and bottom plane node of fin structure.

The following formula expresses the total gate fringe capacitance as the sum of the three components C_{gf}, C_{gr}, and C_{gm}:

$$C_{gtot} = C_{gf} + C_{gr} + C_{gm} . \quad (1)$$

Each capacitance model is derived using several methods: conformal mapping, field integration, and traditional calculation based on parallel-plate capacitance.

The method used to model outer fringe capacitance is summarized in Fig. 2; this analytical model is based on conventional formulas of conformal mapping and field integration, to which empirical parameters and applied practical methods are added. Outer fringe capacitance models (2), (3), and (4) are derived by adding empirical parameters and combining with basic formulas expressing the practical structure between two potential planes.

Three general structure cases are defined in this work, the first of which is the case of parallel structure between two rectangular metal plates (Fig. 2(a)). The field between two parallel metals, termed electric field 0, is integrated as a plate capacitance C_{par}. C_{gr_par} and C_{gm_par} are modeled as parallel plates [19].

$$C_{par} = \varepsilon_{ox} \frac{L}{d} \quad (2)$$

Table 2. Geometric parameters used in the general outer fringe capacitance model.

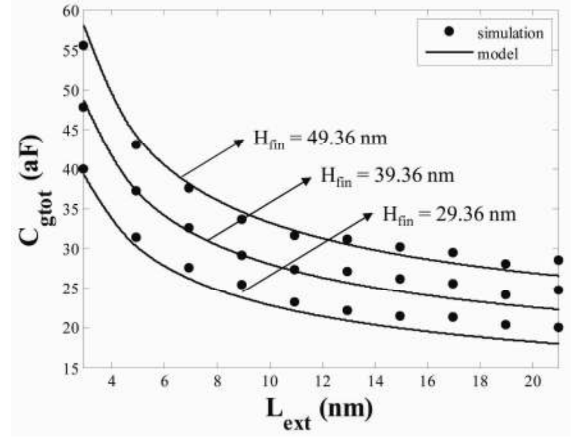
C_{fringe}	L_{ε}	L_{M1}	L_{M2}	H_{Cfr}	k
C_{gf_side}	T_{ox}	W_g	L_{ext}	H_{fin} - H_{br}	4.82
C_{gf_top}	T_{ox}	T_{gate}	L_{ext}	W_{fin}	6.23
C_{gf_bottom}	T_{ox}	W_g	A	H_{br}	5.54
C_{gr_top1}	L_{ext}	C	F	W_{con}	0
C_{gr_top2}	L_{ext}	L_{rsd}	E	W_{rsd} - W_{con}	0
C_{gr_bottom}	L_{ext}	H_{br}	L_{rsd}	W_{rsd} - W_{fin}	0
C_{gm_side}	L_{ext}+B	C	W_{con}	E	0
C_{gm_top}	L_{ext} + B	0.5 L_g	D	W_{con}	2.92

Next is the perpendicular case, in which metal 1 and metal 2 are perpendicular to each other (Fig. 2(b)). In this case, metal 2 is commonly much longer than metal 1, so the electric field between the two metal planes cannot be expressed using only one electric field. Rather, a formula is used that accounts for both the electric fields $\vec{E}_1$ and $\vec{E}_2$ illustrated in Fig. 2(b): the first term of formula (3) represents $\vec{E}_2$ and its second term represents $\vec{E}_1$. An empirical parameter η is used to adjust for the mismatch between the two metal lengths. The coupling capacitance components C_{gf_top}, C_{gf_side}, C_{gf_bottom}, and C_{gm_top} are modeled using this model [10, 14, 15].

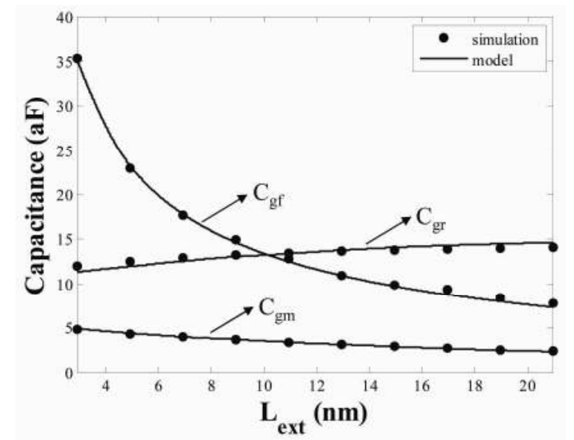
$$C_{per} = \frac{2\varepsilon_{ox}}{\pi} ln\left(\frac{L_{\varepsilon} + \eta\, min(L_{M1}, L_{M2}) + \sqrt{(\eta\, min(L_{M1}, L_{M2}))^2 + 2\eta\, min(L_{M1}, L_{M2}) L_{\varepsilon}}}{L_{\varepsilon}} \right) H_{C_{fr}} + k \frac{\varepsilon_{ox} H_{C_{fr}}}{2\pi} ln\left(\frac{\pi H_{C_{fr}}}{L_{\varepsilon}} \right) \tag{3}$$

The geometrical parameters for this model are defined in Table 2. In modeling C_{gr_top1}, C_{gr_top2}, C_{gr_bottom} and C_{gm_side}, electric field component $\vec{E}_1$ is zero and there is only $\vec{E}_2$. So, they can be modeled with formula (3) by setting k to zero.

The last geometric case is the coplanar case, representing the $\vec{E}_3$ between two coplanar metals (Fig. 2(c)). C_{gr_side} is represented by (4) [14, 15], and δ is adopted as an empirical parameter to modulate the mismatch between L_g and L_{ext}. The formula (5) is adopted to cover the invalid value at the infinitesimal point of denominator.



(a)



(b)

Fig. 3. Proposed model validation versus 3D simulation (a) total fringe capacitance model for L_{ext}, (b) cross capacitance components for L_{ext}.

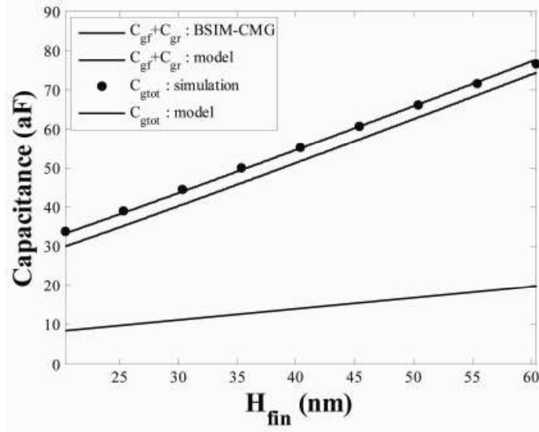
$$C_{cop} = \frac{\varepsilon_{ox}}{2\pi} ln\left(1 + \frac{2L}{L_{ext}}\right) \tag{4}$$

$$\frac{L}{L_{ext}} = \delta\left(\frac{\sqrt{(L_{rsd} + L_g/2)(L_{rsd} + L_{ext})L_{rsd} L_g/2}}{(L_{rsd} + L_{ext} + L_g/2) \cdot L_{ext}} \right) \tag{5}$$

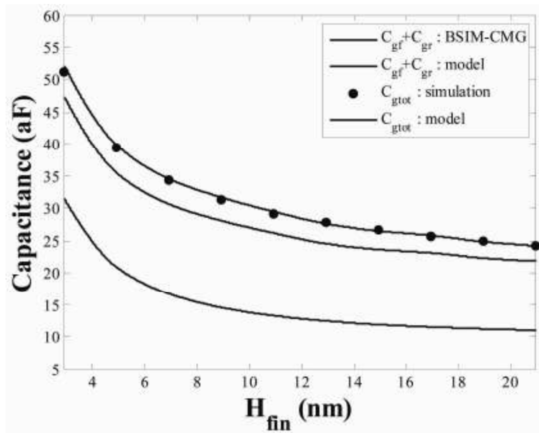
Table 2 summarizes the geometric parameters of the fringe capacitance model. L_{M1} and L_{M2} represent the lengths of the two metals. L_{ε} and H_{cfr} represent the length of the dielectric material and the height of the 2-D outer fringe capacitance, respectively. The empirical parameter η is used to adjust for mismatch among the metal length.

B. Validation of the Proposed Model

The accuracy of the proposed model is validated by using 3D Raphael simulation. In BSIM-CMG [20], the outer fringe capacitance model includes C_{gf} and C_{gr}, but



(a)



(b)

Fig. 4. Proposed model and BSIM-CMG prediction of fringe capacitance (a) total outer fringe capacitance versus H_{fin}, (b) total outer fringe capacitance versus L_{ext}.

does not include C_{gm}; also, the BSIM-CMG model for C_{gf} and C_{gr} cannot accurately model the E-field among the potential nodes in the complicated structure studied herein. For instance, in the case of C_{gf}, the BSIM-CMG model does not include the E-field of the perpendicular case ($\vec{E_2}$), illustrated in Fig. 2(b).

In modeling C_{gr}, the top-side electric field coupling capacitance (the darkly colored area marked A in Fig. 1(b)) is terminated by the metal contact, but BSIM-CMG does not consider the metal structure; thus, this area and the contact area are considered as an electric field between the gate and the RSD. In the proposed model, C_{gr_top} is divided into two cross coupling components (C_{gr_top1} and C_{gr_top2} in this work; see Fig. 1(b)) to better represent the electric field of the top side of the RSD.

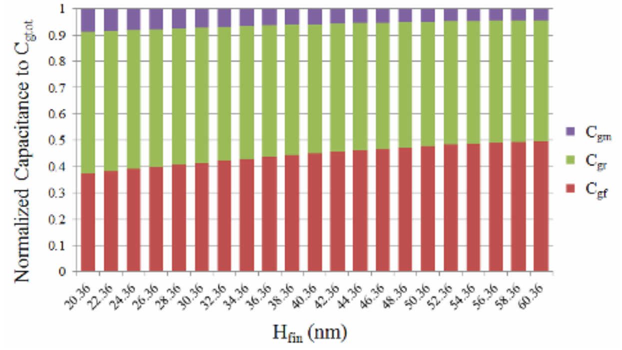


Fig. 5. Relative capacitance contributions of each cross-coupled component for various H_{fin} from 20.36 to 60.36 nm.

The outer fringe capacitance results were validated by comparison with 3D Raphael simulation data, including verification of the total outer fringe capacitance model versus L_{ext} for various H_{fin} (Fig. 3(a)) and verification of the accuracy of cross components versus L_{ext} (Fig. 3(b)). In a comparison of the proposed model and BSIM-CMG (Fig. 4), the modeled C_{gtot} matches the 3D simulation data very well, whereas $C_{gr}+C_{gf}$ is below C_{gtot} because of the elimination of C_{gm} to allow comparison of pure $C_{gr}+C_{gf}$ between the proposed model and BSIM-CMG.

Fig. 5 shows the proportion of each capacitance component of the total gate fringe capacitance for various H_{fin}. C_{gm} accounts for approximately one tenth of the total gate fringe capacitance. The contribution of C_{gm} gradually increases as H_{fin} and L_{ext} scale down.

2. Parasitic Source/Drain Resistance Modeling

A. Proposed Model Derivation

In this study we consider FinFETs whose fabrication includes the application of a selective epitaxial growth (SEG) process to merge individual fins. A 3-dimensional drawing of the raised source/drain FinFET is shown in Fig. 6. The source and drain silicon are enlarged by the SEG process, thereby reducing their resistance. For multi-fin FinFETs, a larger source and drain also makes contact easier. Fig. 7 shows a cross-sectional view of a FinFET along the source-to-drain direction; this FinFET structure has source/drain extension regions on either side of the channel region, and includes a heavily doped source/drain (HDD). The metallic regions (on top of the raised source and drain, and denoted by dotted lines in Fig. 7) are silicide. The SEG height is defined as H_{rsd}.

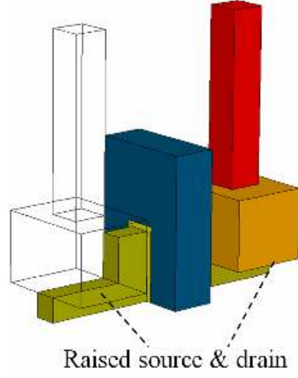


Fig. 6. 3-D view of a FinFET with RSD.

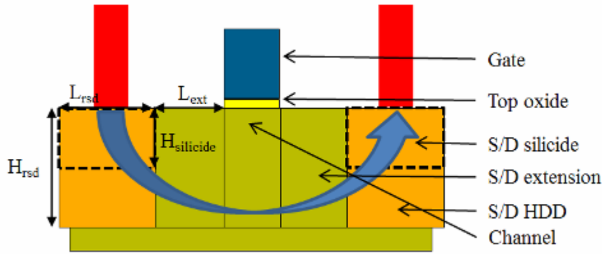


Fig. 7. Cross section of an RSD FinFET including symbol definitions. This figure is a simulation structure in S-visual TCAD [21]; the arrow depicts the current flow between the source and the drain.

$H_{silicide}$ is the thickness of the silicide.

The parasitic source/drain resistance in this study (R_{sd}) includes contact, silicide and HDD region. By subtracting the channel resistance from the total resistance between the source and drain, the total series resistance was simulated for various gate lengths. As the gate length approaches zero, the channel resistance is forced to zero. We can extrapolate R_{sd} according to simulation results in different gate length. Note that R_{sd} is composed of contact metal resistance $R_{contact}$, contact and RSD resistance R_{con}, extension resistance R_{ext}, and spreading resistance R_{sp}. R_{con} and R_{ext} are the dominant components and are investigated thoroughly herein.

We now develop the model for the device type shown in Fig. 8, which depicts a half-side (either source or drain) cross-sectional view of the device and its series resistance components: contact metal resistance, contact and RSD resistance, extension resistance, and spreading resistance. In the figure, R_{con} and R_{ext} are divided by a line between A to B, which denotes the guideline representing the current flow. The serial connection of R_{con} and R_{ext} can be modeled as several small sections of

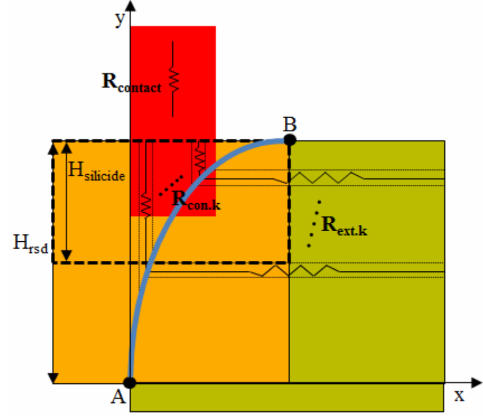


Fig. 8. Cross-sectional view of source region and contact. The parasitic resistance between the contact and the channel region is divided into four parts: $R_{contact}$, R_{con}, R_{ext} and R_{sp}.

parallel resistance. When SEG is divided into n equal parts, $R_{con.k}$ and $R_{ext.k}$ respectively denote the small-section resistance in the k-th vertical section from the left (x=0) and in the k-th horizontal section from the lowest part of the SEG. We define the parasitic source and drain resistance and the guideline in the FinFET as

$$R_{sd} = R_{contact} + \left(\sum_{k=1}^{n} \frac{1}{R_{con.k} + R_{ext.k}} \right)^{-1} + R_{sp} \tag{6}$$

and

$$f(x) = 0.894 \ln\left(\frac{x}{2.512} + 1 \right). \tag{7}$$

By using a basic resistance equation for a square pole, we can express the contact metal resistance $R_{contact}$ as [19]

$$R_{contact} = \rho_{metal} \frac{H_{con}}{W_{con}^{2}}, \tag{8}$$

where ρ_{metal} is the metal's resistivity, H_{con} is its height, and W_{con} represents both its length and width.

When the k-th section from the left (x=0) includes the HDD region, $R_{con.k}$ is the small-section resistance through the silicide and HDD region from the surface between the contact metal and silicide to the guideline. $R_{ext.k}$ is the small-section resistance through the HDD and extension region from the guideline to the surface between the extension and channel region. Accordingly, $R_{con.k}$ and

$R_{ext.k}$ can be expressed as a function of device geometry parameters as

$$R_{con.k} = \rho_c \frac{H_{silicide}}{L_{rsd}/n} + \rho_s \frac{H_{fin} - H_{silicide} - f((k-0.5)L_{rsd}/n)}{L_{rsd}/n} \tag{9}$$

and

$$R_{ext.k} = \rho_s \frac{L_{rsd} - f^{-1}((k-0.5)H_{fin}/n)}{H_{fin}/n} + \rho_{ext} \frac{L_{ext}}{H_{fin}/n}, \tag{10}$$

where ρ_c, ρ_s, and ρ_{ext} are the resistivities of the silicide, HDD, and extension regions and the f function represents the guideline.

When the k-th section from the left (x=0) excludes the HDD region, $R_{con.k}$ is the small-section resistance through only the silicide region from the surface between the contact metal and the silicide to the guideline. $R_{ext.k}$ is the small-section resistance through the silicide and the extension region from the guideline to the surface between the extension and channel regions. By using a similar analysis method to (9) and (10) that accounts for the HDD region, we can express $R_{con.k}$ and $R_{ext.k}$ as

$$R_{con.k} = \rho_c \frac{H_{fin} - f((k-0.5)L_{rsd}/n)}{L_{rsd}/n} \tag{11}$$

and

$$R_{ext.k} = \rho_c \frac{L_{rsd} - f^{-1}((k-0.5)H_{fin}/n)}{H_{fin}/n} + \rho_{ext} \frac{L_{ext}}{H_{fin}/n}. \tag{12}$$

In the remaining part of this section, we model the spreading resistance to compensate for the parasitic source/drain resistance for the case in which the SEG process is applied, producing a wide RSD as shown in Fig. 9(b). The spreading resistance R_{sp} represents the difference between the resistance of a narrow RSD, R_{narrow}, and that of a wide RSD, R_{wide}, as illustrated in Fig. 9. R_{narrow} is derived by using the basic resistance equation for a square pole. The derivation of R_{wide} includes the parameter θ, the current flow angle that arises from the difference in width between the RSD and fin regions. R_{wide} is calculated using field integration by applying θ and geometrical parameters.

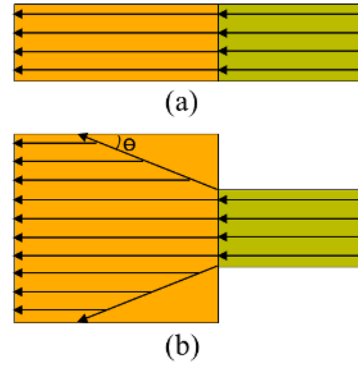


Fig. 9. Schematic drawing showing 2-D current flow for (a) a narrow RSD, (b) a wide RSD.

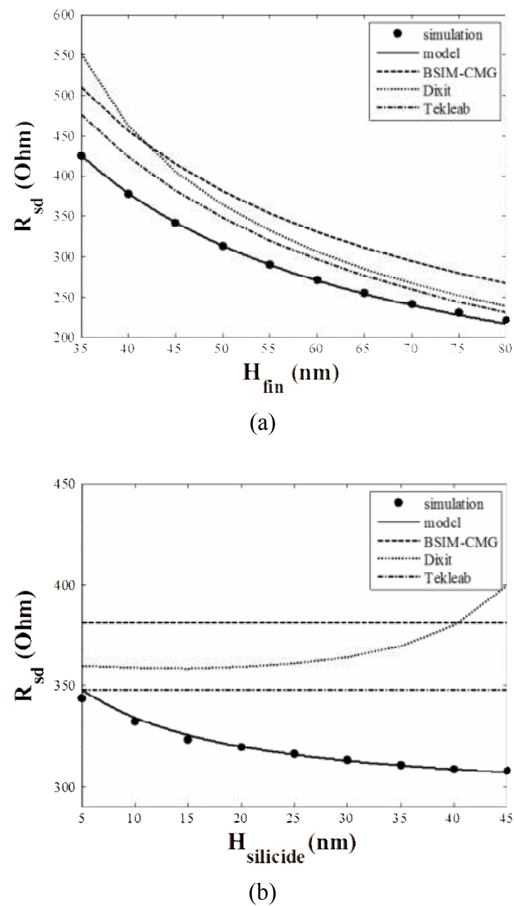


Fig. 10. Comparison of the parasitic source/drain resistance model (lines), 3-D numerical simulation results (symbols), and reference models (dash) as a function of fin height and silicide height.

R_{sp} is modeled as follows [7, 8]:

$$R_{sp} = R_{narrow} - R_{wide}, \tag{13}$$

where

$$R_{narrow} = \rho \frac{L_{rsd}}{W_{fin}} \quad (14)$$

$$R_{wide} = \frac{\rho}{2\tan\theta} \ln\frac{W_{rsd}}{W_{fin}} + \rho \frac{L_{rsd} - 0.5(W_{rsd} - W_{fin})\cos\theta}{W_{rsd}}. \quad (15)$$

B. Proposed Model Validation

The accuracy of the proposed parasitic source/drain resistance model is verified by 3-D numerical simulation, using geometrical parameters such as H_{fin} and $H_{silicide}$. Our model and the 3-D device simulations agree excellently with reference models (Fig. 10). Increasing H_{fin} decreases R_{sd}, indicating that the increase in R_{con} arising from increasing volume is weaker than the R_{ext} decrement that arises from increasing H_{fin}. In previous studies, the rate of change in R_{sd} caused by increasing H_{fin} was larger than in the proposed model and simulation results, because the reference models do not reflect the increase in R_{con} that arises from increasing H_{fin}. In the proposed model, it is observed that a large $H_{silicide}$ reduces R_{sd} because a deep silicide region reduces R_{con}. Contrastingly, the reference models do not reflect changes in the silicide depth.

III. LAYOUT OPTIMIZATION CONSIDERING PARASITIC COMPONENTS IN MULTI-FIN FINFETS

The layout of a FinFET critically impacts its high-frequency performance because of the layout's effect on the important parasitic series resistance and capacitance [12, 13]. To investigate the RF performance of FinFETs, we have studied the performance of a test device (Fig. 11) in various wiring and layout schemes (Fig. 12). In this section, we will discuss the effects of layout configuration on the parasitic resistance and capacitance of a FinFET device, and thus their impacts on the device's RF performance.

1. Fringe capacitance change in multi-finger FinFET

An RF layout typically includes a wide metal gate and uses a number of fingers to obtain high transconductance and fine noise performance. Additionally, to keep the layout compact and to minimize the distance between the contact and the interconnect, interdigitated configurations

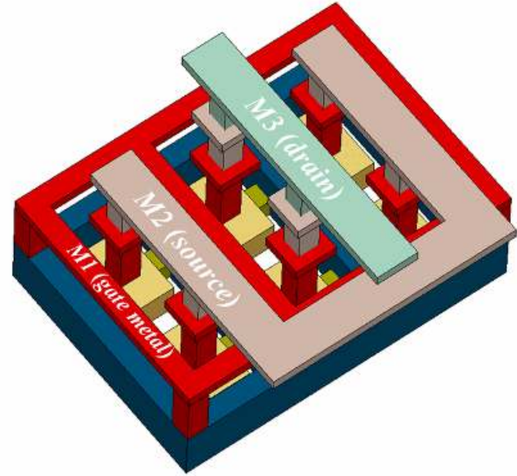
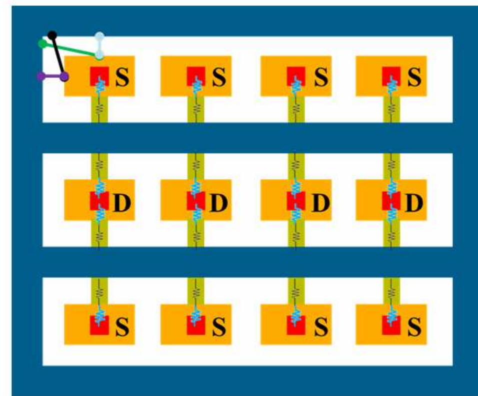
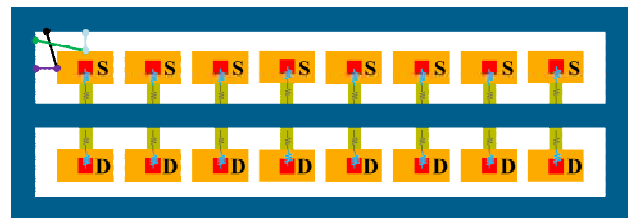


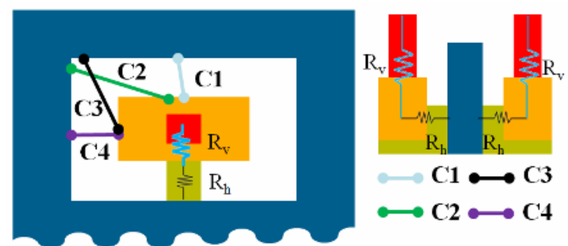
Fig. 11. Layout scheme of a test RF device based on a FinFET (2 fin/ 2 finger – total of 4 fins).



(a)



(b)



(c)

Fig. 12. Layout scheme of RF FinFET (a) 8 fins/ 2 fingers, (b) 8 fin/ 1 finger, (c) Parasitic components in RF layout.

(with alternating source and drain) are used. When designing RF circuits with FinFETs, the extra outer fringe capacitance components labeled C1, C2, C3, and C4 in Fig. 12 should be considered. Fig. 11 shows a simplified RF layout; Fig. 12(a) shows a two-finger layout and Fig. 12(b) shows a single-finger layout, both using 8 fins. The total extra fringe capacitance of the multifinger layout scheme in Fig. 12(a) is 8 C1 + 4 C2 + 4 C3 + 6 C4, whereas that of the single-finger layout in Fig. 12(b) is 16 C1 + 4 C2 + 4 C3 + 4 C4. The values of C1, C2, C3, and C4 can be determined from (1)–(5).

2. Parasitic resistance variation change in multifinger FinFET

Parasitic resistance is denoted as R_v and R_h in Fig. 12. R_v and R_h represents the vertical and the horizontal resistance in the multi-finger FinFET as shown in Fig. 12(c). By associating the proposed model with equation (6), R_v corresponds to $R_{contact}$ and R_h corresponds to $(R_{con.1}+R_{ext.1})//(R_{con.2}+R_{ext.2})//\ldots//(R_{con.n}+R_{ext.n})+R_{sp}$. Both the Figs. 12(a) and (b) layout configurations have the same number of R_h components, but their R_v components differ in number based on the contact position. The number of source and drain contacts differs when different finger numbers are used with the same fin number. The Fig. 12(a) structure has four source contacts and eight drain contacts, whereas the Fig. 12(b) structure has eight source contacts and eight drain contacts. In addition, the series and parallel connections of those resistors change for different fin/finger combinations. In the Fig. 12(a) structure, source-side parasitic resistance is simply composed of the parallel connection of R_v and R_h, but drain-side parasitic resistance is modeled as a parallel connection of the series of R_v and $R_h//R_h$. For the Fig. 12(b) structure, the source and drain sides have the same parasitic resistance: R_v and R_h is connected as a series at each source and drain, giving the resistance sum R_v+R_h for the parallel connection. Thus, the parasitic resistance of the total structure decreases when the N fins/ N fingers design is adopted. The values of R_v and R_h can be determined from (6)–(15) in section II-2.

3. RF performance in multifinger FinFETs

The current-gain cutoff frequency (f_T), an RF figure of merit, is evaluated using the following equation [22]:

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gs}^2 + 2C_{gs}C_{gd}}} \times \left\{ 1 - \frac{C_{gs}+C_{gd}}{C_{gs}^2+2C_{gs}C_{gd}} \times \left[\begin{array}{l} g_{ds}\left(C_{gs}R_s + C_{gs}R_d + C_{gd}R_d\right) \\ + g_m\left(C_{gd}R_d - C_{db}R_s\right) \end{array} \right] \right\} \quad (16)$$

where g_m and g_{ds} are the transconductance and output conductance, C_{gs} and C_{gd} are the gate-source and gate-drain capacitance, R_s and R_d are the extrinsic source and drain resistances, and C_{db} is the drain-to-bulk-junction capacitance. To obtain intrinsic characteristics including g_m and g_{ds}, the BSIM-CMG model can be used, including DC fitting based on the measured FinFET characteristics [23]. The C_{db} can be calculated assuming a simple p-n junction. In RF/analog applications, the device should be designed to improve f_T. When estimating (16), the capacitive and resistive parasitics C_{gs}, C_{gd}, R_s, and R_d significantly degrade the f_T.

In order to validate the analytical model of parasitic components in a multifinger RF device based on a FinFET, 3-D numerical simulations have been done for the 45 fin FinFET in RF layout with variable finger numbers. Total gate fringe capacitance C_{gsd} and parasitic S/D resistance R_{sd} have been extracted from simulated RC extractions. A comparison of these extracted parasitic values and those calculated using the proposed analytical model for the same effective width is shown in Fig. 13. The proposed model is in good agreement with 3-D numerical simulations.

Fig. 14 shows f_T as a function of the number of fingers using the proposed parasitic capacitance and resistance model of the multifin FinFET, considering the layout scheme of the RF device. For a given effective width, there is an optimum number of fingers that can maximize f_T. As can be seen from Fig. 14, we obtain optimum number of finger=10, 9, 6, and 5 values in 60, 45, 30, and 20 fin FinFET. For various cases each using the same effective width, the intrinsic components g_m and g_{ds} do not change in response to changing the number of fingers. C_{db} is also unaffected by finger variations; it is excluded from consideration in this paper to focus on the parasitic capacitance and resistance. The effect of C_{gs} and C_{gd} on f_T is more significant than that of R_s and R_d because the dummy gate causes additional capacitance components C1-C4. Therefore, FinFETs should be designed with a greater focus on parasitic capacitance than on parasitic resistance.

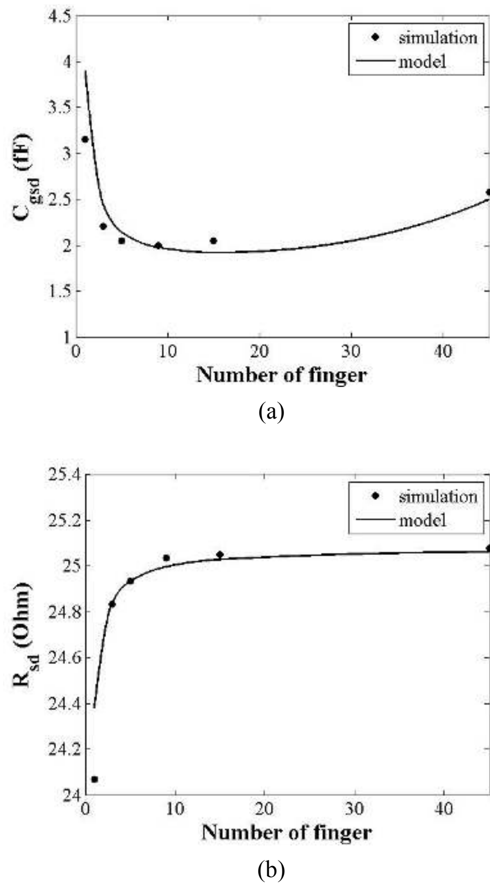


Fig. 13. Total gate fringe capacitance C_{gsd} and parasitic S/D resistance R_{sd} in the 45 fin FinFET with RF layout as a function of finger number. The analytical model has been compared with 3-D numerical simulations using Raphael.

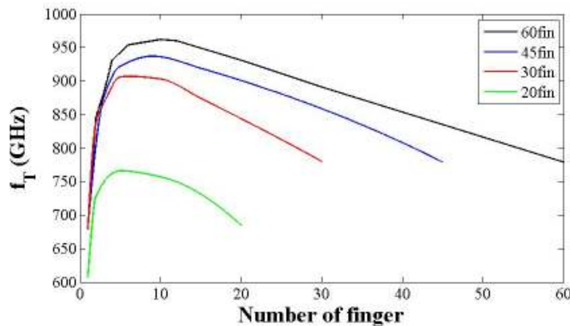


Fig. 14. Current-gain cutoff frequency (f_T) as a function of the number of fingers for several fin numbers. To ensure a fair comparison of f_T values, the finger number of each different fin number is adjusted to have the same device width.

IV. CONCLUSIONS

In this paper, a comprehensive model is proposed for parasitic outer fringe capacitance and source/drain series resistance in FinFETs employing the RSD structure and metal contact. The proposed analytical model can be implemented as a compact model for accurate circuit simulations. We analyze the effects of geometrical parameter variation on parasitic capacitance and resistance of FinFETs. The 3-D fringe capacitance is decomposed into 2-D components, each of which is derived with a conformal mapping technique and non-dimensionalization method. The source/drain parasitic resistance model incorporates the series connection of resistance in the metal contact, silicide, RSD, and extension using field integration instead of TLM. The accuracy of the proposed model is verified with the results of a 3-D field solver, Raphael. We also investigate the effects of layout changes on the parasitic components of an RF circuit design, confirming that a change in the number of fingers in FinFETs having the same device width results in variations in fringe capacitance and parasitic resistance. The FinFET layout design for optimum RF performance can be predicted using the proposed analytical models. This work is based on the ideal assumption that number of fingers variation affects only the parasitic components, namely, C_{gsd} and R_{sd}. We currently study more realistic cases that finger number variation possibly affects the intrinsic characteristics and develop models that can predict optimum number of fingers in various fin numbers in RF layout.

ACKNOWLEDGMENTS

This work was supported by the IT Research and Development program of MKE/KEIT [10039174, Technology development of 22 nm level foundry devices and PDK]. The CAD tools were supported by IDEC.

REFERENCES

[1] The International Technology Roadmap for Semiconductors (ITRS), 2013.

[2] B. K. Choi, K. R. Han, K. H. Park, Y. M. Kim, and J. H. Lee, "Study on Electrical Characteristics of Ideal Double-Gate Bulk FinFETs," Journal of Semiconductor Technology and Science, vol. 43, no. 11, 2005.

[3] E. J. Nowak, Ingo Aller, Thomas Ludwig, KeunWon Kim, Rajiv V. Joshi, ChingTe Chuang, Jerry Bernstein, and Ruchir Puri., “Turning silicon

on its edge [double gate MOS/ FinFET technology],” IEEE Circuits and Devices Magazine, vol. 20, no.1, pp. 20-31, 2004.
[4] K. W. Lee, S. S. Noh, N. H. Kim, K. -W. Kwon, and S. Y. Kim, “Comparative study of analog performance of multiple fin tri-gate FinFETs,” International Conference on Electronics, Information and Communication, 2012.
[5] C. R. Manoj, A. B. Sachid, F. Yuan, C. Y. Chang, and V. R. Rao, "Impact of fringe capacitance on the performance of nanoscale FinFETs," IEEE Electron Device Lett., vol. 31, no. 1, pp. 83-85, 2010.
[6] V. Subramanian, A. Mercha, B. Parvias, M. Dehan, G. Groeseneken, W. Sansen, and S. Decoutere, "Identifying the bottlenecks to the RF performance of FinFETs," in Proc. 23rd Int. Conf. VLSI Design, pp. 111-116, 2010.
[7] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. D. Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," IEEE Trans. Electron Devices, vol. 52, no. 6, pp. 1132-1140, 2005.
[8] D. Tekleab, S. Samavedam, and P. Zeitzoff, "Modeling and Analysis of Parasitic Resistance in Double-Gate FinFETs," IEEE Trans. Electron Devices, vol. 56, no. 10, pp. 2291-2296, 2009.
[9] W. Wu and M. Chan, "Analysis of Geometry-Dependent Parasitics in Multifin Double-Gate FinFETs," IEEE Trans. Electron Devices, vol. 54, no. 4, pp. 692-698, 2007.
[10] J. Lacord and F. Boeuf, "Comprehensive and Accurate Parasitic Capacitance Models for Two- and Three-Dimensional CMOS Device Structures," IEEE Trans. Electron Devices, vol. 59, no. 5, pp. 1332-1344, 2012.
[11] H. H. Berger, "Contact resistance on diffused resistors," in Proc. ISSCC, pp. 162-163, 1969.
[12] S. Kalaivani, K.K. Nagarajan, and Dr. R. Srinivasan, “Sensitivity of 30 nm Gatelength FinFET based LNA to Various Geometrical parameters,” in Proc. ICETECT, pp. 571-576, 2011.
[13] J. C. Tinoco, S. S. Rodriguez and et. al., “Impact of Extrinsic Capacitances on FinFET RF performance,” IEEE trans. vol. 61, no. 2, pp. 833-840, Feb. 2013.
[14] A. Bansal, B. C. Paul, and K. Roy, “Modeling and optimization of fringe capacitance of nanoscale DGMOS devices,” IEEE Trans. Electron Devices, vol. 52, no. 2, pp. 256–262, Feb. 2005.
[15] A. Bansal, B. C. Paul, and K. Roy, “An analytical fringe capacitance model for interconnects using conformal mapping,” IEEE Trans.Computer-Aided Design Integr. Circuits Syst., vol. 25, no. 12, pp.2765–2774, Dec. 2006.
[16] J. D. Anderson, Fundamentals of Aerodynamics, 2nd ed. New York: McGraw Hill, 1991
[17] TCAD Raphael User’s Guide, Synopsys.
[18] D. James,Chipworks, "Intel Ivy Bridge unveiled - the first commercial tri-gate, high-k, metal-gate CPU," IEEE CICC, pp. 1-4, 2012.
[19] M. N. O. Sadiku, Elements of Electromagnetics.: Oxford Univ. Press, 2011.
[20] BSIM-CMG [Online]. Available : www-device.eecs.berkeley.edu/bsim
[21] TCAD Sentaurus User’s Guide, Synopsys.
[22] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices. Cambridge, U. K.: Cambridge Univ. Press, 2009.
[23] C. Auth, et al., “A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors,” Proceeding of Sym. on VLSI Tech., pp. 131-132, 2012.

TaeYoon An received a B.S degree from the Department of Semiconductor Systems Engineering of Sungkyunkwan University, Suwon, Korea, in 2013. He is currently pursuing an M.S. degree at the College of Information and Communication Engineering of Sungkyunkwan University. His research interests are device analytical modeling and circuit-level performance prediction.

Kyungkeun Choe received a B.S degree from the Department of Semiconductor Systems Engineering of Sungkyun-kwan University in 2013. He is currently pursuing an M.S. degree at the College of Information and Communication Engineering of Sungkyunkwan University. His research interests are device analytical modeling and circuit-level performance prediction.

Kee-Won Kwon received a B.S. degree in metallurgical engineering from Seoul National University in 1988. He also received an M.S. degree in electrical engineering and an Ph.D. degree in materials science and engineering from Stanford University, Stanford, CA, in 2000 and 2001, respectively. From 1990 to 1995, he worked for Samsung Electronics, Giheung, Korea. In 2000, he worked for Maxim Integrated Products, Sunnyvale, CA. He rejoined Samsung Electronics in 2001 and worked in high-performance DRAM design, including work on Rambus DRAM and XDR DRAM. In 2007, he joined Sungkyunkwan University, where he researches memory IP design and low-power, high-speed circuit solutions for analog and mixed-signal devices.

SoYoung Kim received a B.S. degree in electrical engineering from Seoul National University in 1997, and M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1999 and 2004, respectively. From 2004 to 2008, she worked for Intel Corporation, Santa Clara, CA, and from 2008 to 2009, she worked for Cadence Design Systems. She is currently an Associate Professor in the Department of Semiconductor Systems Engineering of the College of Information and Communication Engineering of Sungkyunkwan University. Her research interests include device and interconnect modeling, signal integrity, power integrity and electromagnetic interference in electronic systems.