Hindawi
Complexity
Volume 2022, Article ID 8658770, 11 pages
https://doi.org/10.1155/2022/8658770

WILEY | Hindawi

Research Article

Perimeter Degree Technique for the Reduction of Routing Congestion during Placement in Physical Design of VLSI Circuits

Kuruva Lakshmanna,[1] **Fahimuddin Shaik**,[2] **Vinit Kumar Gunjan**,[3] **Ninni Singh**,[3] **Gautam Kumar**,[4] **and R. Mahammad Shafi**[5]

[1]*Department of Information Technology, Vellore Institute of Technology, Vellore, India*
[2]*Department of Electronics & Communications Engineering, Annamacharya Institute of Technology & Science, Rajampet, India*
[3]*Department of Computer Science & Engineering, CMR Institute of Technology, Hyderabad, India*
[4]*Department of Computer Science & Engineering, CMR Engineering College, Hyderabad, India*
[5]*Department of Electrical and Computer Engineering, College of Engineering and Technology, Tepi Campus, MIZAN-TEPI University, Tepi, Ethiopia*

Correspondence should be addressed to R. Mahammad Shafi; mahammadshafi.r@mtu.edu.et

Received 7 March 2022; Revised 6 April 2022; Accepted 12 April 2022; Published 27 April 2022

Academic Editor: Shahzad Sarfraz

When used in conjunction with the current floorplan and the optimization technique in circuit design engineering, this research allows for the evaluation of design parameters that can be used to reduce congestion during integrated circuit fabrication. Testing the multiple alternative consequences of IC design will be extremely beneficial in this situation, as will be demonstrated further below. If the importance of placement and routing congestion concerns is underappreciated, the IC implementation may experience significant nonlinear problems throughout the process as a result of the underappreciation of placement and routing congestion concerns. The use of standard optimization techniques in integrated circuit design is not the most effective strategy when it comes to precisely estimating nonlinear aspects in the design of integrated circuits. To this end, advanced tools such as Xilinx VIVADO and the ICC2 have been developed, in addition to the ICC1 and VIRTUOSO, to explore for computations and recover the actual parameters that are required to design optimal placement and routing for well-organized and ordered physical design. Furthermore, this work employs the perimeter degree technique (PDT) to measure routing congestion in both horizontal and vertical directions for a silicon chip region and then applies the technique to lower the density of superfluous routing (DSR) (PDT). Recently, a metaheuristic approach to computation has increased in favor, particularly in the last two decades. It is a classic graph theory problem, and it is also a common topic in the field of optimization. However, it does not provide correct information about where and how nodes should be put, despite its popularity. Consequently, in conjunction with the optimized floorplan data, the optimized model created by the Improved Harmonic Search Optimization algorithm undergoes testing and investigation in order to estimate the amount of congestion that occurs during the routing process in VLSI circuit design and to minimize the amount of congestion that occurs.

1. Introduction

However, there are several limitations to Significant Level Synthesis that must be taken into consideration. Significant Level Synthesis is swiftly becoming the industry standard for the VLSI approach. One of the challenges that needs to be solved is congestion throughout the steering cycle of bespoke chips and FPGA-based designs. The steering block is not incorporated in the VLSI plan, despite the fact that it is an openly stated idea elsewhere. Even though it has been a concern in the past with normal HDL-based designs, it has reached a level of severity that is unprecedented [1] in an instance of Considerable-Level Synthesis. Because of this, the most effective course of action is to anticipate the block issue as early in the planning phase as is reasonably possible before it occurs. The implementation of a blocking method

leaves the computerized switch with only a limited number of routing alternatives in the event of a failure. SLS, while fast becoming the industry standard for the VLSI strategy, has a number of disadvantages that must be considered. Concerns about congestion in steering cycles for bespoke chips and FPGA-based designs, among other things, are being raised by the industry. It is not typical in other designs to have a steering block, but the VLSI architecture does not have one. Previously, it had been a difficulty for classic HDL-based designs, but with Considerable-Level Synthesis, the severity of the problem has increased significantly [1]. Rather than waiting until the last minute, it is preferable to plan for the problem at a higher level rather than at the lowest one. As a result of the stringent time limits imposed by blocked nets and computerized switchbacks, the computerized switch is left with few options for routing a blockage plan when dealing with a blockage. Recently, it has been shown that steering blocks can cause robotized steering measure spans to get corrupted and diminish the yield of final results and induce director cycle discontent in plans where there is a significant amount of steering congestion. Despite the availability of cutting-edge EDA instruments, they are unable to completely mitigate the negative impact on the shoot caused by the expansion in the multidimensional nature of computerized plans and the scaling of innovation that occurs as a result of the presence of a directing block during the production.

The use of High-Level Synthesis (HLS) by architects and equipment makers has gained in popularity in recent years, particularly among the former. The most advanced EDA streams have likewise solidified HLS-based planning methodologies, elevating them to the top of their respective categories. High-level dialects such as C++, SystemC, and OpenCL (Open Computing Language) are examples of high-level dialects that can be recognized by a computerized cycle and turned into an RTL plan, which may then be used in electronic circuit design. This method can then be completed by the use of a field-programmable gate array (FPGA). FPGAs have limited resources in terms of logic cells and interconnects, which are used to design power supplies, clocks, and signal nets, and these resources are consumed quickly as the number of logic cells and interconnects increases.

When asset utilization is significant or the plan is particularly sophisticated, an inblock is created in the plan usage stream throughout the steering cycle, which must be resolved in order for the plan to be executed successfully. When this steering block is activated, it allows the rails to be skipped, and it is responsible for guiding the vehicle. On rare occasions, the equipment may even become inoperable, resulting in the failure of the overall plan and the disruption of the utilization cycle as a result. This will result in more complex decision-making procedures and longer planning cycles being implemented as a result of the current scenario. Directed-block messages and reports contain just information on the blocked cells and congestion windows, and they do not contain any other information about the network. In order to remedy the issue, the author must first determine which piece of the substantial level code is causing this steering block. Unfortunately, there is no easy-to-find relationship that can guide him or her through this process. However, despite the fact that these ambiguous netlabels may be seen in RTL representations of the plan, there is no clear connection between them and the sophisticated rules that govern the formation of these nets.

For the most part, we are willing to work on creating a link between the HLS code and the Computational Logic Blocks located on the real-time chip area in order to approximate congestion for the streamline that shows the means by using the recommended IHS method and the ICCII tool, which is currently in the process of being developed. Because the Dataflow approach could only handle a small number of macroblocks at a time, it was slower and could not forecast congestion in both the horizontal and vertical directions, as the Flyline method did. The acronym ICC stands for Integrated Circuit Compiler, and it is a sophisticated VLSI CAD tool that generates simulation results with corresponding input files and provides detailed information about the density of congestion by various methods, which is useful for optimum placement of macroblocks and relatively short-length routing among the blocks. The optimal architecture of a benchmark circuit developed from the IHSAlgorithm is used as a significant input for the ICC tool in this research; in this study, the ICC tool receives independent inputs from the number of macroblocks and their corresponding pins made available in the architecture. In the course of the scheduled stream, data created by a large number of apparatuses is collected, and the outcome is a correlation between the increased level of code on the chip area and the number of windows that are blocked. The use of this simulated data allows us to predict routing congestion among compute blocks and their pins, which helps us to anticipate the area where we might be able to obtain a higher density of routing channels on the chip and reduce obstruction using various obstruction approaches. When processing blocks and the pins that connect them are analyzed, it becomes possible to establish whether there is routing congestion between them.

Wiring is used to produce the clock and signal nets, which are then connected together to form a classic standard cell layout. Each of them makes use of the same network resources as the others. In a typical design, as the number of cells increases, the rivalry for desired routing resources becomes much fiercer. This is due to the fact that the electrical characteristics of metal wires do not scale well with an increase in the number of cells. A rise in routing congestion, as well as a decline in the overall quality of design work performed, resulted as a result of these developments. The majority of traditional design techniques begin with the synthesis of the power supply and clock networks before moving on to the synthesis of the signal routing networks and so on. Despite the fact that power supplies and clock networks do not perform any logical operations, they are crucial in supplying power and timing support to the circuitry that does. In the process of building the power supply network, the design's current requirements, the supply voltage's permissible noise limits, and the electromigration constraints are all taken into consideration. It is the usage of

an uneven grid that has been used in the design of this network. In accordance with standard operating practice, all routing resources are normally available before any development of a power supply network can be completed, let alone begin. A more flexible routing scheme for clock nets can be implemented after the power supply grid as a result of the fact that the power supply grid consumes some of the available routing resources. When it comes to synchronization, the clocks that are used to synchronize the sequential elements of the design must meet stringent requirements for signal integrity and skew, among other things, in order to perform properly. In order to meet their higher latency and skew requirements, high-end systems typically make use of clocking technologies such as grids. When it comes to mainstream designs, grids are often implemented as trees in order to meet more stringent criteria. Clock wires are usually protected or spaced apart to avoid the clock waveform from being affected by signals on neighboring lines, which can cause errors. Routing resources, on the other hand, are required in order to achieve both shielding and spacing. The signal nets are the last to be routed after the power supply and clock wires have been routed, and they can only make use of the routing capabilities that have been left over after the previous routing procedures. Congestion in the routing protocols of these networks can cause severe performance degradation. Apart from evaluating congestion, it is possible to use the method provided in this research to analyze the decrease in chip size and operation time for various design types, in addition to evaluating congestion.

When inserting macroblocks, the IHS method is used to maximize chip area and routing wire length by minimizing the number of routing wires. It was decided to combine the Particle Swarm Optimization Algorithm with the Harmony Search Algorithm in order to produce the IHSAlgorithm. The IHS Algorithm is the outcome of combining Harmony Search (HS) with Particle Swarm Optimization approaches to get optimal performance. Combining the Harmony Search (HS) algorithm with the Particle Swarm Optimization (PSO) algorithm is accomplished through the use of a forward-cascading technique. It was decided to merge HS and PSO because their separate best results were so similar. Even though PSO has a slower convergence rate than HS, it is capable of producing answers that are nearly as good as those given by the latter. The Improved Harmony Search (IHS) Algorithm is presented for use in VLSI Physical Design Automation Floorplanning in order to obtain the required performance while maintaining the required speed and accuracy. In addition to causing death and injury, traffic congestion has the potential to cause a wide range of other catastrophes. As a result of this decision, the overall performance of the design, for example, may be compromised in some way. If the design is not followed to the letter, it is possible that lower working conditions exist. In the sections that follow, you will find in-depth examinations of each of the themes listed.

Because wire delays are no longer straightforward in modern process technologies, increased net delays on essential channels may cause a design to fail to fulfill its frequency goal as a result of increased net delays on important paths. A sudden increase in latency time on a network is frequently caused by unanticipated routing congestion that was not anticipated beforehand. Congestion is one of the many elements that can have an impact on net delay in a variety of different ways. The use of more robust metal layers in network routing will almost likely result in an increase in network latency as the number of metal layers used grows. In order to avoid congested areas, it may be necessary to introduce a detour into the network's routing system, which will be sent to the rest of the network. Because of this detour, both the net and the driver will be significantly delayed as a result of the delay.

Making a large number of vias in order to identify the shortest way across (or complete thorough routing in) an extremely densely populated area may result in a significant increase in the total network delay as a result. Due to the fact that the wire route is located in a region with a high population density, it may be more susceptible to interconnect crosstalk, resulting in greater variations in net delay fluctuations. A more sophisticated and effective simulation tool was used throughout the course of this project in order to evaluate and estimate the required parameters. Input files for the ICC tool include the Optimized BMCArchitecture from IHSAlgorithm, which is included in the ICC tool's output files. The IHSAlgorithm creates an architecture that requires the least amount of chip area and the shortest routing wire length possible with 1500 iterations.

When routing long or time-critical nets, global routers that are driven by timing will aim to route them on the lower resistive levels, where the reduced wire delays can compensate for the via stack penalty, rather than on the higher resistive layers, as opposed to the higher resistive layers. Lower layers with more damage resistance may be necessary for some of the vital nets that are routed later on as a result of the presence of other (perhaps crucial) nets that occupied those desired layers in the previous configuration. The routing of crucial nets may be placed on lower layers of the network design, which may result in time violations on paths that pass through these nets being triggered by growing delays on paths that pass through these nets. It is possible that detours to avoid congested places will lead both the net and its driver to be delayed, causing both of them to be late for their appointments. In spite of the fact that the latency of an unbuffered network increases in a quadratic fashion as the network's length increases, even when employing a simple (lumped parasitic) delay model.

2. Review of Literature

In this study, the goal was to devise a strategy for increasing the responsiveness of directors to location requests. As a result of this technique's situational and guiding coadvancements [2], it is possible to cope with diversity, contamination, and imperfection in a methodical manner. When identifying concerns connected to blocks, planners can use the methodologies described in [3] to narrow their search. Large-scale layout, as well as block dissection and analysis, are all possible with this technique. According to the paper, three areas were specially mentioned: the

automated era of the information highway format, enhanced coordination of planning, and force enhancements. It is necessary to combine numerous upper layers in order to fit a design. There is a graphical user interface for blend and effect measurement with lithography awareness. The implications of merging group and arrangement requirements on succession pair portrayal are discussed in this work, which results in a significant reduction in the arrangement space and a significant boost in computing speed. Scientists were investigating both time-saving and traditional methods of allocating level shifter districts [4, 5] while working on the project's design stage. They fail to take into account the fact that clock-network swapping contributes to more than 30% of total strength, which is significant. Several approaches have been taken to solve the issue of increasing the absolute unique force in place for large-scale integrated circuit systems, and new methodologies and methods have been established [5, 6]. An approach known as circular pressing trees, which is a floorplan visualizing technique that may be utilized to solve the full-scale problem, has also been discussed in detail. This design strategy allows for the placement of CLBs in turns or around chip restrictions, depending on the requirements. Longer wires are produced as a result of streamlining large-scale directions, and steering congestion is reduced as a result of the reduction in steering congestion. Using plan space analysis of low-power adders, we were able to carry out a comparative study of physical format and come up with some interesting results. The evaluation of the Location and Route Streams of Aware Synthesis is carried out and the result is created. Considering large-scale blended size arrangements, [7] examines an intriguing computation that is based on a heuristic in order to arrive at a convincing conclusion. Four steps must be completed in order for the procedure to be successful: assembling the items into blocks, predicting where the blocks will be placed on a floor, and increasing the wire length for good transport. Streaming [8] is able to solve some of the challenges that have been experienced by utilizing wire length advancement in conjunction with large-scale blended measured circuit design. The focus of future research should be on routability and full-scale augmentation of arrangement for advanced circuit designs based on location, time, force, and warm-determined augmentation of arrangement, as well as full-scale augmentation of arrangement. In this study, the ways of robotized floor arranging are investigated, which is critical for the achievement of effective plan space research in order to be successful. There are also some proposals for increasing the usefulness of the present floor planning tools [9], which are discussed in more detail below. The implementation of the numerous improvements that can be made on broad plan areas can be facilitated through the use of an integrated change framework [10]. Cloning and altering the register situation and retiming the register are all accomplished with entire concentration and dedication. The introduction of a new revolution power to deal with the problem of full-scale direction in a conspicuous blended size condition is necessary when dealing with the problem. A cross potential model is also offered in order to develop the turn opportunity when in a position [1]. Combination tactics are presented in [11] for reducing wire delay for a substantially reconfigurable processor in the center of spot and course instruments, as well as an updated synthesizer, in order to reduce wire delay for a substantially reconfigurable processor in the center of spot and course instruments, as well as an updated synthesizer (HLS). In part because of the wire delay [11], it has been possible to reduce the expanded amalgamation time by a significant amount. In [12], a module position instrument is created by coordinating the computations of two key powers, which are, respectively, the KK and the FR, resulting in a module position instrument. The cover between standard cells has been removed using an adjustable and powerful blended size legitimization conspiracy, which we developed. Ultimately, a technique known as sliding-window-based cell trading is utilized to reduce the length of the wire after everything has been said and done [13]. Using a unique enlarged imperative chart, it is illustrated in [14] that it is possible to reduce division that has previously been preset or pushed on full-scale cells. According to our findings, one of the disconnection choices would be beneficial in minimizing the quantity of datapath exchanging that was causing overhead in terms of deferral, force, and zone; therefore, it was applied. A disengagement technique that makes use of inventory gates to reduce the costs associated with detaching hardware from a system is discussed in [15] in order to reduce the costs involved with detaching hardware from a system. An approach to designing and producing three-dimensional integrated circuits that takes into account the building elements of the circuit architecture is described in [16]. After taking into consideration the outcomes of the research, it will be important to put this model to the test in order to see how well it works. With the help of the TSV region and the congested mindful layout, a variety of techniques to evaluate findings can be put into practice.

In cases where there are a significant number of elements that can be ordered, floorplanning [17] techniques can be utilized to efficiently organize the required blocks. In this floorplanning, the methodologies used are linked to situational solutions in a planned stream, which answers the layout challenge by providing an answer to it. In addition, circuit designers that demand complete manual control over their circuit designs can benefit from these techniques. It is necessary to utilize a subjective discovery standard cell placer first in order to identify the primary problem, and then the floor planner is employed in order to remove the cover from the standard cell. Wire lengths have been cut by half, or even by 10%, in some situations, in order to save money. In [18], Rent's criteria for determining interconnection power consumption were applied to determine interconnection power consumption. When compared to area streamlined circuits, power consumption is reduced by 72.9 percent overall, with 44.4 percent zone overhead. When compared to area streamlined circuits, power consumption is reduced by 56.0 percent overall, with 44.4 percent zone overhead. Using a model for exact postpones inquiry in large-scale cell location calculation, it is possible to meet the needs of route deferred traffic. It is able to provide superior outcomes in terms of route latency because of the iterative

and consistent character of the technique. Using a delicate full-scale scenario in conjunction with a resynthesis strategy for optimizing region and timing, this novel chip design technique [19] has been developed. Among the three advances described in [20] are early floor planning, design-driven rationale mix, and postdesign resynthesis, to name a few. It is being researched to see if these two calculations can be merged into a single piece of equipment. When the data were compared to the existing scholarly stance gadget [21], the results were mind-blowing. According to [22], the absolute wire length and area of the following floorplan are governed by the following design.

Through the use of cell inflation techniques, it is possible to reduce the pin density in congested areas by increasing the "virtual" size of cells. This enables fewer cells to be put into congested areas, resulting in a lower pin density. Despite the fact that designers have long deployed tactics that are similar to design automation, design automation was the first to propose them [23, 24]. Despite the fact that it is in the context of programmable metal gate arrays. Following that, they were grouped in a normal cell-based arrangement and displayed one after the other in a gallery setting. The use of cell inflation was found to be effective in alleviating congestion in a simulated annealing environment. One of the most significant discoveries in this study is the use of a monotonically rising function of congestion as a target for placement improvement. c is the difference between routing demand and supply at any given location as specified in terms of routing tracks per unit area, and it is this difference that serves as the basis for the objective function that they utilize. An additional contribution was the development of an expression for the impact of padded cell moves on congested networks, which was based on the net bounding box model [25]. This enables them to calculate the exact amount of space required by each cell. When it comes to determining how much inflation each particular cell requires, however, more empirical procedures are employed. In this work, cell inflation is incorporated into a quadratic placement mechanism that resembles a Gordian knot. With the star model, it is possible to predict congestion for the two-pin Steiner segment. Congestion in each division is determined by taking into consideration the calculated routing demand and the available routing supply for that division (after routing blockages are taken into account). At the completion of the partitioning iterations, this congestion estimation is performed for the first time to determine how much congestion exists. During the previous k partitioning iterations, the congested partitions' cells have been empirically enlarged, and the quadratic placement procedure has been performed using the inflated cell sizes. During greedy congestion optimization, congested cells are shifted to sparse partitions via a series of ripple moves, which are performed in succession. Rather than using a curved path to transport cells, a straight line is formed from the most congested global placement bin to the least congested one. Cells are eagerly transferred to subsequent bins along the line, beginning with the most congested. Straight-line trajectory generation and cell movement are carried out several times before the final legalization is activated. All components of congestion-driven placement are summarized in one diagram. [BR03] describes the Bonn Place quadratic placement method, which makes use of cell inflation. This page goes into great detail about how much inflation is required for each cell in the body. Create Steiner topologies for the interpartition networks at any point during the placement process, and distribute them probabilistically over all possible two-bending ("LZ") routes. In order to accomplish this, Steiner topologies for the interpartition networks can be created at any time throughout the placement process [26, 27]. The pin density of cells within a partition is used to estimate network congestion produced by an intrapartition network partition in order to approximate network congestion caused by an intrapartition network partition. Comparing the accuracy of the heuristic placement approach to the quadratic placement method, which makes use of inflated cell sizes by rerunning the final few partitioning rounds with the inflated sizes, the heuristic placement method is superior. Instead of employing inflated cell sizes, local repartitioning shifts cells from dense partitions (which are represented by inflated cell sizes) to sparse neighboring partitions in the same region as the original partition (which is represented by normal cell sizes). The fact that BonnPlace employs a similar repartitioning technique after each quadrisectioning loop eliminates the need to be concerned about incompatibility problems. As a result of this partitioning stage, all two-two windows in congestion in their respective windows result in an alphabetical listing of all two-two windows with at least one congested partition in their respective windows. Combining the wire length and the maximum congestion of a window, we can build the repartitioning goal function, which is then optimized to provide the best results. Whenever the partitions of a window are accepted for acceptance, the sort keys of the partitions are also modified to reflect the acceptance. A concise summary of the entire congestion-driven placement process can be achieved by employing this technique.

3. Methodology

Synthesis is a transactional technique for transforming an HDL coded design module into a netlist, which is a description of the connectivity of a digital circuit; it consists of a list of the electronic components in a circuit as well as the connecting nodes. The synthesis technique is used extensively in this work to determine the highest possibilities of an IC design with optimum congestion. The design compiling software used in this study is the ICC tool; the input files provided to this tool are a BMCArchitecture with optimal placement, the number of macroblocks in architecture, and the number of pins associated with the blocks.

We hope to reduce routing density (routing congestion) in high-density and recursive places on the chip in both horizontal and vertical directions by utilizing the Pin Density Technique in conjunction with the ICC tool during the placement and routing stage of VLSI Physical Design Automation.

(i) The amount of interbin nets that exist within a bin that has at least one pin should be taken into consideration when determining the perimeter degree of the bin.

(ii) The presence of pins within the bin on two different nets, $n2$ and $n4$, which are also connected to cells outside of the bin is permissible. $N2$ and $n4$ are examples of such nets.

(iii) Its circumference is equal to $2(W+H)$, and there are two nets on either side of the bin to keep the contents contained. Because the center bin is so small, it has the smallest feasible perimeter degree of $1/(W+H)$.

(iv) Flyover nets and intrabin nets (such as n1 in our example) are not included in this statistic, which means that they are not taken into account when calculating the overall efficiency (such as net $n3$).

(v) It follows as a result of this that congestion induced by short local networks is completely ignored, and only a fraction of global congestion is represented.

(vi) Because it captures projected congestion along the exterior of the bin rather than within it, it differs from the pin density metric in that it catches predicted congestion along its perimeter rather than within it.

(vii) Through the use of Rent's rule, a relatively efficient approximation can be obtained for this measure. When inserting, the perimeter degree was used to help reduce traffic congestion.

The main goal of the proposed work is to identify regions of high dense and recursive routing in chip areas in both horizontal and vertical directions and try to minimize routing density (routing congestion) by using Pin Density Technique along with the ICC tool in VLSI Physical Design Automation placement and routing stage.

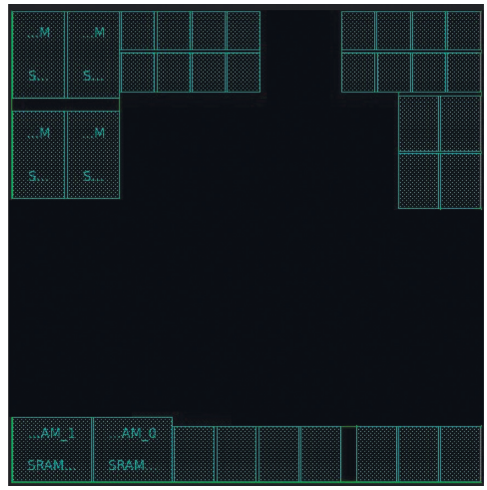

Figure 1: Simulated architecture.

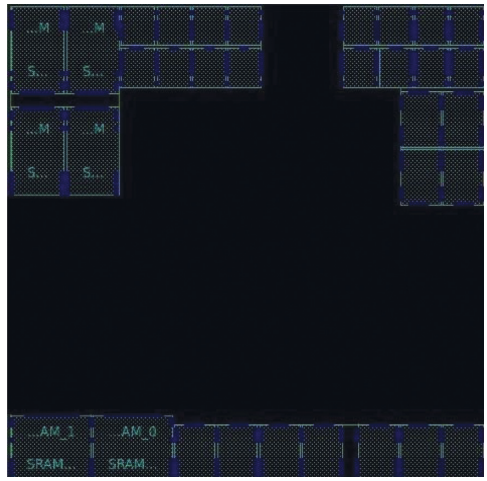

Figure 2: Simulated architecture with pins.

4. Simulation Results

Input, which is the design that was used to complete the floorplan using the Improved Harmonic Search Optimize technique, is applied after architecture, which is the final floorplan created using the Improved Harmonic Search Optimize technique, and the tool accepts it as input and arranges it, which is the final floorplan created using Improved Harmonic Search Optimize technique (see Figures 1and 2).

The values of H routing and V routing represent the total number of nodes among the macroblocks where the greatest cross-path routing occurs during the Global Routing phenomena. In accordance with tool standard methods, the pin positions and cell sizes of blocks. In addition to modeling the tool, each macroblock or CLB (computational logic block) on each of the macros' faces and the number of accessible pins for each of the macros' faces are reported (see Figure 3).

A blue box surrounds each macro or computational logic block (CLB) pin, while green rectangles and square boxes encircle the necessary blocks. In order to properly allocate chip space and pins to blocks, the tool uses a predetermined approach that is integrated into the design process. The "report congestion" command causes the program to generate a report for the BMCircuit as a result of the command. A visual representation of an initial report on congestion incorporates architectural characteristics. The estimation of horizontal and vertical routing resources, as well as the assessment of total routing resources, are revealed in the postsimulation findings. The program also provides overflow totals for H-Routing and V-Routing, as well as maximum overflow for both directories, as well as the same predictions for Global Routing Congestion.

In addition to moving macroblocks and computational logic block (CLB) faces around, we can also add pins to the faces of the blocks using this tool. This request results in the construction of the graphic shown above, which illustrates an estimation of congestion as well as the distribution of on-chip density through the use of various colors to depict the estimation of congestion and distribution of on-chip density (see Figure 4).

```
Layer     |     overflow     |              # GRCs has
Name      |  total   |  max  | overflow (%)       | max overflow
-----------------------------------------------------------------
Both Dirs |       0  |     0 |       0  ( 0.00%)  |       0
H routing |       0  |     0 |       0  ( 0.00%)  |       0
V routing |       0  |     0 |       0  ( 0.00%)  |       0

1
icc2_shell>
```

Figure 3: Initial part of the simulation report for the optimized benchmark.

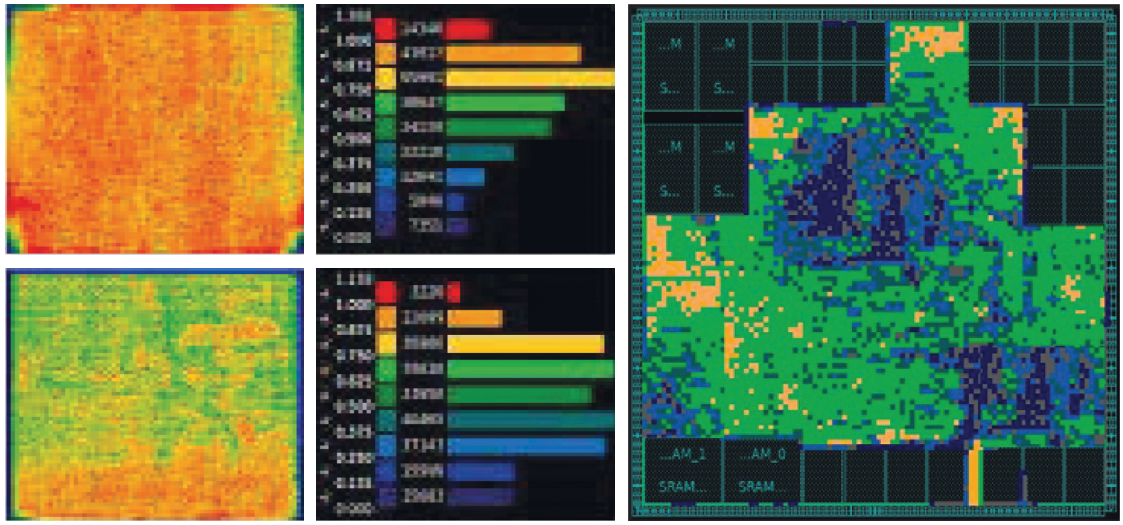

Figure 4: Congestion distribution on chip area.

Congestion is symbolized by four different colors, each of which represents a different level of congested traffic flow. Pink represents less congestion, blue suggests moderate congested conditions, yellow indicates severe congested conditions, and red denotes the most severe congested conditions, according to the color scale. The pins and locations that are the most congested at any given time are depicted in the figure. The IC design process becomes increasingly congested as a result of the use of this technique (CLBs). ICC II presents a technique to reduce congestion in a single design by utilizing the Perimeter Degree Congestion Technique, which is implemented in ICC II. Following the placement of blocks, we may receive a congestion report for the corresponding BMCircuit with the attainment of the H-Routing value of 20421, also attaining a V-Routing value of 18524, and a total overflow attained in the entire process is of 38945, as seen in the image below. Following the release of the BMCircuit Global Routing Congestion report, the overall overflow congestion value was 15798, which is 4.89 percent for the horizontal direction and 2.98 percent for the vertical direction, with a total overflow of 15798 (see Figure 5).

In order to alleviate this congestion, according to the first simulation results, the Perimeter Degree Congestion Approach and the Cell Spacing Congestion Technique are the only approaches that may be used. ICC II's "report congestion" command has an option called "Perimeter Degree" that you can use if you want to relieve congestion by making only minor changes to the position of blocks in your program (see Figure 6).

Simulation results demonstrate that a BMCircuit with an H-Routing value of 521, a V-Routing value of 2584, and a total overflow of 3105 is less congested than a BMCircuit with an H-Routing value of 521, a V-Routing value of 2584, and a total overflow of 3105. According to the BMCircuit Global Routing Congestion report, the network is experiencing 0.22 percent horizontal congestion and 0.09 percent vertical congestion, for the attainment of a total overflow congestion value of 0.56 percent. H-Routing value of 515, V-Routing value of 2132, and the total amount of overflow attained of 2647 indicate that the network is experiencing 0.22 percent horizontal and 0.09 percent vertical congestion (see Figure 7).

A BMCircuit with H-Routing values of 614 and V-Routing values of 3039, as well as a total overflow of 3653, is used in this simulation report to demonstrate how congestion might be minimized. There were a total of 3115 overflows, accounting for 0.22 percent of overall overflow congestion in the horizontal direction and 1.9 percent in the vertical direction, for a total of 0.56 percent of overall overflow congestion in the horizontal direction, according to the Global Routing Congestion report for BMCircuit.

```
icc2_shell> report_congestion
****************************************
Report : Congestion
Design : Optimized_HP_BMC
Version: M-2016.12
Date   : Thu Jan 20 14:15:32 2022
****************************************

Layer      |    overflow     |              # GRCs has
Name       |  total  |  max  | overflow          | max overflow
-------------------------------------------------------------
Both Dirs  |  38945  |  309  |   15798           |     1
H routing  |  20421  |  127  |   9812            |     1
V routing  |  18524  |  309  |   5986            |     1

1
icc2_shell>
```

Figure 5: Simulation report before Perimeter Degree Congestion Technique.

```
icc2_shell> report_congestion
****************************************
Report : Congestion
Design : Optimized_HP_BMC
Version: M-2016.12
Date   : Thu Jan 20 14:15:32 2022
****************************************

Layer      |    overflow     |              # GRCs has
Name       |  total  |  max  | overflow          | max overflow
-------------------------------------------------------------
Both Dirs  |  3105   |   4   |     2647          |     28
H routing  |  521    |   1   |     515           |     8
V routing  |  2584   |   4   |     2132          |     28

1
icc2_shell>
```

Figure 6: The postsimulation results, which show a significant reduction in the design and related simulation report congestion.

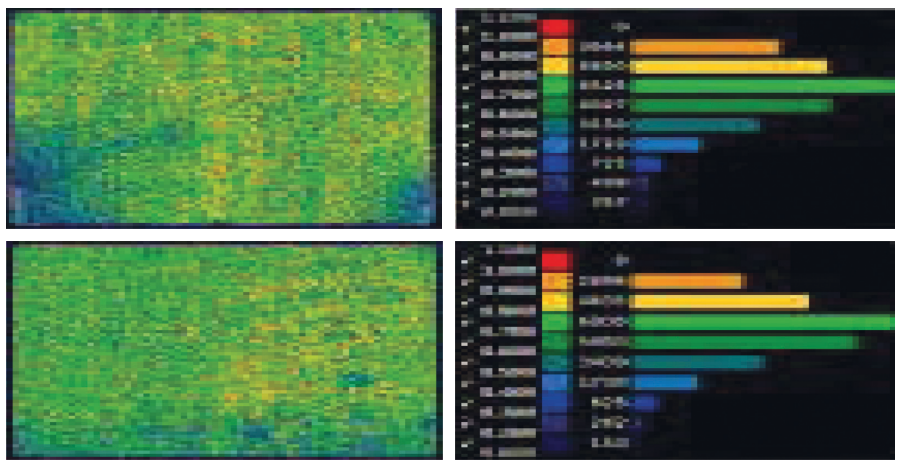

Figure 7: Simulation report after Perimeter Degree Congestion Technique.

5. Comparative Analysis

The Pin Density Technique differs from previous strategies in that it allows the pin count to be adjusted in accordance with desired architecture limits. It has also been shown to be more effective than other techniques for reducing congestion. Dataflow analysis and fly line analysis were used to compare the simulation results of our suggested congestion technique; a table comprising overflow attributes in the H and V directions, as well as total overflow and maximum

Table 1: Parametric Comparison of the Proposed and existing methods in the field.

	Existing techniques		Proposed technique
	Maze routing analysis	Density analysis	Perimeter degree technique (PDT)
H- overflow	9	218	515
V -overflow	219	250	2132
Total amount of overflow	178	344	2647
Maximum amount of overflow (1GRC)	22	22	28

Table 2: Statistical Comparison of several metrics before and after the proposed congestion (PDT) estimation technique was used.

Parameters	Before perimeter degree technique (PDT)	After perimeter degree technique
H Routing	20421	521
V Routing	18524	2584
Both directions	38945	3105
Maximum overflow in the H Routing	127	4
Maximum overflow in the V Routing	309	1
Maximum overflow in the both directions	309	4
GRC based overflow values in the H Routing	9812	515
GRC based overflow values in the V Routing	5986	2132
GRC based overflow values in both directions	15798	2647
Percentage of GRC based overflow values in H Routing	3.62	0.21
Percentage of GRC based overflow values in V Routing	2.02	0.88
Percentage of GRC based overflow values in both directions	3.62	0.42
Maximum GRC based overflow value in H Routing	1	8
Maximum GRC based overflow value in V Routing	0	28
Maximum GRC based overflow value in both directions	1	28

overflow per unit Global Routing Congestion, was created. When it comes to anticipating congestion in the chip region, there are two approaches to consider: the PDT approach and the Global Routing Congestion strategy. The PDT Congestion approach is used to estimate congestion in the chip area (GRC).

The technique displays the accomplishment of the objectives in a comparative manner, based on the data in Table 1. According to the findings of a table, the recommended technique produces the best results.

The simulation results for the optimized standard BMCircuit obtained using the suggested congestion estimate approach for the optimized standard BMCircuit are displayed in the table's tabular column, which is displayed in the next section. According to the simulation results, when H Routing and V Routing are combined, there is a significant improvement in the approximation of congestion, as well as in the maximum amount of overflow in the H Routing, the maximum amount of overflow in the V Routing, the percentage of GRC based overflow in the H routing, the percentage of GRC based overflow in the V Routing, the GRC based overflow in the H Routing, and the maximum GRC based overflow (refer Table 2). This combination of traits enabled us to establish the feasibility of our proposed study utilizing a technically and statistically cutting-edge technique, which will be valuable for future experiments and evaluations in this field in the years to come.

In order to make their relevance evident, the results of simulating an optimized BMC with and without the PDT Congestion Technique are shown in Table 2to the right of the text.

6. Conclusion and Future Scope

An in-depth method for calculating and minimizing congestion in VLSI Physical Design Automation, as well as optimization of placement area and routing wire length, is described in this study. By incorporating the proposed Perimeter Degree Congestion Technique (PDCT) into an integrated circuit design, it surpasses existing techniques for forecasting and mitigating congestion density in the H- and V-direction, such as fly line analysis and Dataflow analysis, in terms of performance. Logic communication between macros or Computational Logic Blocks can be achieved through the use of PDT (Programmable Data Transfer) (CLBs). In order to perform this operation, the integrated circuit (IC) tools that were used have proven to be complicated, as well as having user-friendly interfaces that contain a huge number of colorful technical elements while not overlooking even the most fundamental of qualities. The Perimeter Degree Congestion Technique is used to alleviate congestion in places that are logically congested, such as urban areas (PDT). As part of the experimentation, the method under consideration has supplied a standardization for the use of logic procedures in order to perceive the intended aims of the task, which has been useful in the future. In addition, it has been demonstrated to be cost-effective in a variety of ways when used in conjunction with the congestion control process, which is a positive step forward. While the Dataflow approach could only handle a small number of macroblocks and took longer to anticipate congestion, the Flyline technique was more accurate but was unable to estimate congestion in both horizontal and vertical

directions at the same time, whereas the Dataflow method could. Numerous studies have proved the usefulness of this technique in terms of, among other things, lowering wire length, area, and power consumption during the design of integrated circuits. The usage of the perimeter degree technique, which is highly recommended, can help to achieve these reductions in energy consumption. The proposed approach gives better results, but a few additional improvements to the process flow and operational processes can help to avoid the requirement for the development of more complex approaches that can deliver answers in a shorter period of time. In order to accomplish this, a more in-depth study on a wide range of unique characteristics of the integrated circuit design circuit sector can be conducted. Additionally, the suggested method may be used to analyze chip area and operation time reductions for various architectures in addition to evaluating congestion for various architectures.

Data Availability

The processed data are available upon request from the corresponding author.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] S. M. Ahmed, B. Kovela, and V. K. Gunjan, "IoT based automatic plant watering system through soil moisture sensing-A technique to support farmers' cultivation in rural India," in *Advances in Cybernetics, Cognition, and Machine Learning for Communication Technologies*, pp. 259–268, Springer, Singapore, 2020.

[2] I. Ratkovi, O. Palomar, M. Stani, O. Unsal, A. Cristal, and M. Valero, "Physical vs. physically-aware estimation flow: case study of design space exploration of adders," in *Proceedings of the IEEE Computer Society*, Tampa, FL, USA, July, 2014.

[3] S. Karimullah and Dr. D. Vishnuvardhan, "Experimental Analysis of Optimization Techniques for Placement and Routing in Asic Design," *ICDSMLA 2019*, vol. 601, Springer Nature Singapore Pte Ltd, Singapore, 2020.

[4] IC Compiler, *Implementation User Guide Version J-2014.09-SP4*, March 2015.

[5] K. Golshan, *Physical Design Essentials*, Springer Science Business Media, LLC, Heidelberg, Germany, 2016.

[6] S. Karimullah and D. Vishnu Vardhan, "Iterative Analysis of Optimization Algorithms for Placement and Routing in Asic Design," *ICDSMLA 2019*, Vol. 601, Springer Nature Singapore Pte Ltd, Singapore, 2020.

[7] S. Karimullah, D. Vishnu Vardhan, and S. J. Basha, "Floorplanning for Placement of Modulesin VLSI Physical Design Using HarmonySearch Technique," *ICDSMLA 2019*, Vol. 601, Springer Nature Singapore Pte Ltd, Singapore, 2020.

[8] Yi-F. Chen, C.-C. Huang, C.-H. Chiou, Y.-W. Chang, and C.-J. Wang, Routability-driven blockage-aware macro placement," in *Proceedings of the 51st Annual Design Automation Conference*, pp. 1–6, San Francisco, CA, USA, June 2014.

[9] S. Karimullah and Dr. D. A. Vishnuvardhan, *A Review Paper on Optimization of Placement and Routing Techniques"at NC'e-TIMES # 1.0 IN2018*, pp. 2395–1303, IJET ISSN, 2018.

[10] J. Z. Yan, V. Natarajan, and C. Chu, "Handling Complexities in Modern Large-Scale Mixed-Size Placement," in *Proceedings of the 46th Annual Design Automation Conference*, pp. 436–441, NY, USA, July, 2009.

[11] J. Shin, J. A. Darringer, G. Luo et al., "Floorplanning Challenges in Early Chip Planning," in *Proceedings of the 2011 IEEE International SOC Conference*, pp. 388–393, IEEE, Taipei, Taiwan, September 2011.

[12] P. S. Prasad, B. Sunitha Devi, M. Janga Reddy, and V. K. Gunjan, "A survey of fingerprint recognition systems and their applications," in *International Conference on Communications and Cyber Physical Engineering 2018*, pp. 513–520, Springer, Singapore, 2018.

[13] S. Karimullah and D. Vishnuvardhan, "Simulation of optimized architecture for the estimation of congession during placement and routing," *Design Engineering*, pp. 755–764, 2021.

[14] B. Mokhlesabadifarahani and V. K. Gunjan, *EMG Signals Characterization in Three States of Contraction by Fuzzy Network and Feature Extraction*, Springer, Heidelberg, Germany, 2015.

[15] M. Samaranayake, H. Ji, and J. Ainscough, "Module placement based on hierarchical force directed approach," in *Proceedings of the International Conference on Signals, Circuits and Systems*, pp. 1–6, IEEE, Medenine, Tunisia, November 2009.

[16] M. D. Ansari, V. K. Gunjan, and E. Rashid, "On security and data integrity framework for cloud computing using tamper-proofing," in *ICCCE 2020*, pp. 1419–1427, Springer, Singapore, 2021.

[17] M. Thenappan, T. Senthil Arasu, K. M. Sreekanth, and R. S. Guzar, "An overlap removal algorithm for macrocell placement in VLSI layouts," in *Proceedings of the International Conference on Computing: Theory and Applications (ICCTA'07)*, March 2007.

[18] K. Prasanna and M. Seetha, "A doubleton pattern mining approach for discovering colossal patterns from biological dataset," *International Journal of Computer Application*, vol. 119, no. 21, pp. 41–47, 2015.

[19] M. Usman, M. Wajid, M. Z. Shamim, M. D. Ansari, and V. K. Gunjan, "Threshold detection scheme based on parametric distribution fitting for optical fiber channels," *Recent Advances in Computer Science and Communications*, vol. 14, no. 2, pp. 409–415, 2021.

[20] S. N. Adya and I. L. Markov, "consistent placement of MacroBlock using floorplanning and StandardCell placement"" in *Proceedings of the 2002 international symposium on Physical design*, Del Mar, CA, USA, Apri, 2002.

[21] Z. Lin and N. K. Jha, "Interconnect-aware High-Level Synthesis for Low Power," in *Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design*, pp. 110–117, IEEE, San Jose, CA, USA, November 2002.

[22] A. J. Zargar, N. Singh, G. Rathee, and A. K. Singh, "Image data-deduplication using the block truncation coding technique," in *Proceedings of the 2015 International Conference on Futuristic Trends on Computational Analysis and Knowledge Management (ABLAZE)*, pp. 154–158, IEEE, Greater Noida, India, February 2015.

[23] S. Pinge, K. N. Rajeev, and M. Chrzanowska-Jeske, "Fast Floorplanning with Placement Constraints," in *Proceedings of*

the 2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS), IEEE, Cusco, Peru, February 2013.

[24] S. Iyengar and L. Shrinivasn, "Power, Performance and Area Optimization of I/O Design," in *Proceedings of the International Conference on Inventive Research in Computing Applications (ICIRCA 2018)*, Coimbatore, India, July 2018.

[25] J.-M. Lin, W.-Y Cheng, C.-L. Lee, C. Richard, and J. Hsu, "Voltage Island-Driven Floorplanning Considering Level Shifter Placement," in *Proceedings of the 17th Asia and South Pacific Design Automation Conference*, pp. 443–448, IEEE, Sydney, NSW, Australia, January 2012.

[26] S. Karimullah and D. V. Vardhan, "Pin density technique for congestion estimation and reduction of optimized design during placement and routing," *Applied Nanoscience*, pp. 1–10, 2022.

[27] S. Karimullah, S. J. Basha, P. Guruvyshnavi, K. Sathish Kumar Reddy, and B. Navyatha, "A Genetic Algorithm with Fixed Open Approach for Placements and Routings," *ICCCE 2020*, Vol. 698, Springer Nature Singapore Pte Ltd, Singapore, 2020.