# Perspective: Spintronic synapse for artificial neural network ©

Cite as: J. Appl. Phys. **124**, 151904 (2018); https://doi.org/10.1063/1.5042317 Submitted: 31 May 2018 • Accepted: 20 August 2018 • Published Online: 08 October 2018

Shunsuke Fukami and Hideo Ohno

COLLECTIONS

This paper was selected as Featured



Neuromorphic computing with antiferromagnetic spintronics Journal of Applied Physics **128**, 010902 (2020); https://doi.org/10.1063/5.0009482

A comprehensive review on emerging artificial neuromorphic devices Applied Physics Reviews **7**, 011312 (2020); https://doi.org/10.1063/1.5118217

The design and verification of MuMax3 AIP Advances 4, 107133 (2014); https://doi.org/10.1063/1.4899186

## Lock-in Amplifiers up to 600 MHz







J. Appl. Phys. **124**, 151904 (2018); https://doi.org/10.1063/1.5042317 © 2018 Author(s).



### Perspective: Spintronic synapse for artificial neural network

Shunsuke Fukami<sup>1,2,3,4,5,6,a)</sup> and Hideo Ohno<sup>1,2,3,4,5,6</sup>

<sup>1</sup>Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Sendai 980-8577, Japan

<sup>2</sup>Center for Spintronics Integrated Systems, Tohoku University, Sendai 980-8577, Japan
 <sup>3</sup>Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai 980-0845, Japan
 <sup>4</sup>Center for Spintronics Research Network, Tohoku University, Sendai 980-8577, Japan
 <sup>5</sup>Center for Science and Innovation in Spintronics (Core Research Cluster), Tohoku University, Sendai 980-8577, Japan

<sup>6</sup>WPI-Advanced Institute for Materials Research, Tohoku University, Sendai 980-8577, Japan

(Received 31 May 2018; accepted 20 August 2018; published online 8 October 2018)

While digital integrated circuits with von Neumann architectures, having exponentially evolved for half a century, are an indispensable building block of today's information society, recently growing demand on executing more complex tasks like the human brain has allowed a revisit to the architecture of information processing. Brain-inspired hardware using artificial neural networks is expected to offer a complementary approach to deal with complex problems. Since the neuron and synapse are key components of brains, most of the mathematical models of artificial neural networks require artificial neurons and synapses. Consequently, much effort has been devoted to creating artificial neurons and synapses using various solid-state systems with ferroelectric materials, phase-change materials, oxide-based memristive materials, and so on. Here, we review an example of studies on an artificial synapse based on spintronics and its application to artificial neural networks. The spintronic synapse, having analog and nonvolatile memory functionality, consists of an antiferromagnet/ ferromagnet heterostructure and is operated by spin-orbit torque. After giving an overview of this field, we describe the operation principle and results of analog magnetization switching of the spintronic synapse. We then review a proof-of-concept demonstration of the artificial neural network with 36 spintronic synapses, where an associative memory operation based on the Hopfield model is performed and the learning ability of the spintronic synapses is confirmed, showing promise for low-power neuromorphic computation. Published by AIP Publishing. https://doi.org/10.1063/1.5042317

#### I. INTRODUCTION AND BACKGROUND

Current information processing and communication technologies rely on digital complementary metal-oxidesemiconductor (CMOS)-based integrated circuits with the von Neumann architecture. As the technologies advance by increasing the clock frequency and count of the components in circuits, the limit of this approach has risen to the surface year by year in the form of physical scaling limits, significant stand-by power consumption, data-transfer bottlenecks, and so on.<sup>1</sup> In addition, while the conventional approach efficiently completes simple iterative operations, it is not suitable to execute complex tasks such as perception, prediction, and decision making. Consequently, a growing interest is being paid on information processing inspired by the brain, a system that can readily complete such complex cognitive tasks even from an imperfect set of input information.

A scheme to emulate the information-processing mechanism of the brain in software and run it on conventional hardware, *e.g.*, deep neural network, has been fully recognized as a powerful means<sup>2</sup> and has already been implemented as artificial intelligence. While this approach shows high performance that can compete with the human brain,<sup>2</sup> however, it builds on tremendous hardware resources and power supply, inhibiting the expansion of the area where the technology can be utilized. This fact calls for another strategy where sophisticated hardware is employed, which emulates neural networks of the brain to aim at processing information at a lower level of hardware resources and power comsumption.<sup>3–6</sup>

Key building blocks of the brains are the neuron and synapse. The neuron takes a role of information processing; it integrates frequently input stimuli by a membrane potential and fires once the potential reaches a certain threshold. The synapse, on the other hand, takes the role of learning and memorizing; located at junctions between neurons. The connection strength, or synaptic weight, corresponding to the memorized information, is changed in an analog manner through learning. With neurons and synapses, information processing, memorizing, and learning take place locally, in parallel, and asynchronously, in stark contrast to von Neumann architectures. Mathematical models that abstract the aforementioned mechanism of information processing in neural network or artificial hardware where operations based on the mathematical model are executed are referred to as artificial neural networks and are recognized as a key ingredient to realize low-power, high-performance, and adaptive neuromorphic computing beyond the currently used von Neumann architecture-based artificial intelligence.

In order to construct large-scale and low-power artificial neural networks, it is effective to utilize artificial neurons and

a)s-fukami@riec.tohoku.ac.jp

synapses using solid-state devices. Also, since real neural networks comprise a much larger number of synapses than neurons, mathematical models for artificial neural networks mostly require a large number of synapses. It is also noted that, as in the real synapses, the artificial synapses are desired to change their state in an analog manner through learning and store their state in a nonvolatile manner. These facts have led to extensive efforts on realization of compact, analog, and nonvolatile artificial synapses using solid-state devices made of various material systems such as resistance switching materials (or memristor<sup>8</sup>),<sup>9,10</sup> phase change materials,<sup>11</sup> and ferroelectric materials.<sup>12,13</sup> In addition, several demonstrations of brain-like computation have been reported. For example, Prezioso *et al.* showed a classification of  $3 \times 3$  pixels images using a trained  $12 \times 12$  cross-bar network with metal-oxide memristors.<sup>14</sup> Also, Burr et al. showed a classification of handwritten digits using a trained three-layer perceptron network with 164 885 phase-change memory devices.<sup>15</sup>

Spintronics also offers an attractive platform for solidstate device technologies. Spintronics devices inherently achieve fast and virtually infinite information writing operation (magnetization switching) with standard CMOS-compatible voltages and store their state without the use of a power supply. Following magnetoresistive random access memories (MRAMs) utilizing a magnetic-field-induced switching scheme commercialized since 2006,<sup>16</sup> MRAMs utilizing spintransfer torque (STT)-induced magnetization switching (STT-MRAMs) are about to hit the mass market.<sup>17,18</sup> In addition, these features hold promise for high-performance and low-power artificial neural networks that are adaptive through continuous learning and robust against environmental agitation. At the same time, a variety of physical aspects of spintronics devices make them various constituents in artificial neural networks, unlimited to artificial synapses.<sup>19–24</sup> Spintronic or magnetic material systems in general represent digital information as their magnetization direction, e.g., up or down. However, proper engineering of material systems allows one to deal with analog information by their magnetic domain structures, providing opportunities to realize spintronic synapse for high-performance, low-power, and adaptive artificial neural networks.

In the following, we review our studies on a spintronic artificial synapse<sup>25–27</sup> and its implementation to the artificial neural network.<sup>28</sup> The synaptic device is operated by spin-orbit torque [Fig. 1(a)] and consists of an antiferromagnet/ferromagnet bilayer system [Fig. 1(b)], allowing analog control of magnetization state by electric current. For the demonstration of artificial neural network, the Hopfield model, a representative model of neural network, is employed and an associative memory operation is tested. Through this proof-of-concept demonstration, we show that the employed spintronic artificial synapse has functions of learning and memorizing.

#### **II. ARTIFICIAL SYNAPSE**

In this section, we describe the structure, operation principle, and the mechanism that accounts for the analog operation of the developed artificial spintronic synapses.

Viable spintronics devices require an efficient scheme to electrically control magnetization. STT-induced magnetization switching<sup>29,30</sup> in magnetic tunnel junctions is a leading example and has allowed successful development of STT-MRAMs.<sup>17,18</sup> Meanwhile, recent studies have revealed that torque arising from spin-orbit interactions, spin-orbit torque (SOT), also provides a promising scheme to induce magnetization switching. SOT arises when one introduces an in-plane current to magnetic crystals with noncentrosymmetry<sup>31</sup> or magnetic heterostructures with broken space inversion symmetry,<sup>32</sup> which have sizable spin-orbit interaction. The origin of SOT in heterostructures is still under debate and could be different from one system to another. One of the most likely mechanisms is the spin Hall effect, in which charge current is converted to a spin current in the transverse direction to the original charge current<sup>33-36</sup> as shown in Fig. 1(a). The generated spin current accumulates spinpolarized electrons in the adjacent ferromagnetic layer, exerting a torque on its magnetization. Another possible factor is the Rashba-Edelstein effect, in which charged carriers moving in a two-dimensional interface with an effective electric field feels an effective magnetic field in the transverse direction to both the momentum of the carrier and the electric field.<sup>37,38</sup> This eventually causes a non-equilibrium spin accumulation as well. Importantly, both effects give rise to similar torques with two different symmetries:<sup>39,40</sup> a fieldlike torque with  $\mathbf{m} \times \sigma$  symmetry and a Slonczewski-like torque with  $\mathbf{m} \times (\mathbf{m} \times \sigma)$  symmetry, where **m** is the unit vector of magnetization and  $\sigma$  is the spin accumulation vector  $(\sigma \parallel \mathbf{y})$  in case that current flows in the **x** direction). There are three types of SOT switching schemes in terms of magnetic easy axis direction with respect to the applied current (flowing along the x direction); perpendicular (Type Z) scheme,<sup>32</sup> in-plane and orthogonal-to-current (Type Y) scheme,<sup>41</sup> and in-plane and collinear-to-current (Type X) scheme.<sup>42</sup> For Types Z and X structures, the effective field of the field-like torque always points to the y (hard-axis) direction and the switching is driven by the Slonczewski-like torque. Since the effective field of the Slonczewski-like torque has rotational symmetry about the y axis [Fig. 1(c)], breaking the rotational symmetry of the Slonczewski-like torque is necessary to determine the switching direction [Fig. 1(d)], posing an obstacle for integrated-circuit implementation. While several means have been proposed and demonstrated,<sup>43–47</sup> here we describe a method to utilize antiferromagnet/ferromagnet bilayer systems, which leads to the analog control of magnetization and makes it a candidate for artificial synapses.

A large spin Hall effect has been mostly observed in nonmagnetic materials such as Pt,<sup>48</sup> Ta,<sup>41</sup> and W.<sup>49</sup> However, recent theoretical studies pointed out that some of the noncollinear antiferromagnets exhibit a giant anomalous Hall effect, originating from the Berry curvature<sup>50</sup> which is confirmed experimentally.<sup>51</sup> Experimental studies on the inverse/direct spin Hall effect in antiferromagnetic materials have also been performed, and sizable effects have been observed in various systems.<sup>52–57</sup> Antiferromagnet/ferromagnet bilayer systems are also known to exhibit exchange bias, where a unidirectional anisotropy is exerted on the

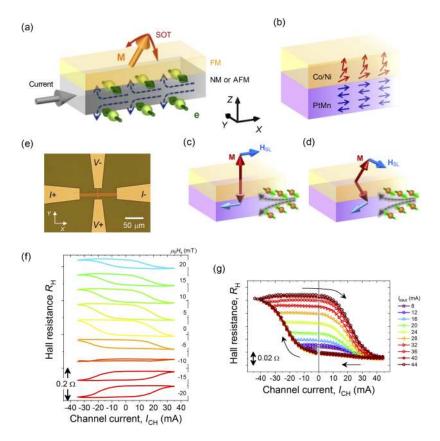


FIG. 1. Field-free and analog switching by spin-orbit torque in antiferromagnet/ferromagnet heterostructure. (a) Schematics of generation of spin-orbit torque in heterostructure. (b) Schematic of antiferromagnet (PtMn)/ ferromagnet (Co/Ni) heterostructure used for an artificial synapse. [(c), (d)] Mechanism of field-free switching. Effective field of the Slonczewski-like spin-orbit torque has rotational symmetry (c) and breaking it by exchange bias achieves field-free switching (d). (e) Optical micrograph of fabricated Hall device. (f) Measured Hall resistance  $R_{\rm H}$  versus applied channel current  $I_{\rm CH}$  under various in-plane external field  $H_{\rm X}$ . (g) Hall resistance field. Increase in current to negative direction is stopped at various current  $I_{\rm MAX}$ . Adapted from Ref. 25.

ferromagnet at the interface.<sup>58</sup> Therefore, combination of these two effects is expected to achieve field-free switching of perpendicular magnetization, where the antiferromagnet plays the role of the source of SOT and the source of in-plane field simultaneously [Figs. 1(b)-1(d)].<sup>25,59</sup> In the following, the experimental results based on this concept<sup>25</sup> will be reviewed.

For this work, antiferromagnetic PtMn and ferromagnetic Co/Ni multilayers were employed. The stack structure was, from the substrate side, Ta(3)/Pt(4)/PtMn (8)/[Co(0.3)/  $Ni(0.6)]_2/Co(0.3)/MgO(1.2)/Ta(2)$  (numbers in parentheses are nominal thickness in nanometers). The films were deposited on high-resistance Si substrate by dc/rf magnetron sputtering. After the deposition, the films were annealed in a magnetic field of 1.2 T along the x direction at 300 °C for one hour. We confirmed from the magnetization hysteresis loop measurement using vibrating sample magnetometer that perpendicular easy axis and finite exchange bias were simultaneously obtained at the PtMn thickness of 8 nm (thinner PtMn resulted in negligible exchange bias whereas thicker PtMn resulted in in-plane easy axis due to too strong exchange bias). The films were processed into cross-shaped Hall-bar devices with a width of  $10\,\mu m$  by photolithography and Ar ion milling, as shown in Fig. 1(e). The channel was fabricated along the x direction, the same direction with the exchange bias. To evaluate the magnetization reversal, the anomalous Hall resistance was measured with a dc current magnitude of 1 mA. The details are described in Ref. 25.

Figure 1(f) shows the Hall resistance as a function of the applied channel current measured at various in-plane magnetic fields  $\mu_0 H_x$  along the x direction ( $\mu_0$  is the permeability in free space). A hysteresis loop is observed at zero magnetic

field. The loop collapses at  $\mu_0 H_x = -10$  mT, meaning that the effective field due to the exchange bias is canceled by the external field. The switching direction reverses above -10 mT. Change in the switching direction indicates that the switching is driven by SOT and finite hysteresis at zero field indicates field-free SOT switching of perpendicular magnetization owing to the exchange bias as expected. We confirmed that the switching direction changes when we reverse the exchange bias direction by reversing the magnetic-field annealing direction, indicating that the exchange bias causes the field-free switching.

We then take a closer look at the current-induced hysteresis loop at zero field. The outer curve in Fig. 1(g) shows the loop obtained by sweeping the current between  $\pm 44$  mA, in the direction indicated by arrows. The inner curves, on the other hand, show the results when the increase of the current in the negative direction was stopped below -44 mA. Depending on the applied maximum current  $I_{MAX}$ , intermediate states of different levels are realized. The intermediate states are found to be stable after turning off the current, which indicates that the present system functions as an analog and nonvolatile memory device, which is expected to be useful as an artificial synapse in artificial neural networks as described earlier. In Sec. III, a proof-of-concept demonstration of an artificial neural network using the analog SOT device will be presented.

We then investigated the underlying mechanism that causes the observed nonvolatile and analog behavior.<sup>26</sup> To examine it, we fabricated dot devices, in which the ferromagnetic Co/Ni multilayer was processed into nanodots with various diameters  $D_{dot}$  from 1 µm to 50 nm and formed on top of a PtMn Hall bar. The channel width  $W_{ch}$  was varied according to  $D_{dot}$ . Figure 2(a) shows the scanning electron

microscopy image of a fabricated dot device with a nominal  $D_{dot}$  of 100 nm. For reference, micrometer-wide Hall devices were also fabricated. The details of the sample fabrication are described in Ref. 26.

Figure 2(b) shows the Hall resistance vs. channel current for devices with different  $D_{dot}$ . The measurement procedure is the same with that for Fig. 1(g). All the measurements were performed at zero magnetic field. The loop for  $D_{dot} = 1 \,\mu m$  is similar to the one for the 5- $\mu$ m-wide Hall device. As  $D_{dot}$ decreases, the loop becomes stepwise and the number of steps decreases. Finally, below  $D_{dot} = 200 \text{ nm}$ , the loop shows a simple binary feature. These results suggest that the Co/Ni dot consists of a number of magnetic domains with different properties that separately switch at different levels of the applied current. By counting the number of intermediate levels for each loop with different  $D_{dot}$ , the size of the domain was derived to be around 200 nm. Meanwhile, the size of crystalline grain was observed to be around 15 nm from cross-sectional transmission electron microscopy, indicating that the domain consists of multiple crystalline grains. A schematic picture inferred from detailed analysis is shown in Fig. 2(c). We found that the magnitude and direction of the exchange bias along both perpendicular and in-plane directions are different among the domains, making the threshold switching current different among them. Also, such variation of exchange bias can stabilize the multidomain states. As a result, each domain switches at different levels of current and resultant multidomain state remains even after the current is turned off, eventually causing the synapse-like analog and nonvolatile property.<sup>20</sup>

The mechanism that stabilizes the multidomain structure has yet to be clarified. It should be noted, however, that such behavior is also observed in other antiferromagnet/ferromagnet bilayer systems.<sup>60,61</sup> Moreover, recent experiments on the electrical switching of antiferromagnets also show similar behavior,<sup>62–65</sup> leading to the inference that the observed analog and nonvolatile behavior may be a common nature of the antiferromagnetic systems.

#### **III. ARTIFICIAL NEURAL NETWORK**

As described in Sec. II, antiferromagnet/ferromagnet bilayer systems operated by spin-orbit torque achieve magnetic-field-free, analog magnetization switching and store the state in a nonvolatile manner, making it a promising building block for an artificial synapse in artificial neural networks. In this section, a proof-of-concept demonstration of an artificial neural network with the spintronic artificial synapse<sup>28</sup> will be described.

As an example of neuromorphic computation, we examined an associative memory operation, which is a typical operation that von Neumann computers struggle with and yet the human brain readily completes. For the associative memory operation, the Hopfield model<sup>66</sup> is used, which is a form of recurrent neural networks, is originally developed from an analogy with spin glass systems, and is known to be useful for the optimization problem. The Hopfield network stores information in a matrix, the so-called synaptic weight matrix, and can robustly associate the closest memorized information with noise-contained inputs by defining an energy function and minimizing the energy. Configuration of each matrix element collectively represents the stored information, where the individual matrix elements take arbitrary analog numbers. To realize hardware

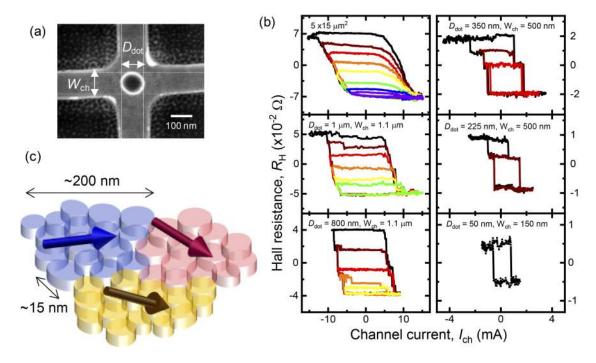


FIG. 2. Mechanism of analog behavior. (a) Scanning electron micrograph of fabricated dot devices with nominal diameter  $D_{dot}$  of 100 nm. (b) Hall resistance  $R_{\rm H}$  as a function of channel current  $I_{\rm CH}$  for microscale Hall bar and dot devices with  $D_{\rm dot} = 1$  mm, 800, 350, 225, 50 nm. (c) Schematic of the texture of crystalline grain and exchange bias direction. Cylinders represent crystalline grains and arrows represent the direction of exchange bias. Reprinted with permission from Appl. Phys. Lett. **110**(9), 092410 (2017). Copyright 2017 AIP Publishing LLC.<sup>26</sup>

executing the Hopfield model-based associative memory operation, artificial analog synaptic devices (or circuit units) are necessary. The work in Ref. 28 was performed based on this concept.

Figures 3(a) and 3(b) show the block diagram and photograph of the developed demonstration system, respectively. It consists of a software-implemented PC, fieldprogrammable gate array (FPGA) development board, and analog front-end circuit board. Chips with 36 SOT devices with an antiferromagnet/ferromagnet bilayer were packed into ceramic packages and mounted on the analog front-end circuit board. The SOT devices play the role of the synapse in the Hopfield model. The PC operates the whole system based on the programmed Hopfield model. The FPGA sends read/write currents to the SOT devices according to control signals received from PC. We here note that, in a final form of sophisticated artificial neural network hardware, the synaptic devices are embedded in an integrated circuit and the circuit performs all the operations that are executed by PC and FPGA in the current proof-of-concept demonstration system.

The SOT devices employed here consisted of a stack with Ta(3)/Pt(2.2)/PtMn(9.5)/Pt(0.6)/[Co(0.3)/Ni(0.6)]<sub>2</sub>/Co(0.3)/ MgO(1)/Ru(1), where the 0.6-nm-thick Pt dusting layer between the PtMn and Co/Ni multilayer was found to enhance both the perpendicular magnetic anisotropy of Co/ Ni multilayer and the exchange bias at the interface.<sup>27</sup> The films were patterned into micrometer-sized Hall devices as shown in Fig. 1(e). The synaptic weight is stored as the magnetization state and extracted as the Hall resistance. Note that while the anomalous Hall effect is used to detect the magnetization state in this proof-of-concept demonstration, the device will be processed into a three-terminal structure<sup>67</sup> for practical use, where the tunneling magnetoresistance effect exhibiting much larger resistance change will be used for reading operation.

Using the developed systems, an associative memory operation was tested for three kinds of  $3 \times 3$ -block patterns, "I, C, and T," shown in Fig. 4(a). The procedure for the associative memory operation is as follows (see Refs. 28 and 68 for details). First, Hall resistance vs. current loops were measured for all the 36 SOT devices, and the region where a virtually linear change of the Hall resistance with the current is ensured for all the 36 devices was determined. This was followed by writing synaptic weights for the "I, C, and T" patterns to each SOT device via the FPGA, where the weight was calculated in the PC based on the Hopfield model and was mapped to the write current based on the measured relation between the Hall resistance and current. At this stage, if the 36 SOT devices were uniform and had sufficient linearity, "I, C, and T" patterns would be already memorized. However, this was not the case due to the variability of the properties among the devices and inevitable non-linearity, and thus correct "I, C, and T" patterns were not recalled from the inputs, even without noise. To compensate for such imperfection of the devices, adjustment of synaptic weights, *i.e.*, a learning process, was performed. In this experiment, Hebbian and anti-Hebbian learning processes<sup>69</sup> were iteratively applied. In this process, we first read  $R_{\rm H}$  from all the devices and configure the synaptic weight matrix in PC. Then, we calculate the recalled pattern from the original three patterns using the synaptic weight matrix. According to the discrepancy between the original pattern and the recalled pattern, the modified synaptic weight matrix to reduce the discrepancy is calculated from the Hebbian and anti-Hebbian learning rule, and new weights are stored to the SOT devices by sending a new set of write current. From a number of trials, we confirmed that the leaning process converges after about 5-20 times iterations, where the recalled patterns match with the original patterns. Figures 4(b) and 4(c) show the measured Hall resistance for 36 SOT devices before and after the learning process, respectively. We confirmed that, after

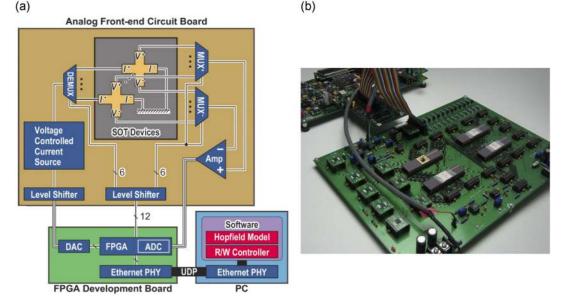


FIG. 3. Demonstration system of artificial neural network. (a) Block diagram. (b) Photograph. Adapted from W. A. Borders, H. Akima, S. Fukami, S. Moriya, S. Kurihara, Y. Horio, S. Sato, and H. Ohno, Appl. Phys. Express **10**(1), 013007 (2017). Copyright 2017 The Japan Society of Applied Physics.<sup>28</sup>

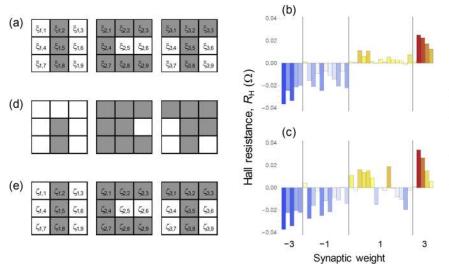


FIG. 4. Associative memory operation. (a) Three kinds of  $3 \times 3$  pattern "I" "C" and "T". [(b), (c)] Hall resistance  $R_{\rm H}$ , representing the synaptic weight, for 36 spin-orbit torque (synaptic) devices before (b) and after (c) the learning process. (d) Example of input noisy patterns, where randomly-selected one block is inverted. (e) Example of associated patterns using Hopfield model.

the learning process, all of the memorized patterns, "I, C, and T," were successfully recalled from the inputs without noise.

Using the synaptic weight matrix after learning [Fig. 4(c)] that memorizes the patterns shown in Fig. 4(a), we then tested the associative memory function, where we input patterns with random noise and calculated the associated patterns based on the Hopfield model. Figure 4(d)shows an example of the input patterns, in which one randomly selected block was inverted, and Fig. 4(e) shows the corresponding associated patterns. Degree of agreement between the input and output (associated) patterns was evaluated by the direction cosine, given by  $(1/N)\xi_{\mu}\zeta_{\mu}$ , where N is the number of blocks (neurons), and  $\xi_{\mu}$  and  $\zeta_{\mu}$  are a number representing the color of each block for memorized and associated patterns, respectively (white = -1, gray = +1). In the case of "I, C, and T" patterns, the ideal value of the direction cosine, calculated for the ideal synaptic weight matrix, is 0.905 for this experiment. The obtained mean direction cosine when we used the synaptic weight matrix before and after the learning process was 0.601 and 0.852, respectively, from 100 trials. The improved direction cosine clearly indicates that the developed artificial synapse can function as an artificial synapse with learning capability, allowing associative memory operation. We also found from a numerical calculation that the remaining gap of the direction cosine to the ideal value is caused by the variability among the devices of the dynamic range of the Hall resistance. The dominant factor and countermeasure of the variability will be described elsewhere.<sup>68</sup>

We finally discuss potential advantage of the proposed approach, i.e., artificial neural network with spintronic artificial synapse, over the conventional computing paradigm. In terms of power consumption and chip area, it has been shown that nonvolatile integrated circuits with digital spintronics devices achieve a significant power reduction by a factor of 1/100 at the same or smaller chip area compared with conventional semiconductor-based integrated circuits, owing to the nonvolatility and back-end-of-line compatibility of spintronics devices.<sup>70–73</sup> This benefit holds true for the artificial neural network paradigm with analog spintronics device. In addition, if one uses nanoscale spintronic synapse with the analog

nature, significant reduction of the count of components should be achieved, leading to further reduction of power consumption and chip size. More importantly, unique features of spintronics devices such as nonvolatility and high endurance allow one to combine two important aspects of brain-inspired computing, learning, and memory. This fact makes the spintronic artificial neural network qualitatively different from conventional systems and offers unexplored opportunities, e.g., low-power, compact, and adaptive systems.

#### **IV. CONCLUSION**

In conclusion, this article has reviewed material and device studies on an artificial spintronic synapse and a proof-of-concept demonstration of artificial neural network using the artificial synapse. Hardware inspired by the structure and information processing mechanism of the brain offers a promising pathway to execute complex cognitive tasks at a lower power consumption level. In particular, to realize high-performance, low-power, and adaptive artificial neural networks, the use of artificial synapses consisting of solid-state devices with nonvolatile and analog-memory functionality provides an attractive approach. We have shown that antiferromagnet/ferromagnet heterostructures operated by the spin-orbit torque not only allow field-free switching of perpendicular magnetization, but also achieve analog control of magnetization depending on the magnitude of applied current. The detailed investigation revealed that the magnetization reversal proceeds in the unit of fine magnetic domain with the scale of around 200 nm, resulting in the analog behavior. Using this analog nature, an artificial neural network was developed, where the 36 analog spin-orbit torque devices were implemented, and Hopfield model-based associative memory operation was tested as а proof-of-concept demonstration of spintronics neuromorphic computing. We confirmed that the artificial spintronic synapse can learn the patterns, enabling execution of the brain-like associative memory operation.

Spintronics devices, in general, allow for high-speed and virtually unlimited read/write operation as well as storage of information without the use of a power supply, holding promise for realization of low-power and adaptive neuromorphic hardware. Through further advances, they will open new avenues for information processing technologies.

#### ACKNOWLEDGMENTS

The authors are grateful to W. A. Borders, A. Kurenkov, C. Igarashi, T. Hirata, H. Iwanuma, K. Goto, C. Zhang, S. DuttaGupta, and H. Sato for discussion and technical supports for the studies of artificial-synapse part and H. Akima, S. Sato, and Y. Horio for the part of artificial neural network. This work was supported in part by the R&D Project for ICT Key Technology to Realize Future Society of MEXT, ImPACT Program of CSTI, JST-OPERA, JSPS KAKENHI Grant No. 17H06093, JSPS Core-to-Core Program, and Cooperative Research Projects of RIEC (H28/B01, H28/A16, H29/B15).

- <sup>1</sup>H. Ohno, T. Endoh, T. Hanyu, N. Kasai, and S. Ikeda, in 2010 IEEE International Electron Devices Meeting, San Francisco, CA, 6–8 December 2010 (IEEE, 2010), pp. 9.4.1–9.4.4.
- <sup>2</sup>D. Silver, A. Huang, C. J. Maddison, A. Guez, L. Sifre, G. van den
- Driessche, J. Schrittwieser, I. Antonoglou, V. Panneershelvam, M. Lanctot, S. Dieleman, D. Grewe, J. Nham, N. Kalchbrenner, I. Sutskever, T. Lillicrap, M. Leach, K. Kavukcuoglu, T. Graepel, and D. Hassabis, Nature **529**, 484 (2016).
- <sup>3</sup>S. Scholze, H. Eisenreich, S. Höppner, G. Ellguth, S. Henker, M. Ander, S. Hänzsche, J. Partzsch, C. Mayr, and R. Schüffny, Integration 45(1), 61–75 (2012).
- <sup>4</sup>P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner,
- W. P. Risk, R. Manohar, and D. S. Modha, Science 345(6197), 668–673 (2014).
  <sup>5</sup>B. V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. R.
- Chandrasekaran, J. M. Bussat, R. Alvarez-Icaza, J. V. Arthur, P. A. Merolla, and K. Boahen, Proc. IEEE **102**(5), 699–716 (2014).
- <sup>6</sup>S. B. Furber, F. Galluppi, S. Temple, and L. A. Plana, Proc. IEEE **102**(5), 652–665 (2014).
- <sup>7</sup>A. Krogh, Nat. Biotechnol. **26**, 195 (2008).
- <sup>8</sup>L. O. Chua, IEEE Trans. Circuit Theory **18**(5), 507 (1971).
- <sup>9</sup>D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, Nature **453**(7191), 80–83 (2008).
- <sup>10</sup>S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nano Lett. **10**(4), 1297–1301 (2010).
- <sup>11</sup>D. Kuzum, R. G. D. Jeyasingh, B. Lee, and H. S. P. Wong, Nano Lett. **12**(5), 2179–2186 (2012).
- <sup>12</sup>Y. Nishitani, Y. Kaneko, M. Ueda, T. Morie, and E. Fujii, J. Appl. Phys. 111(12), 124108 (2012).
- <sup>13</sup>S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes,
- A. Barthélémy, S. Saïghi, and V. Garcia, Nat. Commun. 8, 14736 (2017).
- <sup>14</sup>M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, Nature **521**(7550), 61–64 (2015).
- <sup>15</sup>G. W. Burr, R. M. Shelby, S. Sidler, C. d. Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti, B. N. Kurdi, and H. Hwang, IEEE Trans. Electron Devices **62**(11), 3498–3507 (2015).
- <sup>16</sup>M. Durlam, B. Craigo, M. DeHerrera, B. N. Engel, G. Grynkewich, B. Huang, J. Janesky, M. Martin, B. Martino, J. Salter, J. M. Slaughter, L. Wise, and S. Tehrani, in 2007 IEEE International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Taiwan, 23–25 April 2007 (IEEE, 2007).
- <sup>17</sup>D. Apalkov, B. Dieny, and J. M. Slaughter, Proc. IEEE **104**(10), 1796–1830 (2016).
- <sup>18</sup>S. Bhatti, R. Sbiaa, A. Hirohata, H. Ohno, S. Fukami, and S. N. Piramanayagam, Mater. Today **20**(9), 530–548 (2017).
- <sup>19</sup>N. Locatelli, V. Cros, and J. Grollier, Nature Mater. 13(1), 11–20 (2014).
- <sup>20</sup>J. Grollier, D. Querlioz, and M. D. Stiles, Proc. IEEE **104**(10), 2024–2039 (2016).

- <sup>21</sup>J. Torrejon, M. Riou, F. A. Araujo, S. Tsunegi, G. Khalsa, D. Querlioz, P. Bortolotti, V. Cros, K. Yakushiji, A. Fukushima, H. Kubota, S. Yuasa, M. D. Stiles, and J. Grollier, Nature **547**, 428 (2017).
- <sup>22</sup>D. Zhang, L. Zeng, K. Cao, M. Wang, S. Peng, Y. Zhang, Y. Zhang, J. O. Klein, Y. Wang, and W. Zhao, IEEE Trans. Biomed. Circuits Syst. **10**(4), 828–836 (2016).
- <sup>23</sup>A. Sengupta and K. Roy, Appl. Phys. Express **11**(3), 030101 (2018).
- <sup>24</sup>K. Y. Camsari, R. Faria, B. M. Sutton, and S. Datta, Phys. Rev. X 7(3), 031014 (2017).
- <sup>25</sup>S. Fukami, C. Zhang, S. DuttaGupta, A. Kurenkov, and H. Ohno, Nature Mater. **15**(5), 535–541 (2016).
- <sup>26</sup>A. Kurenkov, C. Zhang, S. DuttaGupta, S. Fukami, and H. Ohno, Appl. Phys. Lett. **110**(9), 092410 (2017).
- <sup>27</sup>W. A. Borders, S. Fukami, and H. Ohno, IEEE Trans. Magn. **53**(11), 6000804 (2017).
- <sup>28</sup>W. A. Borders, H. Akima, S. Fukami, S. Moriya, S. Kurihara, Y. Horio, S. Sato, and H. Ohno, Appl. Phys. Express 10(1), 013007 (2017).
- <sup>29</sup>J. C. Slonczewski, J. Magn. Magn. Mater. **159**(1), L1–L7 (1996).
- <sup>30</sup>L. Berger, Phys. Rev. B **54**(13), 9353–9358 (1996).
- <sup>31</sup>A. Chernyshov, M. Overby, X. Liu, J. K. Furdyna, Y. Lyanda-Geller, and L. P. Rokhinson, Nature Phys. 5(9), 656–659 (2009).
- <sup>32</sup>I. M. Miron, K. Garello, G. Gaudin, P.-J. Zermatten, M. V. Costache, S. Auffret, S. Bandiera, B. Rodmacq, A. Schuhl, and P. Gambardella,
- Nature **476**(7359), 189–193 (2011). <sup>33</sup>M. I. D'yakonov and V. I. Perel, JETP Lett. **13**, 467 (1971).
- <sup>34</sup>J. E. Hirsch, Phys. Rev. Lett. **83**(9), 1834–1837 (1999).
- <sup>35</sup>Y. K. Kato, R. C. Myers, A. C. Gossard, and D. D. Awschalom, Science 306, 1910 (2004).
- <sup>36</sup>J. Wunderlich, B. Kaestner, J. Sinova, and T. Jungwirth, Phys. Rev. Lett. 94(4), 047204 (2005).
- <sup>37</sup>Y. A. Bychkov and E. I. Rashba, JETP Lett. **39**, 78 (1984).
- <sup>38</sup>V. M. Edelstein, Solid State Commun. **73**(3), 233–235 (1990).
- <sup>39</sup>J. Kim, J. Sinha, M. Hayashi, M. Yamanouchi, S. Fukami, T. Suzuki, S. Mitani, and H. Ohno, Nature Mater. **12**(3), 240–245 (2013).
- <sup>40</sup>K. Garello, I. M. Miron, C. O. Avci, F. Freimuth, Y. Mokrousov, S. Blugel, S. Auffret, O. Boulle, G. Gaudin, and P. Gambardella, Nature Nanotech. 8(8), 587–593 (2013).
- <sup>41</sup>L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, Science **336**(6081), 555 (2012).
- <sup>42</sup>S. Fukami, T. Anekawa, C. Zhang, and H. Ohno, Nature Nanotech. **11**(7), 621–625 (2016).
- <sup>43</sup>G. Yu, P. Upadhyaya, Y. Fan, J. G. Alzate, W. Jiang, K. L. Wong, S. Takei, S. A. Bender, L. T. Chang, Y. Jiang, M. Lang, J. Tang, Y. Wang, Y. Tserkovnyak, P. K. Amiri, and K. L. Wang, Nature Nanotech. 9(7), 548–554 (2014).
- <sup>44</sup>L. You, O. Lee, D. Bhowmik, D. Labanowski, J. Hong, J. Bokor, and S. Salahuddin, Proc. Natl. Acad. Sci. **112**(33), 10310–10315 (2015).
- <sup>45</sup>J. Torrejon, F. Garcia-Sanchez, T. Taniguchi, J. Sinha, S. Mitani, J.-V. Kim, and M. Hayashi, Phys. Rev. B **91**(21), 214434 (2015).
- <sup>46</sup>S. C. Baek, V. P. Amin, Y. W. Oh, G. Go, S. J. Lee, G. H. Lee, K. J. Kim, M. D. Stiles, B. G. Park, and K. J. Lee, *Nature Mater.* **17**, 509 (2018).
- <sup>47</sup>Q. Ma, Y. Li, D. B. Gopman, Y. P. Kabanov, R. D. Shull, and C. L. Chien, Phys. Rev. Lett. **120**(11), 117703 (2018).
- <sup>48</sup>E. Saitoh, M. Ueda, H. Miyajima, and G. Tatara, Appl. Phys. Lett. 88(18), 182509 (2006).
- <sup>49</sup>C.-F. Pai, L. Liu, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, Appl. Phys. Lett. **101**(12), 122404 (2012).
- <sup>50</sup>H. Chen, Q. Niu, and A. H. MacDonald, Phys. Rev. Lett. **112**(1), 017205 (2014).
- <sup>51</sup>S. Nakatsuji, N. Kiyohara, and T. Higo, Nature **527**, 212 (2015).
- <sup>52</sup>W. Zhang, M. B. Jungfleisch, W. Jiang, J. E. Pearson, A. Hoffmann, F. Freimuth, and Y. Mokrousov, Phys. Rev. Lett. **113**(19), 196602 (2014).
- <sup>53</sup>W. Zhang, M. B. Jungfleisch, F. Freimuth, W. Jiang, J. Sklenar, J. E. Pearson, J. B. Ketterson, Y. Mokrousov, and A. Hoffmann, Phys. Rev. B **92**(14), 144405 (2015).
- <sup>54</sup>V. Tshitoyan, C. Ciccarelli, A. P. Mihai, M. Ali, A. C. Irvine, T. A. Moore, T. Jungwirth, and A. J. Ferguson, Phys. Rev. B 92(21), 214406 (2015).
- <sup>55</sup>W. Zhang, W. Han, S.-H. Yang, Y. Sun, Y. Zhang, B. Yan, and S. S. P. Parkin, Science Adv. 2(9), e1600759 (2016).
- <sup>56</sup>Y. Ou, S. Shi, D. C. Ralph, and R. A. Buhrman, Phys. Rev. B 93(22), 220405 (2016).
- <sup>57</sup>S. DuttaGupta, T. Kanemura, C. Zhang, A. Kurenkov, S. Fukami, and H. Ohno, Appl. Phys. Lett. **111**(18), 182412 (2017).

- <sup>58</sup>W. H. Meiklejohn and C. P. Bean, Phys. Rev. **102**(5), 1413–1414 (1956).
  <sup>59</sup>Y.-W. Oh, S.-h. Chris Baek, Y. M. Kim, H. Y. Lee, K.-D. Lee, C.-G. Yang,
- E.-S. Park, K.-S. Lee, K.-W. Kim, G. Go, J.-R. Jeong, B.-C. Min, H.-W. Lee, K.-J. Lee, and B.-G. Park, Nature Nanotech. **11**(10), 878–884 (2016).
- <sup>60</sup>A. van den Brink, G. Vermijs, A. Solignac, J. Koo, J. T. Kohlhepp, H. J. Swagten, and B. Koopmans, Nature Commun. 7, 10854 (2016).
- <sup>61</sup>Y. C. Lau, D. Betto, K. Rode, J. M. Coey, and P. Stamenov, Nature Nanotech. 11(9), 758–762 (2016).
- <sup>62</sup>P. Wadley, B. Howells, J. Železný, C. Andrews, V. Hills, R. P. Campion, V. Novák, K. Olejník, F. Maccherozzi, S. S. Dhesi, S. Y. Martin, T. Wagner, J. Wunderlich, F. Freimuth, Y. Mokrousov, J. Kuneš, J. S. Chauhan, M. J. Grzybowski, A. W. Rushforth, K. W. Edmonds, B. L.
- Gallagher, and T. Jungwirth, Science **351**, 587 (2016).
- <sup>63</sup>K. Olejník, V. Schuler, X. Marti, V. Novák, Z. Kašpar, P. Wadley, R. P. Campion, K. W. Edmonds, B. L. Gallagher, J. Garces, M. Baumgartner, P. Gambardella, and T. Jungwirth, Nature Commun. 8, 15434 (2017).
- <sup>64</sup>S. Y. Bodnar, L. Smejkal, I. Turek, T. Jungwirth, O. Gomonay, J. Sinova, A. A. Sapozhnik, H. J. Elmers, M. Klaui, and M. Jourdan, Nature Commun. 9(1), 348 (2018).
- <sup>65</sup>X. Z. Chen, R. Zarzuela, J. Zhang, C. Song, X. F. Zhou, G. Y. Shi, F. Li, H. A. Zhou, W. J. Jiang, F. Pan, and Y. Tserkovnyak, Phys. Rev. Lett. **120**(20), 207204 (2018).

- <sup>66</sup>J. J. Hopfield, Proc. Natl. Acad. Sci. **79**(8), 2554–2558 (1982).
- <sup>67</sup>S. Fukami and H. Ohno, Jpn. J. Appl. Phys. **56**(8), 0802A0801 (2017).
- <sup>68</sup>W. A. Borders, S. Fukami, and H. Ohno, Jpn. J. Appl. Phys. **57**, 1002B2 (2018).
- <sup>69</sup>D. H. Ackley, G. E. Hinton, and T. J. Sejnowski, Cogn. Sci. **9**(1), 147–169 (1985).
- <sup>70</sup>T. Ohsawa, H. Koike, S. Miura, H. Honjo, K. Tokutome, S. Ikeda, T. Hanyu, H. Ohno, and T. Endoh, in 2012 Symposium on VLSI Circuits (VLSIC), Honolulu, HI, 13–15 June 2012 (IEEE, 2012), pp. 46–47.
- <sup>71</sup>S. Matsunaga, N. Sakimura, R. Nebashi, Y. Tsuji, A. Morioka, T. Sugibayashi, S. Miura, H. Honjo, K. Kinoshita, H. Sato, S. Fukami, M. Natsui, A. Mochizuki, S. Ikeda, T. Endoh, H. Ohno, and T. Hanyu, in 2013 Symposium on VLSI Circuits (VLSIC), Kyoto, Japan, 12–14 June 2013 (IEEE, 2013), pp. C106–107.
- <sup>72</sup>D. Suzuki, M. Natsui, A. Mochizuki, S. Miura, H. Honjo, K. Kinoshita, H. Sato, S. Ikeda, T. Endoh, H. Ohno, and T. Hanyu, IEICE Electronics Express 10(23), 20130772 (2013).
- <sup>73</sup>N. Sakimura, Y. Tsuji, R. Nebashi, H. Honjo, A. Morioka, K. Ishihara,
- K. Kinoshita, S. Fukami, S. Miura, N. Kasai, T. Endoh, H. Ohno, T. Hanyu, and T. Sugibayashi, in 2014 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 9–13 February 2014
- (IEEE, 2014), pp. 184–185.