

# PERVEANCE MONITOR FOR MEASURING AN 80-MW KLYSTRON CHARACTERISTICS\*

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## Abstract

The high power klystron-modulator (K&M) system is a main pulse and microwave source for the PLS linac. The peak powers of the modulator and the klystron have 200 MW and 80 MW, respectively. The total heater run time of an oldest klystron system has been accumulated over 75,000-hours as of now. This klystron must operate efficiently and stably in the linear gain region within a band of frequencies. The micro-perveance will change as the tube ages. It is believed that a change in the perveance of the klystron may be a predictor of when a klystron is about to fail. Therefore, it is necessary to monitor the klystron operational status for stable beam operation. It can be achieved by measuring the klystron micro-perveance to diagnose characteristics of klystron. Up to now, the operator manually performs it. The prototype perveance monitor system has been designed by processing the sensing signal of a beam voltage and current of the klystron. In this paper, the design concept and experimental results for application will be presented.

## INTRODUCTION

The high power klystron-modulator (K&M) system is a main pulse and microwave source for the PLS linac. The peak powers of the modulator and the klystron are 200 MW and 80 MW, respectively. This klystron must operate efficiently and stably in the linear gain region within a band of frequencies as well as when the electron gun control electrode voltage changes the beam perveance. It is necessary to define end-of-life for repairs or replacement. A klystron tube shall be considered to have reached end-of-life if the power output at the acceptance test conditions operating levels has dropped to 85% of the values specified for these conditions. It shall also be considered to have reached end-of-life if the micro-perveance decreases to 1.7 [1]. The perveance will change as the tube ages. Perveances of the PLS Linac klystrons are running at about 2 micro-perveance for each klystron. Although we have not lost very many klystrons yet, it is believed that a change in the perveance of the klystron may be a predictor of when a klystron is about to fail. The prototype perveance monitor system has been designed and tested with a klystron at the test laboratory. As a first stage, we applied it to HV processing for a high-power prototype klystron. In this paper, the conceptual design and experimental results will be presented.

## CONCEPTUAL DESIGN

### Perveance definition

The klystron is a device for amplifying signals at microwave radio frequencies. The perveance is an important design parameter since it is totally determined by electron gun dimensions. When the cathode is operated in the space-charge-limited region, the emission current will be a specific function of the applied voltage [2]. The constant,  $k$ , is a function of the geometry of the cathode-anode structure, and is termed perveance. It is space-charge characteristic between electrodes in a klystron tube. It is equal to the current ( $I_k$ ) divided by the electronic potential ( $V_k$ ) of the collector raised to the 3/2 powers [3].

### Basic design concept

The perveance monitor can be divided into two major sections: a pulse conditioning & peak hold module (PCPHM) section, a perveance processor module (PPM) section. The basic concept governing the klystron perveance monitor may be understood via the block diagram shown in Figure 1. The operational function for it can be expressed as an equation (1).

$$I_k = k \cdot V_k^{1.5} \quad (1)$$

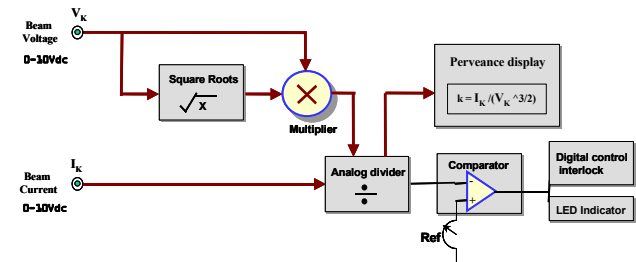


Figure 1: Conceptual block diagram for klystron perveance monitor

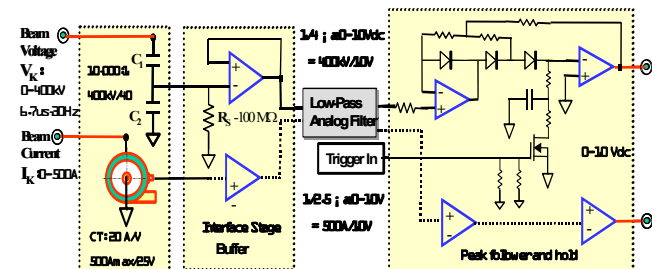


Figure 2: Signal processing concept for analogue input pulse signals.

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Figure 2 shows a signal-processing concept for analogue input pulse signal from the klystron tube. According to the design considerations, the characteristics of the main components are discussed below.

- Capacitive Voltage Divider (CVD): A CVD was chosen as the voltage attenuator. Due to its low loss factor, it is suited for high-voltage applications. Particular shield was also required in the divider shield, in order to confine the parasitic capacitance and compensate for them by proper calibration.
- Interface Stage: When a CVD is connected to an electronic device, the possible effects of the input bias current of the electronic device must be taken into account. A resistor ( $R_s$ ) must be connected in parallel with the low voltage capacitor  $C_2$  of the divider to prevent the input bias current from charging the capacitor itself. The circuit input impedance levels determine the current drain.
- LPF: To avoid amplitude and phase distortions, it must have a constant gain and a linear phase in the pass band. Quantization noise power in the filter output can be reduced by reducing the filter cutoff frequency. The transducer bandwidth is fairly narrower than the maximum permitted, but the accuracy, in terms of equivalent bits, is pushed as high as possible.

**DETAILED SYSTEM CONFIGURATION**

Following the above design considerations, a prototype of a perveance monitor was built. Figure 3 visualizes overview of front side for the hardware configuration. It is consisted of two modules including a pulse conditioning & peak hold module (PCPHM) and a perveance processor module (PPM).

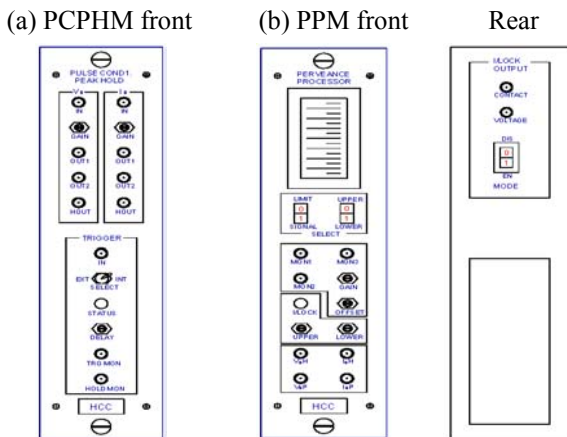


Figure 3: Hardware configuration of the system

The detailed functional block diagram of the realized is shown in Fig. 4 and Fig. 5, respectively [4]. Figure 6 shows photographs for a perveance processor module.

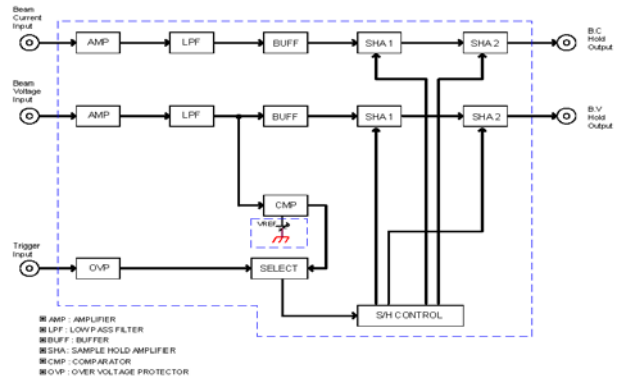


Figure 4: Functional block diagram of PCPHM

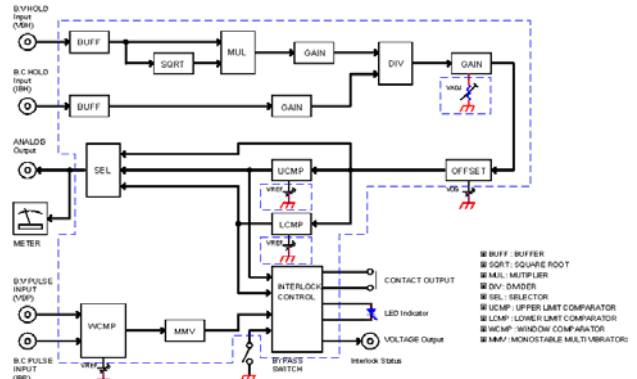


Figure 5: Functional block diagram of PPM

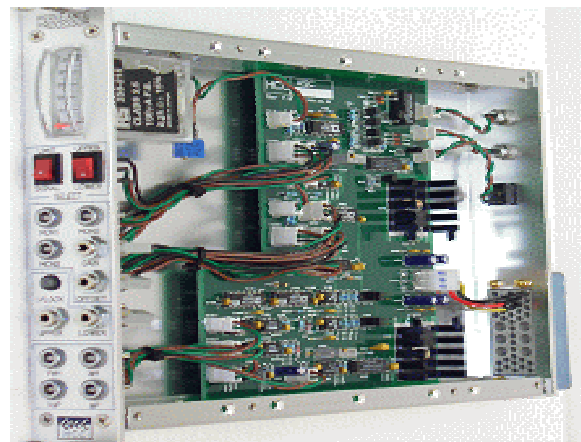


Figure 6: Photographs for a perveance processor module

Main design features of this system can be listed as follows:

- Dual 50 Ohms drive buffers for each beam voltage monitor and beam current monitor.
- High fidelity signal reproduction by slew rate compensation circuits and low pass filter circuits.
- Very short acquisition time and ultra low droop rate by cascading dual sample & hold amplifiers.
- Automatic sample and hold mode arming and releasing operations.
- External and internal trigger generation.

- Front panel accesses on connections and adjustments.
- Easy gain and offset adjustments.
- Interlock bypass by mode key and warming-up detection circuits.
- Various interlock outputs (dry contact, voltage, and indicators).
- Low noise design by using 12V CMOS logics and 4 layer printed circuit boards.

### TEST AND CALIBRATION

The developed system has been performed for the basic functional test and calibration itself based on Fig 5 and 6, respectively.

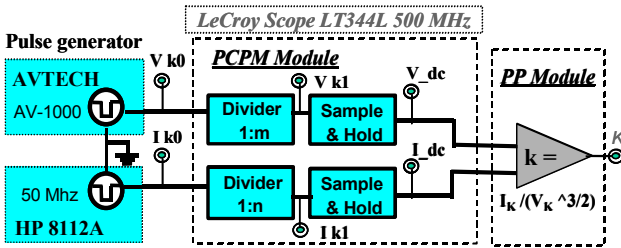


Figure 7: Experimental setup for the output response calibration

The perveance monitor calibration consists of applying a pulse source voltage and measuring the output voltage on each stage. The experimental set-up used for the output response calibration is shown Fig 7.

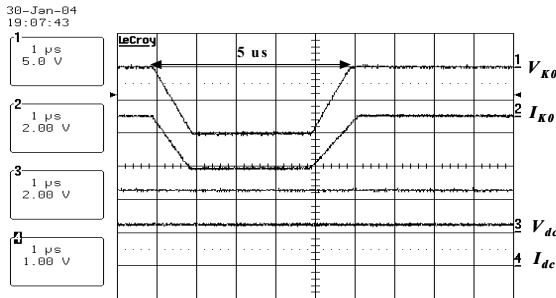


Figure 8: Waveforms of source and response output (Ch1:beam voltage, Ch2:beam current)

A pulse source signal with a width of 5 us and a frequency of 30 Hz is generated across the PCPM module. Along the way, Vdc and Idc are measured. The source and response waveform in each test point is shown in Fig. 8. The perveance is then calculated as the equation (1). Table 1 summarises the measured and calibrated results.

Table 1: Measured and Calibrated Data

| V <sub>k0</sub> (V) | V <sub>dc</sub> (V) | I <sub>k0</sub> (V) | I <sub>dc</sub> (V) | k    |
|---------------------|---------------------|---------------------|---------------------|------|
| 10.010              | 2.500               | 3.133               | 1.248               | 1.98 |
| 9.04                | 2.244               | 2.669               | 1.072               | 1.98 |
| 8.019               | 2.002               | 2.239               | 0.885               | 1.98 |
| 7.010               | 1.757               | 1.832               | 0.726               | 1.98 |
| 6.000               | 1.514               | 1.450               | 0.582               | 1.98 |

Figure 7 shows the linearity trend of calculated and measured data for beam voltage signals.

Within the measuring range of the voltage and current, the voltage variation is about less than 1 %. Test results show that the accuracy of this system has good match with design value.

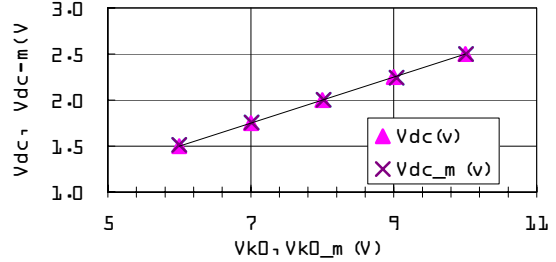


Figure 7: Voltage linearity trend of calculated and measured data

### SUMMARY

The prototype perveance monitor for measuring 80-MW klystron characteristics have been designed and constructed. The test of basic operational functions was demonstrated. So far, the test results have good match to design concept and clearly indicate their usefulness for the perveance monitoring. Now, it is under preparation for the real application test. We will apply this system to HV processing of the electron gun assembly for a high-power prototype klystron that is under development in PAL. Our goal in the test operation is to demonstrate and improve the reliability and stability of the system for a real application, together with the research effort to understand the non-linear characteristics of it. An accuracy of conventional CVD has +/- 5%. In the future, to improve the accuracy, it is needed to study on measuring techniques and calibration for high accuracy of voltage and current.

### ACKNOWLEDGMENTS

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